CHAPTER 5

Bipolar Junction Transistors (BJTs)

Introduction

In this chapter, we study the other major three-terminal device: the bipolar junction transistor (BJT). The presentation of the material in this chapter parallels but does not rely on that for the MOSFET in Chapter 4; thus, if desired, the BJT can be studied before the MOSFET.

Three-terminal devices are far more useful than two-terminal ones, such as the diodes studied in Chapter 3, because they can be used in a multitude of applications, ranging from signal amplification to the design of digital logic and memory circuits. The basic principle involved is the use of the voltage between two terminals to control the current flowing in the third terminal. In this way, a three-terminal device can be used to realize a controlled source, which as we learned in Chapter 1 is the basis for amplifier design. Also, in the extreme, the control signal can be used to cause the current in the third terminal to change from zero to a large value, thus allowing the device to act as a switch. As we learned also in Chapter 1,

the switch is the basis for the realization of the logic inverter, the basic element of digital circuits.

The invention of the BJT in 1948 at the Bell Telephone Laboratories ushered in the era of solid-state circuits, which led to electronics changing the way we work, play, and indeed, live. The invention of the BJT also eventually led to the dominance of information technology and the emergence of the knowledge-based economy.

The bipolar transistor enjoyed nearly three decades as the device of choice in the design of both discrete and integrated circuits. Although the MOSFET had been known very early on, it was not until the 1970s and 1980s that it became a serious competitor to the BJT. At the time of this writing (2003), the MOSFET is undoubtedly the most widely used electronic device, and CMOS technology is the technology of choice in the design of integrated circuits. Nevertheless, the BJT remains a significant device that excels in certain applications. For instance, the reliability of BJT circuits under severe environmental conditions makes them the dominant device in automotive electronics, an important and still-growing area.

The BJT remains popular in discrete circuit design, in which a very wide selection of BJT types are available to the designer. Here we should mention that the characteristics of the bipolar transistor are so well understood that one is able to design transistor circuits whose performance is remarkably predictable and quite insensitive to variations in device parameters.

The BJT is still the preferred device in very demanding analog circuit applications, both integrated and discrete. This is especially true in very-high-frequency applications, such as radio frequency (RF) circuits for wireless systems. A very-high-speed digital logic-circuit family based on bipolar transistors, namely emitter-coupled logic, is still in use. Finally, bipolar transistors can be combined with MOSFETs to create innovative circuits that take advantage of the high-input-impedance and low-power operation of MOSFETs and the very-high-frequency operation and high-current-driving capability of bipolar transistors. The resulting technology is known as BiMOS or BiCMOS, and it is finding increasingly larger areas of application (see Chapters 6, 7, 10, and 11).

In this chapter, we shall start with a simple description of the physical operation of the BJT. Though simple, this physical description provides considerable insight regarding the performance of the transistor as a circuit element. We then quickly move from describing current flow in terms of electrons and holes to a study of the transistor terminal characteristics. Circuit models for transistor operation in different modes will be developed and utilized in the analysis and design of transistor circuits. The main objective of this chapter is to develop in the reader a high degree of familiarity with the BJT. Thus, by the end of the chapter, the reader should be able to perform rapid first-order analysis of transistor circuits and to design single-stage transistor amplifiers and simple logic inverters.

5.1 DEVICE STRUCTURE AND PHYSICAL OPERATION

5.1.1 Simplified Structure and Modes of Operation

Figure 5.1 shows a simplified structure for the BJT. A practical transistor structure will be shown later (see also Appendix A, which deals with fabrication technology).

As shown in Fig. 5.1, the BJT consists of three semiconductor regions: the emitter region (n type), the base region (p type), and the collector region (n type). Such a transistor is called an *npn* transistor. Another transistor, a dual of the *npn* as shown in Fig. 5.2, has a p-type emitter, an n-type base, and a p-type collector and is appropriately called a *pnp* transistor.

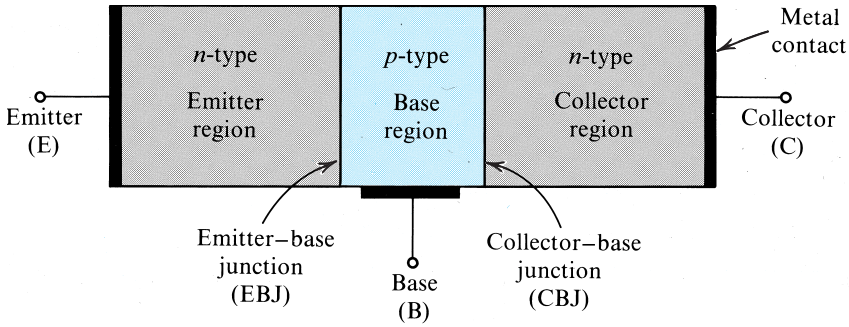


FIGURE 5.1 A simplified structure of the *npn* transistor.

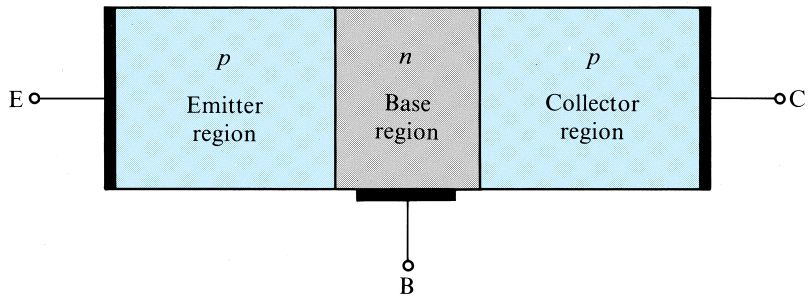


FIGURE 5.2 A simplified structure of the *pnp* transistor.

A terminal is connected to each of the three semiconductor regions of a transistor, with the terminals labeled **emitter** (E), **base** (B), and **collector** (C).

The transistor consists of two *pn* junctions, the **emitter–base junction** (EBJ) and the **collector–base junction** (CBJ). Depending on the bias condition (forward or reverse) of each of these junctions, different modes of operation of the BJT are obtained, as shown in Table 5.1.

The **active mode,** which is also called forward active mode, is the one used if the transistor is to operate as an amplifier. Switching applications (e.g., logic circuits) utilize both the **cutoff** and the **saturation modes.** The **reverse active** (or inverse active) mode has very limited application but is conceptually important.

As we will see shortly, charge carriers of both polarities—that is, electrons and holes—participate in the current conduction process in a bipolar transistor, which is the reason for the name *bipolar*.

TABLE 5.1 BJT Modes of Operation

Mode	EBJ	CBJ
Cutoff	Reverse	Reverse
Active	Forward	Reverse
Reverse active	Reverse	Forward
Saturation	Forward	Forward

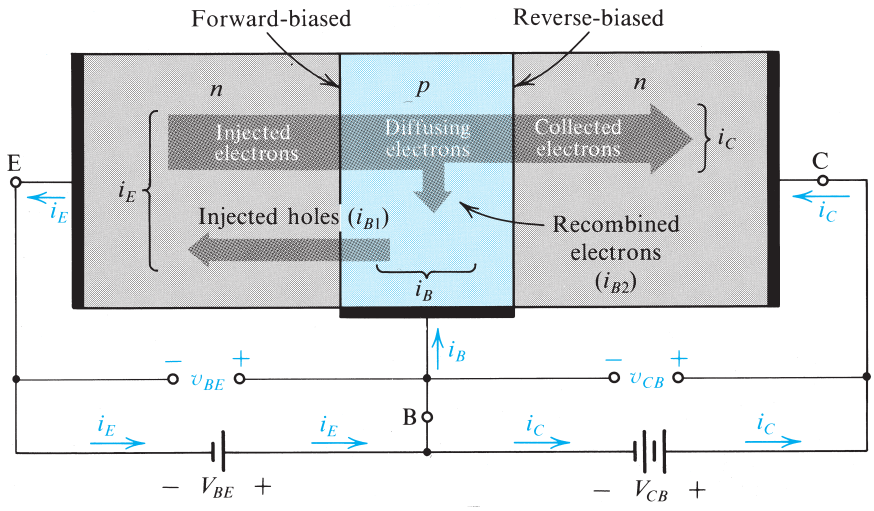


FIGURE 5.3 Current flow in an *npn* transistor biased to operate in the active mode. (Reverse current components due to drift of thermally generated minority carriers are not shown.)

5.1.2 Operation of the *npn* Transistor in the Active Mode

Let us start by considering the physical operation of the transistor in the active mode.[1] This situation is illustrated in Fig. 5.3 for the *npn* transistor. Two external voltage sources (shown as batteries) are used to establish the required bias conditions for active-mode operation. The voltage V_{BE} causes the *p*-type base to be higher in potential than the *n*-type emitter, thus forward-biasing the emitter–base junction. The collector–base voltage V_{CB} causes the *n*-type collector to be higher in potential than the *p*-type base, thus reverse-biasing the collector–base junction.

Current Flow In the following description of current flow only diffusion-current components are considered. Drift currents due to thermally generated minority carriers are usually very small and can be neglected. Nevertheless, we will have more to say about these reverse-current components at a later stage.

The forward bias on the emitter–base junction will cause current to flow across this junction. Current will consist of two components: electrons injected from the emitter into the base, and holes injected from the base into the emitter. As will become apparent shortly, it is highly desirable to have the first component (electrons from emitter to base) at a much higher level than the second component (holes from base to emitter). This can be accomplished by fabricating the device with a heavily doped emitter and a lightly doped base; that is, the device is designed to have a high density of electrons in the emitter and a low density of holes in the base.

The current that flows across the emitter–base junction will constitute the emitter current i_E, as indicated in Fig. 5.3. The direction of i_E is "out of" the emitter lead, which is in the direction of the hole current and opposite to the direction of the electron current, with the emitter current i_E being equal to the sum of these two components. However, since the electron component is much larger than the hole component, the emitter current will be dominated by the electron component.

[1] The material in this section assumes that the reader is familiar with the operation of the *pn* junction under forward-bias conditions (Section 3.X).

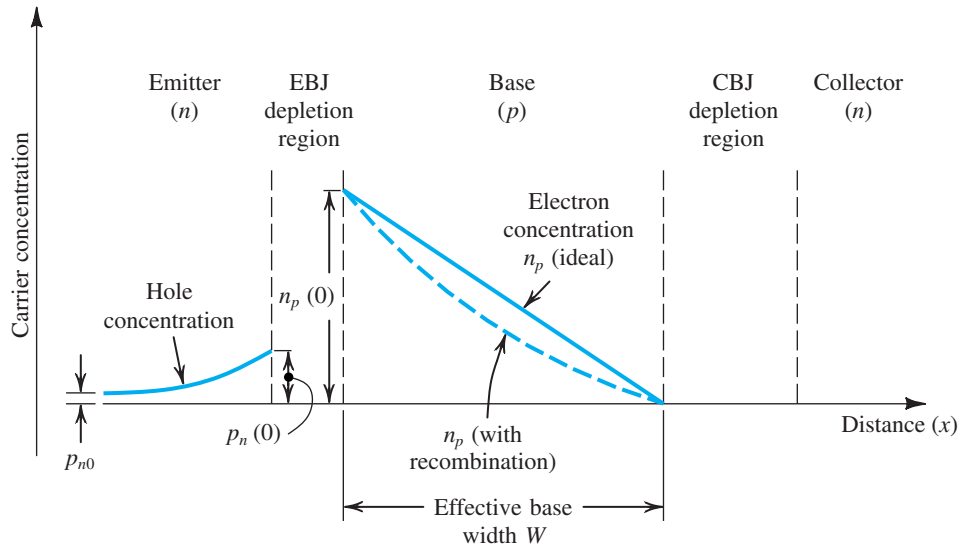


FIGURE 5.4 Profiles of minority-carrier concentrations in the base and in the emitter of an *npn* transistor operating in the active mode: $v_{BE} > 0$ and $v_{CB} \geq 0$.

Let us now consider the electrons injected from the emitter into the base. These electrons will be **minority carriers** in the *p*-type base region. Because the base is usually very thin, in the steady state the excess minority carrier (electron) concentration in the base will have an almost straight-line profile, as indicated by the solid straight line in Fig. 5.4. The electron concentration will be highest [denoted by $n_p(0)$] at the emitter side and lowest (zero) at the collector side.[2] As in the case of any forward-biased *pn* junction (Section 3.X), the concentration $n_p(0)$ will be proportional to e^{v_{BE}/V_T},

$$n_p(0) = n_{p0} e^{v_{BE}/V_T} \tag{5.1}$$

where n_{p0} is the thermal equilibrium value of the minority-carrier (electron) concentration in the base region, v_{BE} is the forward base–emitter bias voltage, and V_T is the thermal voltage, which is equal to approximately 25 mV at room temperature. The reason for the zero concentration at the collector side of the base is that the positive collector voltage v_{CB} causes the electrons at that end to be swept across the CBJ depletion region.

The tapered minority-carrier concentration profile (Fig. 5.4) causes the electrons injected into the base to diffuse through the base region toward the collector. This electron diffusion current I_n is directly proportional to the slope of the straight-line concentration profile,

$$\begin{aligned} I_n &= A_E q D_n \frac{dn_p(x)}{dx} \\ &= A_E q D_n \left(-\frac{n_p(0)}{W} \right) \end{aligned} \tag{5.2}$$

[2] This minority carrier distribution in the base results from the boundary conditions imposed by the two junctions. It is not an exponentially decaying distribution, which would result if the base region were infinitely thick. Rather, the thin base causes the distribution to decay linearly. Furthermore, the reverse bias on the collector–base junction causes the electron concentration at the collector side of the base to be zero.

where A_E is the cross-sectional area of the base–emitter junction (in the direction perpendicular to the page), q is the magnitude of the electron charge, D_n is the electron diffusivity in the base, and W is the effective width of the base. Observe that the negative slope of the minority-carrier concentration results in a negative current I_n across the base; that is, I_n flows from right to left (in the negative direction of x).

Some of the electrons that are diffusing through the base region will combine with holes, which are the majority carriers in the base. However, since the base is usually very thin, the proportion of electrons "lost" through this recombination process will be quite small. Nevertheless, the recombination in the base region causes the excess minority-carrier concentration profile to deviate from a straight line and take the slightly concave shape indicated by the broken line in Fig. 5.4. The slope of the concentration profile at the EBJ is slightly higher than that at the CBJ, with the difference accounting for the small number of electrons lost in the base region through recombination.

The Collector Current From the above we see that most of the diffusing electrons will reach the boundary of the collector–base depletion region. Because the collector is more positive than the base (by v_{CB} volts), these successful electrons will be swept across the CBJ depletion region into the collector. They will thus get "collected" to constitute the collector current i_C. Thus $i_C = I_n$, which will yield a negative value for i_C, indicating that i_C flows in the negative direction of the x axis (i.e., from right to left). Since we will take this to be the positive direction of i_C, we can drop the negative sign in Eq. (5.2). Doing this and substituting for $n_p(0)$ from Eq. (5.1), we can thus express the collector current i_C as

$$i_C = I_S e^{v_{BE}/V_T} \tag{5.3}$$

where the **saturation current** I_S is given by

$$I_S = A_E q D_n n_{p0} / W$$

Substituting $n_{p0} = n_i^2 / N_A$, where n_i is the intrinsic carrier density and N_A is the doping concentration of the base, we can express I_S as

$$I_S = \frac{A_E q D_n n_i^2}{N_A W} \tag{5.4}$$

An important observation to make here is that the magnitude of i_C is independent of v_{CB}. That is, as long as the collector is positive with respect to the base, the electrons that reach the collector side of the base region will be swept into the collector and register as collector current.

The saturation current I_S is inversely proportional to the base width W and is directly proportional to the area of the EBJ. Typically I_S is in the range of 10^{-12} A to 10^{-15} A (depending on the size of the device). Because I_S is proportional to n_i^2, it is a strong function of temperature, approximately doubling for every 5°C rise in temperature. (For the dependence of n_i^2 on temperature, refer to Eq. 3.X.)

Since I_S is directly proportional to the junction area (i.e., the device size), it will also be referred to as the **scale current.** Two transistors that are identical except that one has an EBJ area, say, twice that of the other will have saturation currents with that same ratio (i.e., 2). Thus for the same value of v_{BE} the larger device will have a collector current twice that in the smaller device. This concept is frequently employed in integrated-circuit design.

The Base Current The base current i_B is composed of two components. The first component i_{B1} is due to the holes injected from the base region into the emitter region. This current component is proportional to e^{v_{BE}/V_T},

$$i_{B1} = \frac{A_E q D_p n_i^2}{N_D L_p} e^{v_{BE}/V_T} \tag{5.5}$$

where D_p is the hole diffusivity in the emitter, L_p is the hole diffusion length in the emitter, and N_D is the doping concentration of the emitter.

The second component of base current, i_{B2}, is due to holes that have to be supplied by the external circuit in order to replace the holes lost from the base through the recombination process. An expression for i_{B2} can be found by noting that if the average time for a minority electron to recombine with a majority hole in the base is denoted τ_b (called **minority-carrier lifetime**), then in τ_b seconds the minority-carrier charge in the base, Q_n, recombines with holes. Of course in the steady state, Q_n is replenished by electron injection from the emitter. To replenish the holes, the current i_{B2} must supply the base with a positive charge equal to Q_n every τ_b seconds,

$$i_{B2} = \frac{Q_n}{\tau_b} \tag{5.6}$$

The minority-carrier charge stored in the base region, Q_n, can be found by reference to Fig. 5.4. Specifically, Q_n is represented by the area of the triangle under the straight-line distribution in the base, thus

$$Q_n = A_E q \times \tfrac{1}{2} n_p(0) W$$

Substituting for $n_p(0)$ from Eq. (5.1) and replacing n_{p0} by n_i^2/N_A gives

$$Q_n = \frac{A_E q W n_i^2}{2N_A} e^{v_{BE}/V_T} \tag{5.7}$$

which can be substituted in Eq. (5.6) to obtain

$$i_{B2} = \frac{1}{2} \frac{A_E q W n_i^2}{\tau_b N_A} e^{v_{BE}/V_T} \tag{5.8}$$

Combining Eqs. (5.5) and (5.8) and utilizing Eq. (5.4), we obtain for the total base current i_B the expression

$$i_B = I_S \left(\frac{D_p}{D_n} \frac{N_A}{N_D} \frac{W}{L_p} + \frac{1}{2} \frac{W^2}{D_n \tau_b} \right) e^{v_{BE}/V_T} \tag{5.9}$$

Comparing Eqs. (5.3) and (5.9), we see that i_B can be expressed as a fraction of i_C as follows:

$$i_B = \frac{i_C}{\beta} \tag{5.10}$$

That is,

$$i_B = \left(\frac{I_S}{\beta} \right) e^{v_{BE}/V_T} \tag{5.11}$$

where β is given by

$$\beta = 1 \Big/ \left(\frac{D_p}{D_n} \frac{N_A}{N_D} \frac{W}{L_p} + \frac{1}{2} \frac{W^2}{D_n \tau_b} \right) \tag{5.12}$$

from which we see that β is a constant for the particular transistor. For modern *npn* transistors, β is in the range 100 to 200, but it can be as high as 1000 for special devices. For reasons that will become clear later, the constant β is called the **common-emitter current gain.**

Equation (5.12) indicates that the value of β is highly influenced by two factors: the width of the base region, W, and the relative dopings of the base region and the emitter region, (N_A/N_D). To obtain a high β (which is highly desirable since β represents a gain parameter) the base should be thin (W small) and lightly doped and the emitter heavily doped (N_A/N_D small). Finally, we note that the discussion thus far assumes an idealized situation, where β is a constant for a given transistor.

The Emitter Current Since the current that enters a transistor must leave it, it can be seen from Fig. 5.3 that the emitter current i_E is equal to the sum of the collector current i_C and the base current i_B,

$$i_E = i_C + i_B \tag{5.13}$$

Use of Eqs. (5.10) and (5.13) gives

$$i_E = \frac{\beta+1}{\beta} i_C \tag{5.14}$$

That is,

$$i_E = \frac{\beta+1}{\beta} I_S e^{v_{BE}/V_T} \tag{5.15}$$

Alternatively, we can express Eq. (5.14) in the form

$$i_C = \alpha i_E \tag{5.16}$$

where the constant α is related to β by

$$\alpha = \frac{\beta}{\beta+1} \tag{5.17}$$

Thus the emitter current in Eq. (5.15) can be written

$$i_E = (I_S/\alpha) e^{v_{BE}/V_T} \tag{5.18}$$

Finally, we can use Eq. (5.17) to express β in terms of α; that is,

$$\beta = \frac{\alpha}{1-\alpha} \tag{5.19}$$

It can be seen from Eq. (5.17) that α is a constant (for the particular transistor) that is less than but very close to unity. For instance, if $\beta = 100$, then $\alpha \simeq 0.99$. Equation (5.19) reveals an important fact: Small changes in α correspond to very large changes in β. This mathematical observation manifests itself physically, with the result that transistors of the same type may have widely different values of β. For reasons that will become apparent later, α is called the **common-base current gain.**

Finally, we should note that because α and β characterize the operation of the BJT in the "forward active" mode, as opposed to the "reverse active" mode, which we shall discuss shortly, they are often denoted α_F and β_F. We shall use α and α_F interchangeably and, similarly, β and β_F.

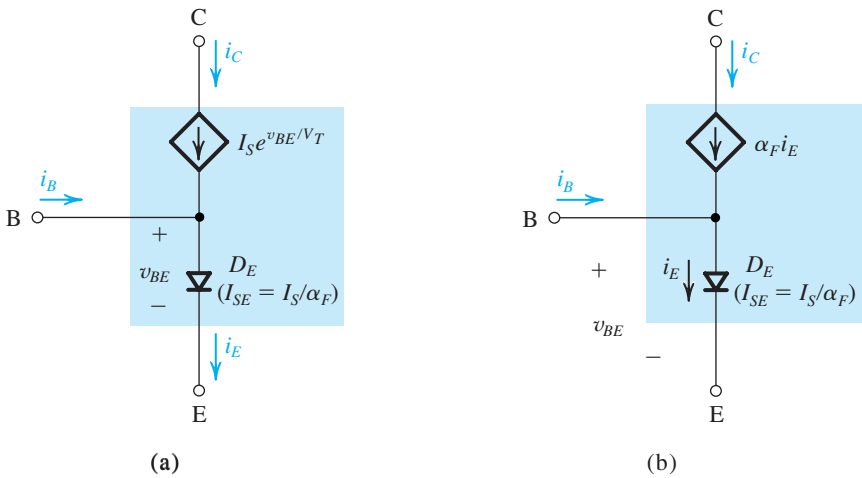


FIGURE 5.5 Large-signal equivalent-circuit models of the *npn* BJT operating in the forward active mode.

Recapitulation and Equivalent-Circuit Models We have presented a first-order model for the operation of the *npn* transistor in the active (or "forward" active) mode. Basically, the forward-bias voltage v_{BE} causes an exponentially related current i_C to flow in the collector terminal. The collector current i_C is independent of the value of the collector voltage as long as the collector–base junction remains reverse-biased; that is, $v_{CB} \geq 0$. Thus in the active mode the collector terminal behaves as an ideal constant-current source where the value of the current is determined by v_{BE}. The base current i_B is a factor $1/\beta_F$ of the collector current, and the emitter current is equal to the sum of the collector and base currents. Since i_B is much smaller than i_C (i.e., $\beta_F \gg 1$), $i_E \simeq i_C$. More precisely, the collector current is a fraction α_F of the emitter current, with α_F smaller than, but close to, unity.

This first-order model of transistor operation in the forward active mode can be represented by the equivalent circuit shown in Fig. 5.5(a). Here diode D_E has a scale current I_{SE} equal to (I_S/α_F) and thus provides a current i_E related to v_{BE} according to Eq. (5.18). The current of the controlled source, which is equal to the collector current, is controlled by v_{BE} according to the exponential relationship indicated, a restatement of Eq. (5.3). This model is in essence a nonlinear voltage-controlled current source. It can be converted to the current-controlled current-source model shown in Fig. 5.5(b) by expressing the current of the controlled source as $\alpha_F i_E$. Note that this model is also nonlinear because of the exponential relationship of the current i_E through diode D_E and the voltage v_{BE}. From this model we observe that if the transistor is used as a two-port network with the input port between E and B and the output port between C and B (i.e., with B as a common terminal), then the current gain observed is equal to α_F. Thus α_F is called the common-base current gain.

EXERCISES

5.1 Consider an *npn* transistor with $v_{BE} = 0.7$ V at $i_C = 1$ mA. Find v_{BE} at $i_C = 0.1$ mA and 10 mA.

Ans. 0.64 V; 0.76 V

5.2 Transistors of a certain type are specified to have β values in the range 50 to 150. Find the range of their α values.

Ans. 0.980 to 0.993

5.3 Measurement of an *npn* BJT in a particular circuit shows the base current to be 14.46 μA, the emitter current to be 1.460 mA, and the base–emitter voltage to be 0.7 V. For these conditions, calculate α, β, and I_S.

Ans. 0.99; 100; 10^{-15} A

5.4 Calculate β for two transistors for which $\alpha = 0.99$ and 0.98. For collector currents of 10 mA, find the base current of each transistor.

Ans. 99; 49; 0.1 mA; 0.2 mA

5.1.3 Structure of Actual Transistors

Figure 5.6 shows a more realistic (but still simplified) cross-section of an *npn* BJT. Note that the collector virtually surrounds the emitter region, thus making it difficult for the electrons injected into the thin base to escape being collected. In this way, the resulting α_F is close to unity and β_F is large. Also, observe that the device is not symmetrical. For more details on the physical structure of actual devices, the reader is referred to Appendix A.

The fact that the BJT structure is not symmetrical means that if the emitter and collector are interchanged and the transistor is operated in the reverse active mode, the resulting values of α and β, denoted α_R and β_R, will be different from the forward active mode values, α_F and β_F. Furthermore, because the structure is optimized for forward mode operation, α_R and β_R will be much lower than their forward mode counterparts. Of course, α_R and β_R are related by equations identical to those that relate α_F and β_F. Typically, α_R is in the range of 0.01 to 0.5, and the corresponding range of β_R is 0.01 to 1.

The structure in Fig. 5.6 indicates also that the CBJ has a much larger area than the EBJ. It follows that if the transistor is operated in the reverse active mode (i.e., with the CBJ forward biased and the EBJ reverse biased) and the operation is modeled in the manner of Fig. 5.5(b), we obtain the model shown in Fig. 5.7. Here diode D_C represents the collector-base junction and has a scale current I_{SC} that is much larger than the scale current I_{SE} of diode D_E. The two scale currents have, of course, the same ratio as the areas of the corresponding junctions. Furthermore, a simple and elegant formula relates the scale currents I_{SE}, I_{SC}, and I_S and the current gains α_F and α_R, namely

$$\alpha_F I_{SE} = \alpha_R I_{SC} = I_S \tag{5.20}$$

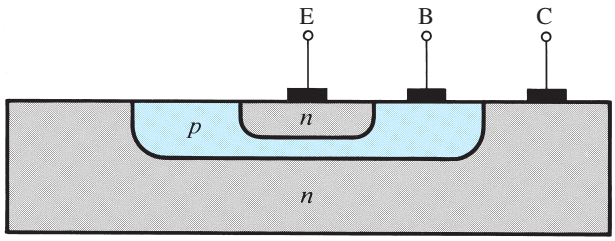


FIGURE 5.6 Cross-section of an *npn* BJT.

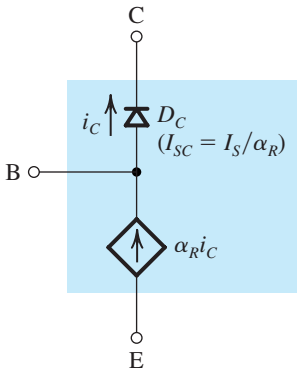


FIGURE 5.7 Model for the *npn* transistor when operated in the reverse active mode (i.e., with the CBJ forward biased and the EBJ reverse biased).

The large scale current I_{SC} has the effect that for the same current, the CBJ exhibits a lower voltage drop when forward biased than the forward voltage drop of the EBJ, V_{BE}. This point will have implications for the BJT's operation in the saturation mode.

EXERCISE

5.5 A particular transistor is said to have $\alpha_F \cong 1$ and $\alpha_R = 0.01$. Its emitter scale current (I_{SE}) is approximately 10^{-15} A. What is its collector scale current (I_{SC})? What is the size of the collector junction relative to the emitter junction? What is the value of β_R?

Ans. 10^{-13} A; 100 times larger; 0.01

5.1.4 The Ebers-Moll (EM) Model

The model of Fig. 5.5(a) can be combined with that of Fig. 5.7 to obtain the circuit model shown in Fig. 5.8. Note that we have relabelled the currents through D_E and D_C and the corresponding control currents of the controlled sources as i_{DE} and i_{DC}. Ebers and Moll, two

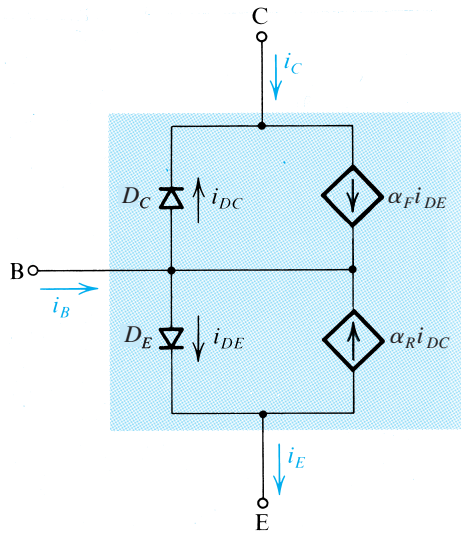


FIGURE 5.8 The Ebers-Moll (EM) model of the *npn* transistor.

early workers in the area, have shown that this composite model can be used to predict the operation of the BJT *in all of its possible modes*. To see how this can be done, we derive expressions for the terminal currents i_E, i_C, and i_B in terms of the junction voltages v_{BE} and v_{BC}. Toward that end, we write an expression for the current at each of the three nodes of the model in Fig. 5.8 as follows:

$$i_E = i_{DE} - \alpha_R i_{DC} \tag{5.21}$$

$$i_C = -i_{DC} + \alpha_F i_{DE} \tag{5.22}$$

$$i_B = (1 - \alpha_F) i_{DE} + (1 - \alpha_R) i_{DC} \tag{5.23}$$

Then we use the diode equation to express i_{DE} and i_{DC} as

$$i_{DE} = I_{SE}(e^{v_{BE}/V_T} - 1) \tag{5.24}$$

and

$$i_{DC} = I_{SC}(e^{v_{BC}/V_T} - 1) \tag{5.25}$$

Substituting for i_{DE} and i_{DC} into Eqs. (5.21), (5.22), and (5.23) and using the relationship in Eq. (5.20) yield the required expressions:

$$i_E = \left(\frac{I_S}{\alpha_F}\right)(e^{v_{BE}/V_T} - 1) - I_S(e^{v_{BC}/V_T} - 1) \tag{5.26}$$

$$i_C = I_S(e^{v_{BE}/V_T} - 1) - \left(\frac{I_S}{\alpha_R}\right)(e^{v_{BC}/V_T} - 1) \tag{5.27}$$

$$i_B = \left(\frac{I_S}{\beta_F}\right)(e^{v_{BE}/V_T} - 1) + \left(\frac{I_S}{\beta_R}\right)(e^{v_{BC}/V_T} - 1) \tag{5.28}$$

where

$$\beta_F = \frac{\alpha_F}{1 - \alpha_F} \tag{5.29}$$

and

$$\beta_R = \frac{\alpha_R}{1 - \alpha_R} \tag{5.30}$$

As a first application of the EM model, we shall use it to predict the terminal currents of a transistor operating in the forward active mode. Here v_{BE} is positive and in the range of 0.6 V to 0.8 V, and v_{BC} is negative. One can easily see that terms containing e^{v_{BC}/V_T} will be negligibly small and can be neglected to obtain

$$i_E \cong \left(\frac{I_S}{\alpha_F}\right)e^{v_{BE}/V_T} + I_S\left(1 - \frac{1}{\alpha_F}\right) \tag{5.31}$$

$$i_C \cong I_S e^{v_{BE}/V_T} + I_S\left(\frac{1}{\alpha_R} - 1\right) \tag{5.32}$$

$$i_B \cong \left(\frac{I_S}{\beta_F}\right)e^{v_{BE}/V_T} - I_S\left(\frac{1}{\beta_F} + \frac{1}{\beta_R}\right) \tag{5.33}$$

In each of these three equations, one can normally neglect the second term on the right-hand side. This results in the familiar current-voltage relationships we derived earlier, namely, Eqs. (5.18), (5.3), and (5.11), respectively.

Thus far, we have stated the condition for forward active mode operation as $v_{CB} \geq 0$ to ensure that the CBJ is reverse biased. In actual fact, however, a *pn* junction does not become effectively forward biased until the forward voltage across it exceeds approximately 0.5 V or so. It follows that one can maintain active mode operation of an *npn* transistor for negative v_{CB} down to approximately -0.4 V or so. This is illustrated in Fig. 5.9, which shows a sketch of i_C versus v_{CB} for an *npn* transistor operated with a constant emitter I_E. Observe that i_C remains constant at $\alpha_F I_E$ for v_{CB} going negative to approximately -0.4 V. Below this value of v_{CB}, the CBJ becomes forward biased and the transistor leaves the active mode and enters the saturation mode of operation, where i_C decreases. We shall study BJT saturation next. For now, however, note that we can use the EM equations to verify that the terms containing e^{v_{BC}/V_T} remain negligibly small for v_{BC} as high as 0.4 V.

EXERCISE

5.6 For a BJT with $\alpha_F = 0.99$, $\alpha_R = 0.02$, and $I_S = 10^{-15}$ A, calculate the second term on the right-hand side of each of Eqs. (5.31), (5.32), and (5.33) to verify that they can be ignored. Then calculate i_E, i_C, and i_B for $v_{BE} = 0.7$ V.

Ans. -10^{-17} A; 49×10^{-15} A; -3×10^{-17} A; 1.461 mA; 1.446 mA; 0.0145 mA

5.1.5 Operation in the Saturation[3] Mode

Figure 5.9 indicates that as v_{CB} is lowered below approximately 0.4 V, the BJT enters the saturation mode of operation. Ideally, v_{CB} has no effect on the collector current in the active mode, but the situation changes dramatically in saturation: Increasing v_{CB} in the negative direction—that is, increasing the forward-bias voltage of the CBJ—reduces i_C. To see this analytically, consider the Ebers-Moll expression for i_C in Eq. (5.27) and, for simplicity, neglect the terms not involving exponentials to obtain

$$i_C = I_S e^{v_{BE}/V_T} - \left(\frac{I_S}{\alpha_R}\right) e^{v_{BC}/V_T} \tag{5.34}$$

The first term on the right-hand side is a result of the forward-biased EBJ, and the second term is a result of the forward-biased CBJ. The second term starts to play a role when v_{BC} exceeds approximately 0.4 V or so. As v_{BC} is increased, this term becomes larger and subtracts from the first term, causing i_C to reduce, eventually reaching zero. Of course, one can operate

[3] Saturation in a BJT means something completely different from that in a MOSFET. The saturation mode of operation of the BJT is analogous to the triode region of operation of the MOSFET. On the other hand, the saturation region of operation of the MOSFET corresponds to the active mode of BJT operation.

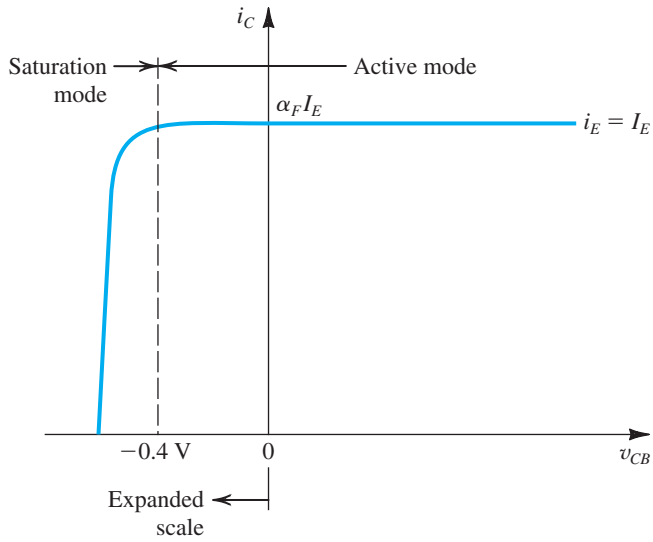


FIGURE 5.9 The i_C–v_{CB} characteristics of an *npn* transistor fed with a constant emitter current I_E. The transistor enters the saturation mode of operation for $v_{CB} < -0.4$ V, and the collector current falls off.

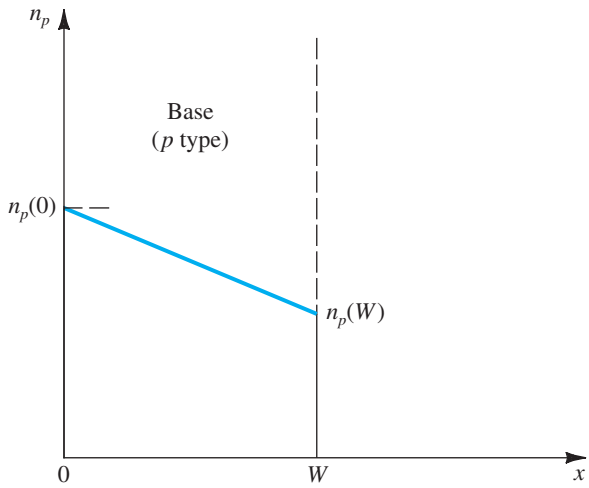


FIGURE 5.10 Concentration profile of the minority carriers (electrons) in the base of an *npn* transistor operating in saturation mode.

the saturated transistor at any value of i_C lower than $\alpha_F I_E$. We will have more to say about saturation-mode operation in subsequent sections. Here, however, it is instructive to examine the minority-carrier concentration profile in the base of the saturated transistor, as shown in Fig. 5.10. Observe that because the CBJ is now forward biased, the electron concentration at the collector edge of the base is no longer zero; rather, it is a value proportional to e^{v_{BC}/V_T}. Also note that the slope of the concentration profile is reduced in correspondence with the reduction in i_C.

EXERCISE

5.7 (a) Use the EM expressions in Eqs. (5.26) and (5.27) to show that the i_C–v_{CB} relationship sketched in Fig. 5.9 can be described by $i_C = \alpha_F I_E + I_S[\alpha_F - (1/\alpha_R)]e^{v_{BC}/V_T}$. Neglect all terms not containing exponentials.

(b) For the case $I_S = 10^{-15}$ A, $I_E = 1$ mA, $\alpha_F \cong 1$, and $\alpha_R = 0.01$, find i_C for $v_{BC} = -1$ V, +0.4 V, +0.5 V, +0.54 V, and +0.57 V. Also find the value of v_{BC} at which $i_C = 0$.

(c) At the value of v_{BC} that makes i_C zero, what do you think i_B should be? Verify using Eq. (5.28).

Ans. 1 mA; 1 mA; 0.95 mA; 0.76 mA; 0.20 mA; 576 mV; 1 mA; 1 mA

5.1.6 The *pnp* Transistor

The *pnp* transistor operates in a manner similar to that of the *npn* device described above. Figure 5.11 shows a *pnp* transistor biased to operate in the active mode. Here the voltage V_{EB} causes the *p*-type emitter to be higher in potential than the *n*-type base, thus forward-biasing the base–emitter junction. The collector–base junction is reverse-biased by the voltage V_{BC}, which keeps the *p*-type collector lower in potential than the *n*-type base.

Unlike the *npn* transistor, current in the *pnp* device is mainly conducted by holes injected from the emitter into the base as a result of the forward-bias voltage V_{EB}. Since the component of emitter current contributed by electrons injected from base to emitter is kept small by using a lightly doped base, most of the emitter current will be due to holes. The electrons injected from base to emitter give rise to the first component of base current, i_{B1}. Also, a number of the holes injected into the base will recombine with the majority carriers in the base (electrons) and will thus be lost. The disappearing base electrons will have to be replaced from the external circuit, giving rise to the second component of base current, i_{B2}. The holes that succeed in reaching the boundary of the depletion region of the collector–base junction will be attracted by the negative voltage on the collector. Thus these holes will be swept across the depletion region into the collector and appear as collector current.

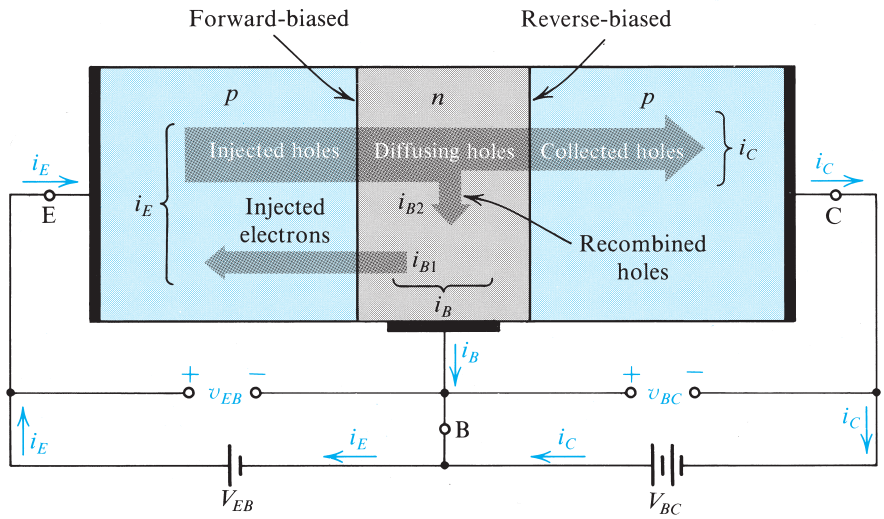


FIGURE 5.11 Current flow in a *pnp* transistor biased to operate in the active mode.

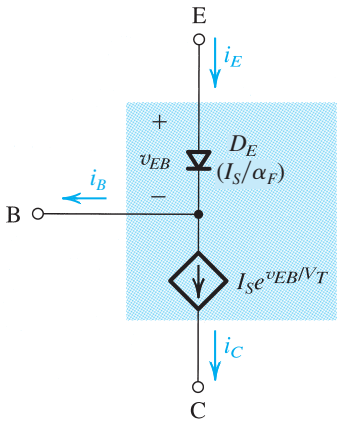


FIGURE 5.12 Large-signal model for the *pnp* transistor operating in the active mode.

It can easily be seen from the above description that the current-voltage relationships of the *pnp* transistor will be identical to those of the *npn* transistor except that v_{BE} has to be replaced by v_{EB}. Also, the large-signal active-mode operation of the *pnp* transistor can be modeled by the circuit depicted in Fig. 5.12. As in the *npn* case, another version of this equivalent circuit is possible in which the current source is replaced with a current-controlled current source $\alpha_F i_E$. Finally, we note that the *pnp* transistor can operate in the saturation mode in a manner analogous to that described for the *npn* device.

EXERCISES

5.8 Consider the model in Fig. 5.12 applied in the case of a *pnp* transistor whose base is grounded, the emitter is fed by a constant-current source that supplies a 2-mA current into the emitter terminal, and the collector is connected to a –10-V dc supply. Find the emitter voltage, the base current, and the collector current if for this transistor $\beta = 50$ and $I_S = 10^{-14}$ A.

Ans. 0.650 V; 39.2 μA; 1.96 mA

5.9 For a *pnp* transistor having $I_S = 10^{-11}$ A and $\beta = 100$, calculate v_{EB} for $i_C = 1.5$ A.

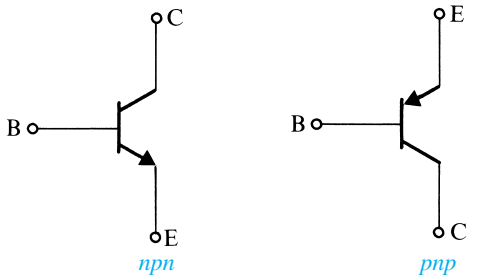
Ans. 0.643 V

5.2 CURRENT-VOLTAGE CHARACTERISTICS

5.2.1 Circuit Symbols and Conventions

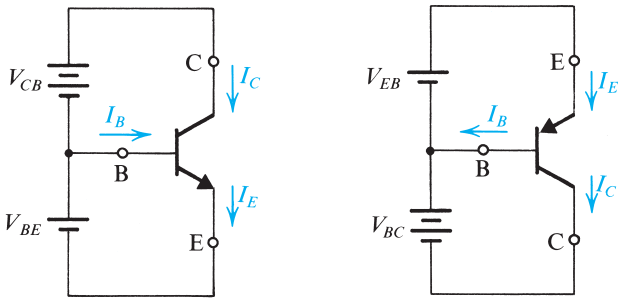
The physical structure used thus far to explain transistor operation is rather cumbersome to employ in drawing the schematic of a multitransistor circuit. Fortunately, a very descriptive and convenient circuit symbol exists for the BJT. Figure 5.13(a) shows the symbol for the *npn* transistor; the *pnp* symbol is given in Fig. 5.13(b). In both symbols the emitter is distinguished by an arrowhead. This distinction is important because, as we have seen in the last section, practical BJTs are not symmetric devices.

The polarity of the device—*npn* or *pnp*—is indicated by the direction of the arrowhead on the emitter. This arrowhead points in the direction of normal current flow in the emitter, which is also the forward direction of the base–emitter junction. Since we have adopted a



(a) (b)

FIGURE 5.13 Circuit symbols for BJTs.



(a) (b)

FIGURE 5.14 Voltage polarities and current flow in transistors biased in the active mode.

drawing convention by which currents flow from top to bottom, we will always draw *pnp* transistors in the manner shown in Fig. 5.13 (i.e., with their emitters on top).

Figure 5.14 shows *npn* and *pnp* transistors biased to operate in the active mode. It should be mentioned in passing that the biasing arrangement shown, utilizing two dc sources, is not a usual one and is used merely to illustrate operation. Practical biasing schemes will be presented in Section 5.5. Figure 5.14 also indicates the reference and actual directions of current flow throughout the transistor. Our convention will be to take the reference direction to coincide with the normal direction of current flow. Hence, normally, we should not encounter a negative value for i_E, i_B, or i_C.

The convenience of the circuit drawing convention that we have adopted should be obvious from Fig. 5.14. Note that currents flow from top to bottom and that voltages are higher at the top and lower at the bottom. The arrowhead on the emitter also implies the polarity of the emitter–base voltage that should be applied in order to forward bias the emitter–base junction. Just a glance at the circuit symbol of the *pnp* transistor, for example, indicates that we should make the emitter higher in voltage than the base (by v_{EB}) in order to cause current to flow into the emitter (downward). Note that the symbol v_{EB} means the voltage by which the emitter (E) is higher than the base (B). Thus for a *pnp* transistor operating in the active mode v_{EB} is positive, while in an *npn* transistor v_{BE} is positive.

From the discussion of Section 5.1 it follows that an *npn* transistor whose EBJ is forward biased will operate in the active mode *as long as the collector voltage does not fall below that of the base by more than approximately 0.4 V*. Otherwise, the transistor leaves the active mode and enters the saturation region of operation.

TABLE 5.2 Summary of the BJT Current-Voltage Relationships in the Active Mode

$$i_C = I_S e^{v_{BE}/V_T}$$

$$i_B = \frac{i_C}{\beta} = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_E = \frac{i_C}{\alpha} = \left(\frac{I_S}{\alpha}\right) e^{v_{BE}/V_T}$$

Note: For the *pnp* transistor, replace v_{BE} with v_{EB}.

$$i_C = \alpha i_E \qquad i_B = (1-\alpha) i_E = \frac{i_E}{\beta+1}$$

$$i_C = \beta i_B \qquad i_E = (\beta+1) i_B$$

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1}$$

V_T = thermal voltage = $\frac{kT}{q} \cong 25$ mV at room temperature

In a parallel manner, the *pnp* transistor will operate in the active mode *if the EBJ is forward biased and the collector voltage is not allowed to rise above that of the base by more than 0.4 V or so*. Otherwise, the CBJ becomes forward biased, and the *pnp* transistor enters the saturation region of operation.

For easy reference, we present in Table 5.2 a summary of the BJT current-voltage relationships in the active mode of operation. Note that for simplicity we use α and β rather than α_F and β_F.

The Constant *n* In the diode equation (Chapter 3) we used a constant n in the exponential and mentioned that its value is between 1 and 2. For modern bipolar junction transistors the constant n is close to unity except in special cases: (1) at high currents (i.e., high relative to the normal current range of the particular transistor) the i_C–v_{BE} relationship exhibits a value for n that is close to 2, and (2) at low currents the i_B–v_{BE} relationship shows a value for n of approximately 2. Note that for our purposes we shall assume always that $n = 1$.

The Collector–Base Reverse Current (I_{CBO}) In our discussion of current flow in transistors we ignored the small reverse currents carried by thermally generated minority carriers. Although such currents can be safely neglected in modern transistors, the reverse current across the collector–base junction deserves some mention. This current, denoted I_{CBO}, is the reverse current flowing from collector to base with the emitter open-circuited (hence the subscript O). This current is usually in the nanoampere range, a value that is many times higher than its theoretically predicted value. As with the diode reverse current, I_{CBO} contains a substantial leakage component, and its value is dependent on v_{CB}. I_{CBO} depends strongly on temperature, approximately doubling for every 10°C rise.[4]

[4] The temperature coefficient of I_{CBO} is different from that of I_S because I_{CBO} contains a substantial leakage component.

EXAMPLE 5.1

The transistor in the circuit of Fig. 5.15(a) has $\beta = 100$ and exhibits a v_{BE} of 0.7 V at $i_C = 1$ mA. Design the circuit so that a current of 2 mA flows through the collector and a voltage of +5 V appears at the collector.

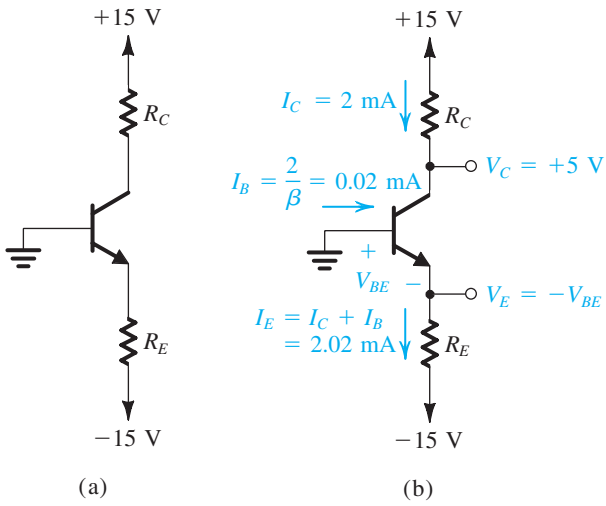


FIGURE 5.15 Circuit for Example 5.1.

Solution

Refer to Fig. 5.15(b). We note at the outset that since we are required to design for $V_C = +5$ V, the CBJ will be reverse biased and the BJT will be operating in the active mode. To obtain a voltage $V_C = +5$ V the voltage drop across R_C must be 15 – 5 = 10 V. Now, since $I_C = 2$ mA, the value of R_C should be selected according to

$$R_C = \frac{10 \text{ V}}{2 \text{ mA}} = 5 \text{ k}\Omega$$

Since $v_{BE} = 0.7$ V at $i_C = 1$ mA, the value of v_{BE} at $i_C = 2$ mA is

$$V_{BE} = 0.7 + V_T \ln\left(\frac{2}{1}\right) = 0.717 \text{ V}$$

Since the base is at 0 V, the emitter voltage should be

$$V_E = -0.717 \text{ V}$$

For $\beta = 100$, $\alpha = 100/101 = 0.99$. Thus the emitter current should be

$$I_E = \frac{I_C}{\alpha} = \frac{2}{0.99} = 2.02 \text{ mA}$$

Now the value required for R_E can be determined from

$$R_E = \frac{V_E - (-15)}{I_E}$$
$$= \frac{-0.717 + 15}{2.02} = 7.07 \text{ k}\Omega$$

This completes the design. We should note, however, that the calculations above were made with a degree of accuracy that is usually neither necessary nor justified in practice in view, for instance, of the expected tolerances of component values. Nevertheless, we chose to do the design precisely in order to illustrate the various steps involved.

EXERCISES

5.10 In the circuit shown in Fig. E5.10, the voltage at the emitter was measured and found to be –0.7 V. If $\beta = 50$, find I_E, I_B, I_C, and V_C.

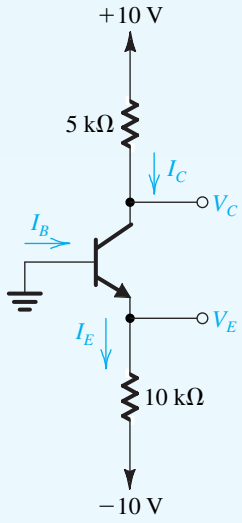


FIGURE E5.10

Ans. 0.93 mA; 18.2 μA; 0.91 mA; +5.45 V

5.11 In the circuit shown in Fig. E5.11, measurement indicates V_B to be +1.0 V and V_E to be +1.7 V. What are α and β for this transistor? What voltage V_C do you expect at the collector?

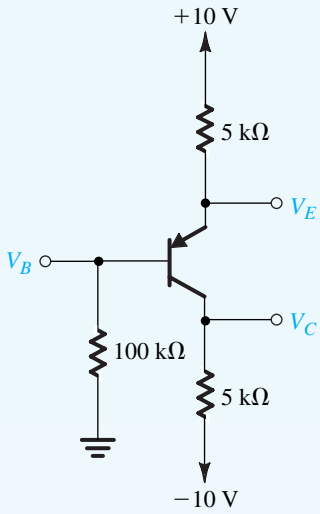


FIGURE E5.11

Ans. 0.994; 165; –1.75 V

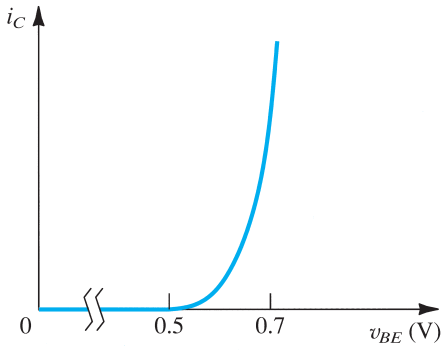


FIGURE 5.16 The i_C–v_{BE} characteristic for an *npn* transistor.

5.2.2 Graphical Representation of Transistor Characteristics

It is sometimes useful to describe the transistor i–v characteristics graphically. Figure 5.16 shows the i_C–v_{BE} characteristic, which is the exponential relationship

$$i_C = I_S e^{v_{BE}/V_T}$$

which is identical (except for the value of constant n) to the diode i–v relationship. The i_E–v_{BE} and i_B–v_{BE} characteristics are also exponential but with different scale currents: I_S/α for i_E, and I_S/β for i_B. Since the constant of the exponential characteristic, $1/V_T$, is quite high ($\simeq$40), the curve rises very sharply. For v_{BE} smaller than about 0.5 V, the current is negligibly small.[5] Also, over most of the normal current range v_{BE} lies in the range of 0.6 V to 0.8 V. In performing rapid first-order dc calculations we normally will assume that $V_{BE} \simeq 0.7$ V, which is similar to the approach used in the analysis of diode circuits (Chapter 3). For a *pnp* transistor, the i_C–v_{EB} characteristic will look identical to that of Fig. 5.16.

As in silicon diodes, the voltage across the emitter–base junction decreases by about 2 mV for each rise of 1°C in temperature, provided that the junction is operating at a constant current. Figure 5.17 illustrates this temperature dependence by depicting i_C–v_{BE} curves at three different temperatures for an *npn* transistor.

The Common-Base Characteristics One way to describe the operation of a transistor is to plot i_C versus v_{CB} for various values of i_E. We have already encountered one such graph, in Fig. 5.9, which we used to introduce the saturation mode of operation. A conceptual experimental setup for measuring such characteristics is shown in Fig. 5.18(a). Observe that in these measurements the base voltage is held constant, here at ground potential, and thus the base serves as a common terminal between the input and output ports. Consequently, the resulting set of characteristics, shown in Fig. 5.18(b), are known as common-base characteristics.

[5] The i_C–v_{BE} characteristic is the BJT's counterpart of the i_D–v_{GS} characteristic of the enhancement MOSFET. They share an important attribute: In both cases the voltage has to exceed a "threshold" for the device to conduct appreciably. In the case of the MOSFET, there is a formal threshold voltage, V_t, which lies in the range of 0.6 V to 0.8 V. For the BJT, there is an "apparent threshold" of approximately 0.5 V. The i_D–v_{GS} characteristic of the MOSFET is parabolic and thus is less steep than the i_C–v_{BE} characteristic of the BJT. This difference has a direct and significant implication to the value of transconductance g_m realized with each device.

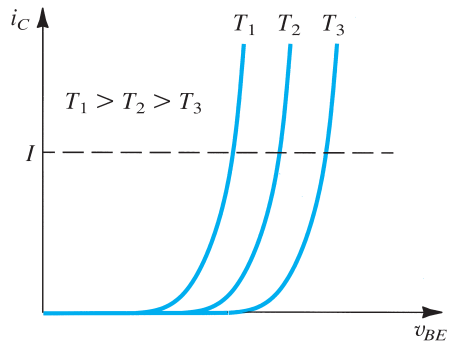


FIGURE 5.17 Effect of temperature on the i_C–v_{BE} characteristic. At a constant emitter current (broken line), v_{BE} changes by –2 mV/°C.

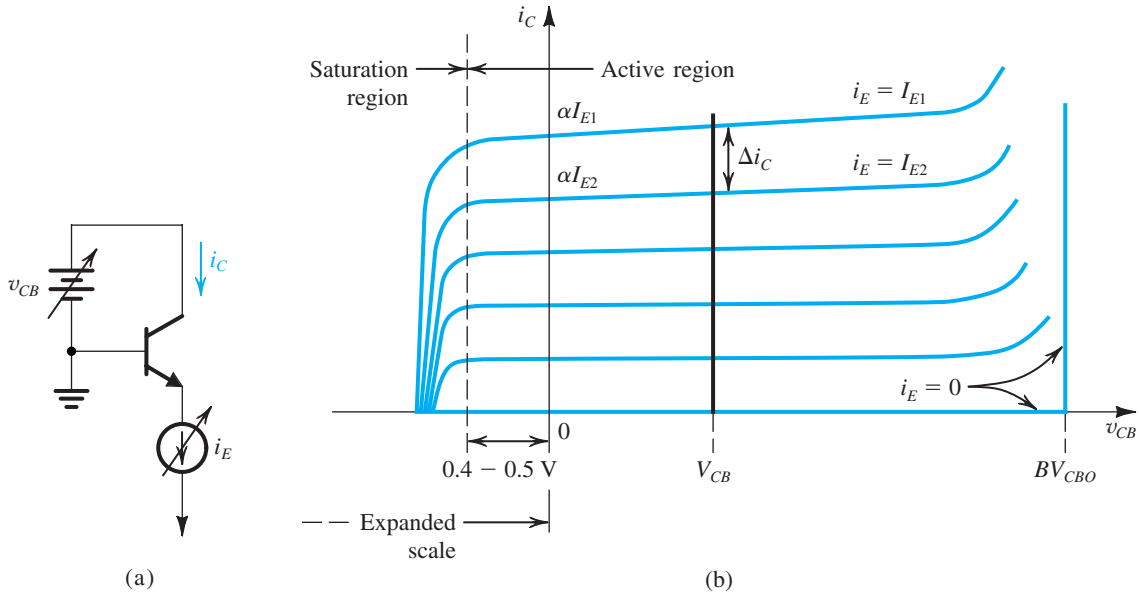


FIGURE 5.18 The i_C–v_{CB} characteristics for an *npn* transistor.

In the active region of operation, obtained for $v_{CB} \geq -0.4$ V or so, the i_C–v_{CB} curves deviate from our expectations in two ways. First, the curves are not horizontal straight lines but show a small positive slope, indicating that i_C depends slightly on v_{CB} in the active mode. We shall discuss this phenomenon shortly. Second, at relatively large values of v_{CB}, the collector current shows a rapid increase, which is a breakdown phenomenon we will consider at a later stage.

As indicated in Fig. 5.18(b), each of the characteristic curves intersects the vertical axis at a current level equal to αI_E, where I_E is the constant emitter current at which the particular curve is measured. The resulting value of α is a **total** or **large-signal** α; that is, $\alpha = i_C/i_E$, where i_C and i_E denote total collector and emitter currents, respectively. Here we recall that α is appropriately called the common-base current gain. An **incremental** or **small-signal** α can be determined by measuring the change in i_C, Δi_C, obtained as a result of changing i_E by an increment Δi_E, $\alpha \equiv \Delta i_C/\Delta i_E$. This measurement is usually made at a constant v_{CB}, as indicated in Fig. 5.18(b). Usually, the values of incremental and total α differ slightly, but we shall not make a distinction between the two in this book.

Finally, turning to the saturation region, the Ebers-Moll equations can be used to obtain the following expression for the i_C–v_{CB} curve in the saturation region (for $i_E = I_E$),

$$i_C = \alpha_F I_E - I_S\left(\frac{1}{\alpha_R} - \alpha_F\right)e^{v_{BC}/V_T} \tag{5.35}$$

We can use this equation to determine the value of v_{BC} at which i_C is reduced to zero. Recalling that the CBJ is much larger than the EBJ, the forward-voltage drop v_{BC} will be smaller than v_{BE} resulting in a collector-emitter voltage, v_{CE}, of 0.1 V to 0.3 V in saturation.

EXERCISES

5.12 Consider a *pnp* transistor with $v_{EB} = 0.7$ V at $i_E = 1$ mA. Let the base be grounded, the emitter be fed by a 2-mA constant-current source, and the collector be connected to a –5-V supply through a 1-kΩ resistance. If the temperature increases by 30°C, find the changes in emitter and collector voltages. Neglect the effect of I_{CBO}.

Ans. –60 mV; 0 V.

5.13 Find the value of v_{CB} at which i_C of an *npn* transistor operated in the CB configuration with $I_E = 1$ mA is reduced (a) to half its active-mode value and (b) to zero. Assume $\alpha_F \cong 1$ and $\alpha_R = 0.1$. The value of V_{BE} was measured for $v_{CB} = 0$ [see measuring setup in Fig. 5.18(a)] and found to be 0.70 V. Repeat (a) and (b) for $\alpha_R = 0.01$.

Ans. 0.628 V; 0.645 V; 0.568 V; 0.585 V.

5.2.3 Dependence of i_C on the Collector Voltage—The Early Effect

When operated in the active region, practical BJTs show some dependence of the collector current on the collector voltage, with the result that their i_C–v_{CB} characteristics are not perfectly horizontal straight lines. To see this dependence more clearly, consider the conceptual circuit shown in Fig. 5.19(a). The transistor is connected in the **common-emitter configuration;** that is, here the emitter serves as a common terminal between the input and output ports. The voltage V_{BE} can be set to any desired value by adjusting the dc source connected between base and emitter. At each value of V_{BE}, the corresponding i_C–v_{CE} characteristic curve can be measured point-by-point by varying the dc source connected between collector and emitter and measuring the corresponding collector current. The result is the family of i_C–v_{CE} characteristic curves shown in Fig. 5.19(b) and known as **common-emitter characteristics.**

At low values of v_{CE}, as the collector voltage goes below that of the base by more than 0.4 V, the collector–base junction becomes forward biased and the transistor leaves the active mode and enters the saturation mode. We shall shortly look at the details of the i_C–v_{CE} curves in the saturation region. At this time, however, we wish to examine the characteristic curves in the active region in detail. We observe that the characteristic curves, though still straight lines, have finite slope. In fact, when extrapolated, the characteristic lines meet at a point on the negative v_{CE} axis, at $v_{CE} = -V_A$. The voltage V_A, a positive number, is a parameter for the particular BJT, with typical values in the range of 50 V to 100 V. It is called the **Early voltage,** after J. M. Early, the engineering scientist who first studied this phenomenon.

At a given value of v_{BE}, increasing v_{CE} increases the reverse-bias voltage on the collector–base junction and thus increases the width of the depletion region of this junction (refer to Fig. 5.3). This in turn results in a decrease in the **effective base width** W. Recalling that I_S is inversely proportional to W (Eq. 5.4), we see that I_S will increase and that i_C increases proportionally. This is the Early effect.

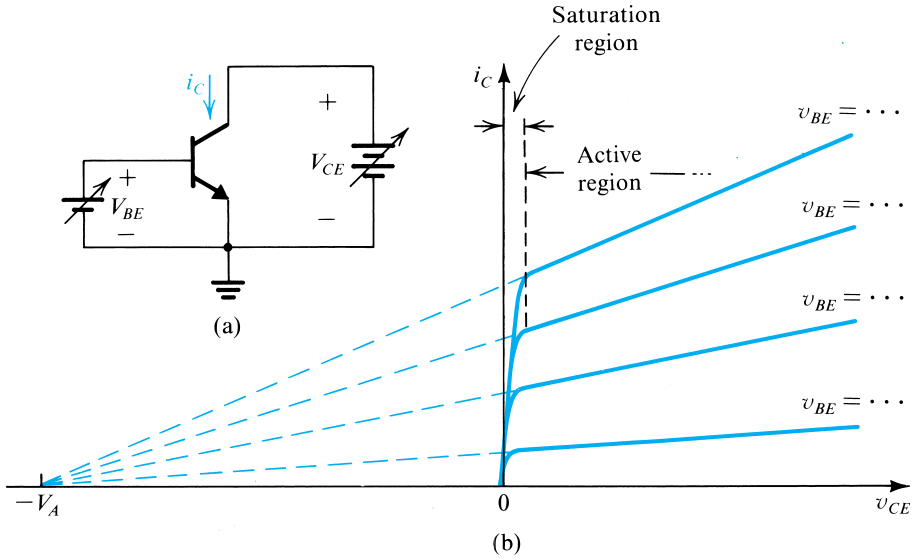


FIGURE 5.19 **(a)** Conceptual circuit for measuring the i_C–v_{CE} characteristics of the BJT. **(b)** The i_C–v_{CE} characteristics of a practical BJT.

The linear dependence of i_C on v_{CE} can be accounted for by assuming that I_S remains constant and including the factor $(1 + v_{CE}/V_A)$ in the equation for i_C as follows:

$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right) \tag{5.36}$$

The nonzero slope of the i_C–v_{CE} straight lines indicates that the **output resistance** looking into the collector is not infinite. Rather, it is finite and defined by

$$r_o \equiv \left[\frac{\partial i_C}{\partial v_{CE}}\bigg|_{v_{BE}=\text{constant}}\right]^{-1} \tag{5.37}$$

Using Eq. (5.36) we can show that

$$r_o = \frac{V_A + V_{CE}}{I_C} \tag{5.38}$$

where I_C and V_{CE} are the coordinates of the point at which the BJT is operating on the particular i_C–v_{CE} curve (i.e., the curve obtained for $v_{BE} = V_{BE}$). Alternatively, we can write

$$r_o = \frac{V_A}{I'_C} \tag{5.38a}$$

where I'_C is the value of the collector current with the Early effect neglected; that is,

$$I'_C = I_S e^{V_{BE}/V_T} \tag{5.38b}$$

It is rarely necessary to include the dependence of i_C on v_{CE} in dc bias design and analysis. However, the finite output resistance r_o can have a significant effect on the gain of transistor amplifiers, as will be seen in later sections and chapters.

The output resistance r_o can be included in the circuit model of the transistor. This is illustrated in Fig. 5.20, where we show large-signal circuit models of a common-emitter *npn* transistor operating in the active mode. Observe that diode D_B models the exponential dependence of i_B on v_{BE} and thus has a scale current $I_{SB} = I_S/\beta$. Also note that the two models

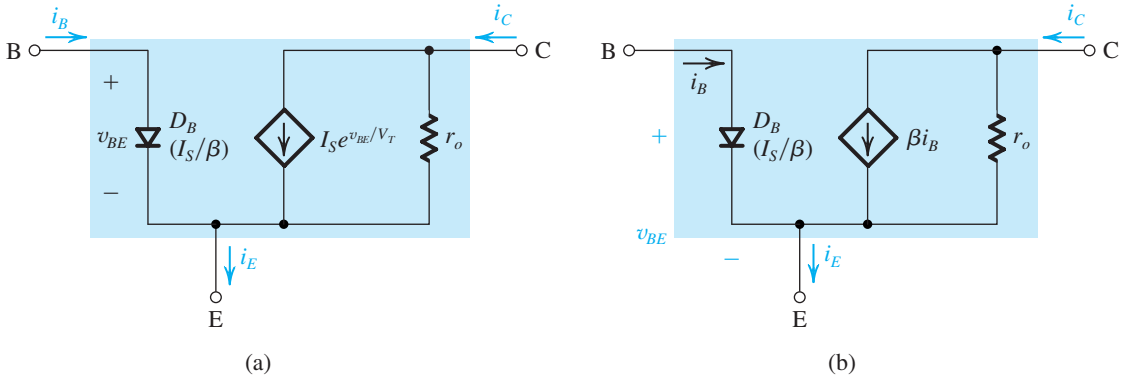


FIGURE 5.20 Large-signal equivalent-circuit models of an *npn* BJT operating in the active mode in the common-emitter configuration.

differ only in how the control function of the transistor is expressed: In the circuit of Fig. 5.20(a), voltage v_{BE} controls the collector current source, while in the circuit of Fig. 5.20(b), the base current i_B is the control parameter for the current source βi_B. Here we note that β represents the ideal current gain (i.e., when r_o is not present) of the common-emitter configuration, which is the reason for its name, the **common-emitter current gain.**

EXERCISES

5.14 Find the output resistance of a BJT for which $V_A = 100$ V at $I_C = 0.1$, 1, and 10 mA.

Ans. 1 MΩ; 100 kΩ; 10 kΩ

5.15 Consider the circuit in Fig. 5.19(a). At $V_{CE} = 1$ V, V_{BE} is adjusted to yield a collector current of 1 mA. Then, while V_{BE} is kept constant, V_{CE} is raised to 11 V. Find the new value of I_C. For this transistor, $V_A = 100$ V.

Ans. 1.1 mA

5.2.4 The Common-Emitter Characteristics

An alternative way of expressing the transistor common-emitter characteristics is illustrated in Fig. 5.21. Here the base current i_B rather than the base–emitter voltage v_{BE} is used as a parameter. That is, each i_C–v_{CE} curve is measured with the base fed with a constant current I_B. The resulting characteristics look similar to those in Fig. 5.19 except that here we show the breakdown phenomenon, which we shall discuss shortly. We should also mention that although it is not obvious from the graphs, the slope of the curves in the active region of operation differs from the corresponding slope in Fig. 5.19. This, however, is a rather subtle point and beyond our interest at this moment.

The Common-Emitter Current Gain β An important transistor parameter is the common-emitter current gain β_F or simply β. Thus far we have defined β as the ratio of the total current in the collector to the total current in the base, and we have assumed that β is constant for a given transistor, independent of the operating conditions. In the following we examine those two points in some detail.

Consider a transistor operating in the active region at the point labeled Q in Fig. 5.21, that is, at a collector current I_{CQ}, a base current I_{BQ}, and a collector-emitter voltage V_{CEQ}. The

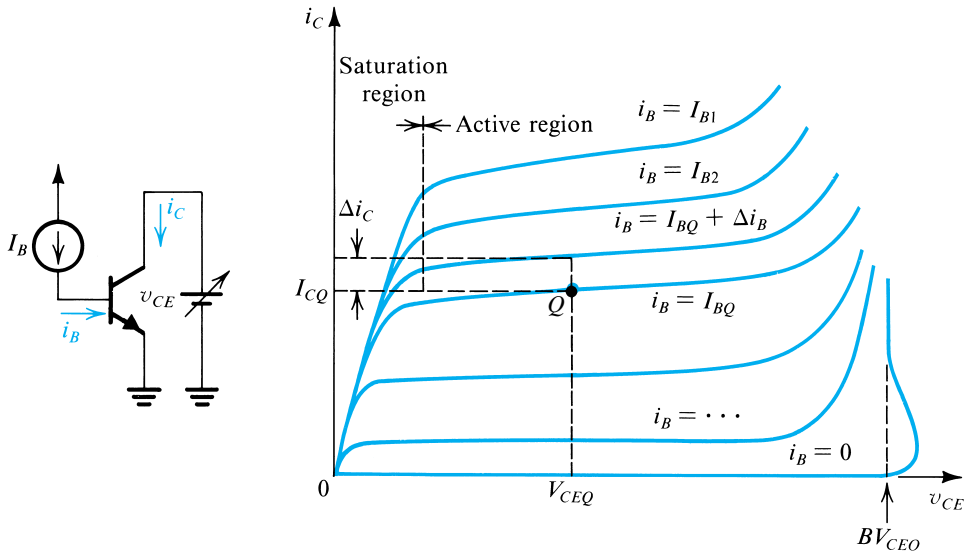


FIGURE 5.21 Common-emitter characteristics. Note that the horizontal scale is expanded around the origin to show the saturation region in some detail.

ratio of the collector current to the base current is the **large-signal or dc** β,

$$\beta_{\text{dc}} \equiv \frac{I_{CQ}}{I_{BQ}} \tag{5.39}$$

which is the β we have been using in our description of transistor operation. It is commonly referred to on the manufacturer's data sheets as h_{FE}, a symbol that comes from the use of the hybrid, or h, two-port parameters to characterize transistor operation (see Appendix X and Appendix Y). One can define another β based on incremental or small-signal quantities. Referring to Fig. 5.21 we see that while keeping v_{CE} constant at the value V_{CEQ}, changing i_B from I_{BQ} to $(I_{BQ} + \Delta i_B)$ results in i_C increasing from I_{CQ} to $(I_{CQ} + \Delta i_C)$. Thus we can define the **incremental or ac** β, β_{ac}, as

$$\beta_{\text{ac}} = \left.\frac{\Delta i_C}{\Delta i_B}\right|_{v_{CE}=\text{constant}} \tag{5.40}$$

The magnitudes of β_{ac} and β_{dc} differ, typically by approximately 10% to 20%. In this book we shall not normally make a distinction between the two. Finally, we should mention that the small-signal β or β_{ac} is also known by the alternate symbol h_{fe}. Because the small-signal β or h_{fe} is defined and measured at a constant v_{CE}—that is, with a zero signal component between collector and emitter—it is known as the **short-circuit common-emitter current gain.**

The value of β depends on the current at which the transistor is operating and the relationship takes the form shown in Fig. 5.22. The physical processes that give rise to this relationship are beyond the scope of this book. Figure 5.22 also shows the temperature dependence of β.

The Saturation Voltage V_{CEsat} and Saturation Resistance R_{CEsat} An expanded view of the common-emitter characteristics in the saturation region is shown in Fig. 5.23. The fact that the curves are "bunched" together in the saturation region implies that the incremental β is lower than in the active region. A possible operating point in the saturation region is that labeled X. It is characterized by a base current I_B, a collector current $I_{C\text{sat}}$, and a collector–emitter voltage $V_{CE\text{sat}}$. Note that $I_{C\text{sat}} < \beta_F I_B$. Since the value of $I_{C\text{sat}}$ is decided on

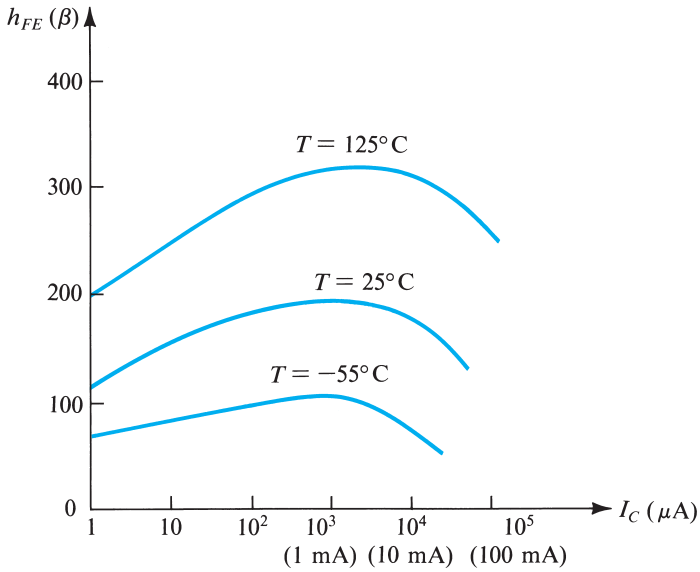


FIGURE 5.22 Typical dependence of β on I_C and on temperature in a modern integrated-circuit *npn* silicon transistor intended for operation around 1 mA.

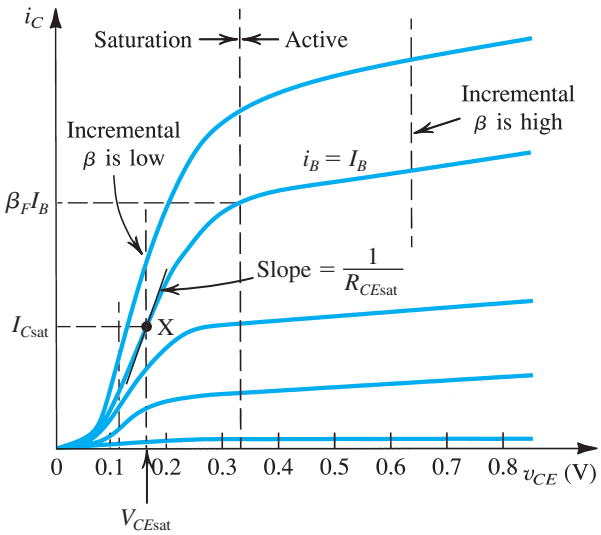


FIGURE 5.23 An expanded view of the common-emitter characteristics in the saturation region.

by the circuit designer, a saturated transistor is said to be operating at a **forced** β given by

$$\beta_{\text{forced}} \equiv \frac{I_{C\text{sat}}}{I_B} \tag{5.41}$$

Thus,

$$\beta_{\text{forced}} < \beta_F \tag{5.42}$$

The ratio of β_F to β_{forced} is known as the **overdrive factor.** The greater the overdrive factor, the deeper the transistor is driven into saturation and the lower $V_{CE\text{sat}}$ becomes.

The i_C–v_{CE} curves in saturation are rather steep, indicating that the saturated transistor exhibits a low collector-to-emitter resistance $R_{CE\text{sat}}$,

$$R_{CE\text{sat}} \equiv \left.\frac{\partial v_{CE}}{\partial i_C}\right|_{\substack{i_B=I_B \\ i_C=I_{C\text{sat}}}} \tag{5.43}$$

Typically, $R_{CE\text{sat}}$ ranges from a few ohms to a few tens of ohms.

Figure 5.24(b) shows one of the i_C–v_{CE} characteristic curves of the saturated transistor shown in Fig. 5.24(a). It is interesting to note that the curve intersects the v_{CE} axis at $V_T \ln(1/\alpha_R)$, a value common to all the i_C–v_{CE} curves. We have also shown in Fig. 5.24(b) the tangent at operating point X of slope $1/R_{CE\text{sat}}$. When extrapolated, the tangent intersects the v_{CE}-axis at a voltage $V_{CE\text{off}}$, typically approximately 0.1 V. It follows that the i_C–v_{CE} characteristic of a saturated transistor can be approximately represented by the equivalent circuit shown in Fig. 5.24(c). At the collector side, the transistor is represented by a resistance $R_{CE\text{sat}}$ in

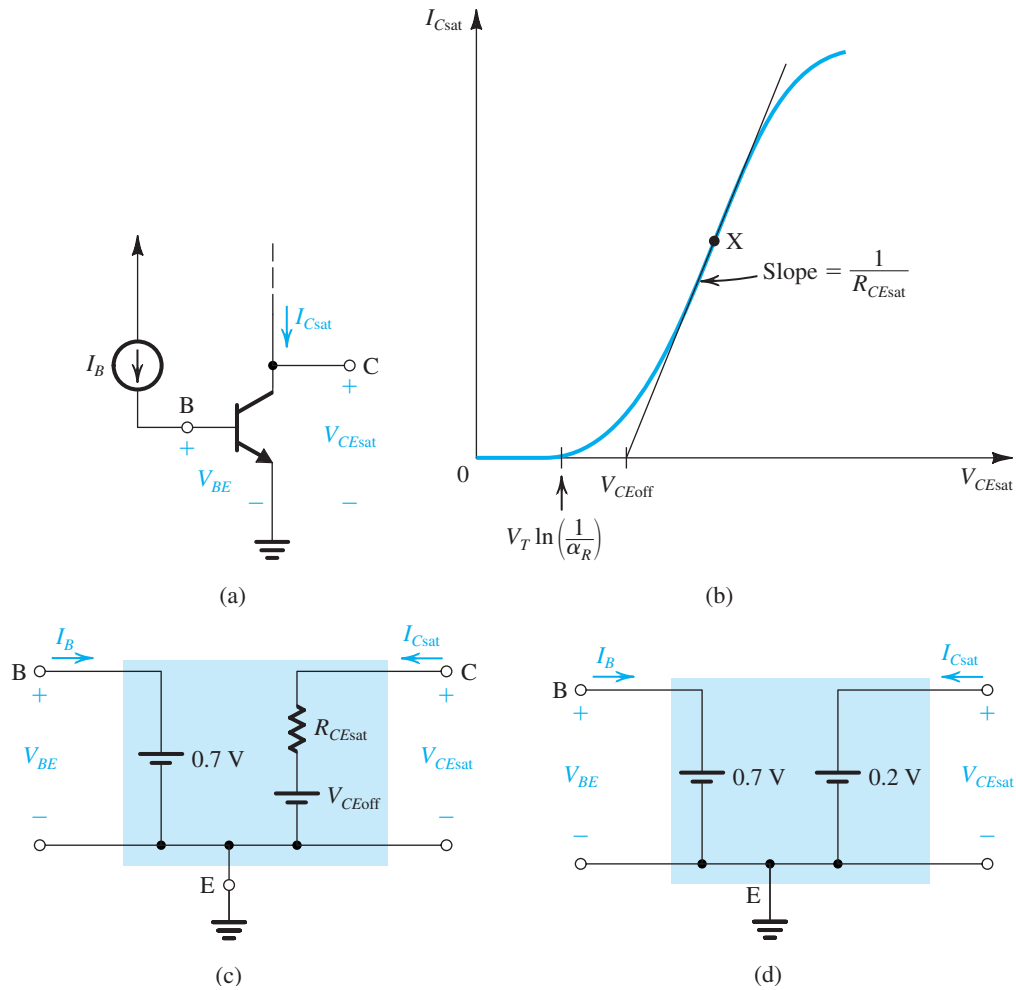


FIGURE 5.24 **(a)** An *npn* transistor operated in saturation mode with a constant base current I_B. **(b)** The i_C–v_{CE} characteristic curve corresponding to $i_B = I_B$. The curve can be approximated by a straight line of slope $1/R_{CE\text{sat}}$. **(c)** Equivalent-circuit representation of the saturated transistor. **(d)** A simplified equivalent-circuit model of the saturated transistor.

series with a battery V_{CEoff}. Thus the saturation voltage V_{CEsat} can be found from

$$V_{CEsat} = V_{CEoff} + I_{Csat}R_{CEsat} \tag{5.44}$$

Typically, V_{CEsat} falls in the range of 0.1 V to 0.3 V. For many applications the even simpler model shown in Fig. 5.24(d) suffices. The offset voltage of a saturated transistor, though small, makes the BJT less attractive as a switch than the MOSFET, whose i_D–v_{DS} characteristics go right through the origin of the i_D–v_{DS} plane.

It is interesting and instructive to use the Ebers-Moll model to derive analytical expressions for the characteristics of the saturated transistor. Toward that end we use Eqs. (5.28) and (5.27), substitute $i_B = I_B$, and neglect the small terms that do not include exponentials; thus,

$$I_B = \frac{I_S}{\beta_F} e^{v_{BE}/V_T} + \frac{I_S}{\beta_R} e^{v_{BC}/V_T} \tag{5.45}$$

$$i_C = I_S e^{v_{BE}/V_T} - \frac{I_S}{\alpha_R} e^{v_{BC}/V_T} \tag{5.46}$$

Dividing Eq. (5.46) by Eq. (5.45) and writing $v_{BE} = v_{BC} + v_{CE}$ enables us to express i_C in the form

$$i_C = (\beta_F I_B)\left(\frac{e^{v_{CE}/V_T} - \dfrac{1}{\alpha_R}}{e^{v_{CE}/V_T} + \dfrac{\beta_F}{\beta_R}}\right) \tag{5.47}$$

This is the equation of the i_C–v_{CE} characteristic curve obtained when the base is driven with a constant current I_B. Figure 5.25 shows a typical plot of the normalized collector current $i_C/(\beta_F I_B)$,

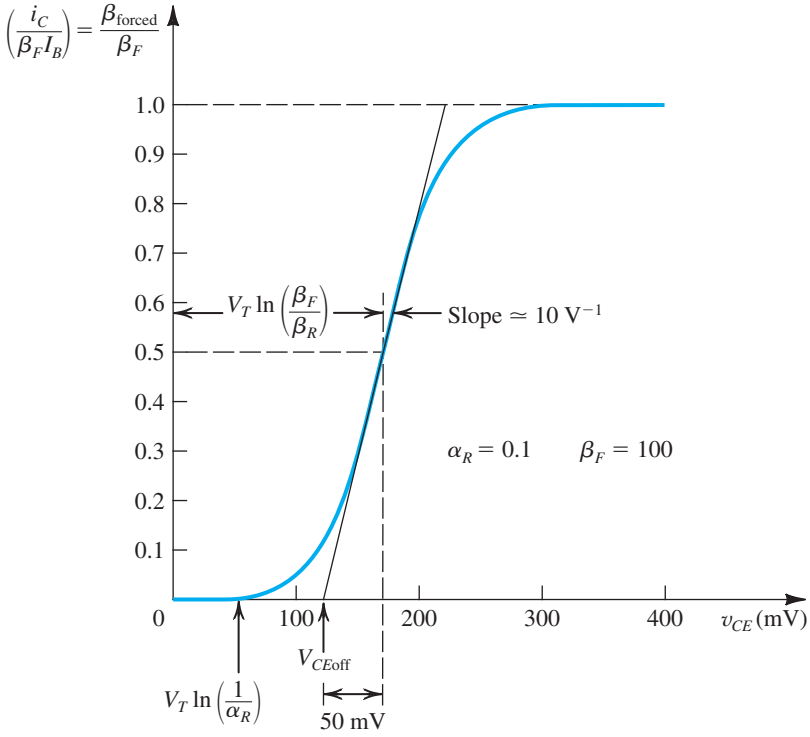


FIGURE 5.25 Plot of the normalized i_C versus v_{CE} for an *npn* transistor with $\beta_F = 100$ and $\alpha_R = 0.1$. This is a plot of Eq. (5.47), which is derived using the Ebers-Moll model.

which is equal to $(\beta_{\text{forced}}/\beta_F)$, versus v_{CE}. As shown, the curve can be approximated by a straight line coincident with the tangent at the point $\beta_{\text{forced}}/\beta_F = 0.5$. It can be shown that this tangent has a slope of approximately 10 V^{-1}, independent of the transistor parameters. Thus,

$$R_{CE\text{sat}} = 1/10\beta_F I_B \tag{5.48}$$

Other important parameters of the normalized plot are indicated in Fig. 5.25. Finally, we can obtain an expression for $V_{CE\text{sat}}$ by substituting $i_C = I_{C\text{sat}} = \beta_{\text{forced}} I_B$ and $v_{CE} = V_{CE\text{sat}}$ in Eq. (5.47),

$$V_{CE\text{sat}} = V_T \ln \frac{1 + (\beta_{\text{forced}} + 1)/\beta_R}{1 - (\beta_{\text{forced}}/\beta_F)} \tag{5.49}$$

EXERCISES

5.16 An *npn* transistor characterized by $\beta_F = 100$ and $\alpha_R = 0.1$ is operated in saturation with a constant base current of 0.1 mA and a forced β of 10. Find the values of V_{CE} at $i_C = 0$, $R_{CE\text{sat}}$, and $V_{CE\text{off}}$. Use the latter two figures to obtain an approximate value for $V_{CE\text{sat}}$ [i.e., using the equivalent circuit model of Fig. 5.24(c)]. Find a more accurate value for $V_{CE\text{sat}}$ using Eq. (5.49), and compare results. Repeat for a β_{forced} of 20.

Ans. 58 mV; 10 Ω; 120 mV; 130 mV and 118 mV; 140 mV and 137 mV

5.17 Measurements made on a BJT operated in saturation with a constant base-current drive provide the following data: at $i_C = 5$ mA, $v_{CE} = 170$ mV; at $i_C = 2$ mA, $v_{CE} = 110$ mV. What are the values of the offset voltage $V_{CE\text{off}}$ and saturation resistance $R_{CE\text{sat}}$ in this situation?

Ans. 70 mV; 20 Ω

5.2.5 Transistor Breakdown

The maximum voltages that can be applied to a BJT are limited by the EBJ and CBJ breakdown effects that follow the avalanche multiplication mechanism described in Section 3.X. Consider first the common-base configuration. The i_C–v_{CB} characteristics in Fig. 5.18(b) indicate that for $i_E = 0$ (i.e., with the emitter open-circuited) the collector–base junction breaks down at a voltage denoted by BV_{CBO}. For $i_E > 0$, breakdown occurs at voltages smaller than BV_{CBO}. Typically, BV_{CBO} is greater than 50 V.

Next consider the common-emitter characteristics of Fig. 5.21, which show breakdown occurring at a voltage BV_{CEO}. Here, although breakdown is still of the avalanche type, the effects on the characteristics are more complex than in the common-base configuration. We will not explain these details; it is sufficient to point out that typically BV_{CEO} is about half BV_{CBO}. On the transistor data sheets BV_{CEO} is sometimes referred to as the **sustaining voltage** LV_{CEO}.

Breakdown of the CBJ in either the common-base or common-emitter configuration is not destructive as long as the power dissipation in the device is kept within safe limits. This, however, is not the case with the breakdown of the emitter–base junction. The EBJ breaks down in an avalanche manner at a voltage BV_{EBO} much smaller than BV_{CBO}. Typically, BV_{EBO} is in the range of 6 V to 8 V, and the breakdown is destructive in the sense that the β of the transistor is permanently reduced. This does not prevent use of the EBJ as a zener diode to generate reference voltages in IC design. In such applications, however, one is not concerned with the β-degradation effect. A circuit arrangement to prevent EBJ breakdown in IC amplifiers will be discussed in Chapter 10. Transistor breakdown and the maximum allowable power dissipation are important parameters in the design of power amplifiers (Chapter 9).

EXERCISE

5.18 What is the output voltage of the circuit in Fig. E5.18 if the transistor $BV_{BCO} = 70$ V?

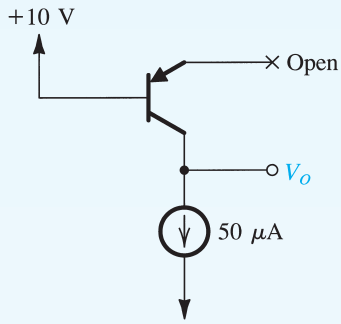


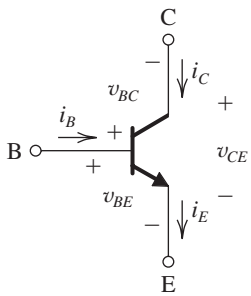
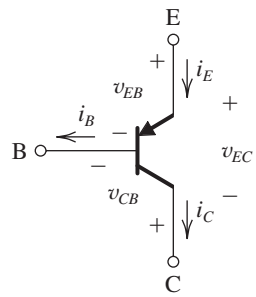
FIGURE E5.18

Ans. –60 V

5.2.6 Summary

We conclude our study of the current-voltage characteristics of the BJT with a summary of important results in Table 5.3.

TABLE 5.3 Summary of the BJT Current-Voltage Characteristics

Circuit Symbol and Directions of Current Flow	*npn* Transistor	*pnp* Transistor
		
Operation in the Active Mode (for Amplifier Application)		
Conditions:		
1. EBJ Forward Biased	$v_{BE} > V_{BEon}$; $V_{BEon} \cong 0.5$ V	$v_{EB} > V_{EBon}$; $V_{EBon} \cong 0.5$ V
	Typically, $v_{BE} = 0.7$ V	Typically, $v_{EB} = 0.7$ V
2. CBJ Reversed Biased	$v_{BC} \le V_{BCon}$; $V_{BCon} \cong 0.4$ V	$v_{CB} \le V_{CBon}$; $V_{CBon} \cong 0.4$ V
	$\Rightarrow v_{CE} \ge 0.3$ V	$\Rightarrow v_{EC} \ge 0.3$ V

(Continued)

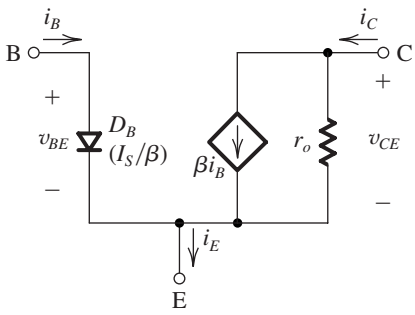
TABLE 5.3 *(Continued)*

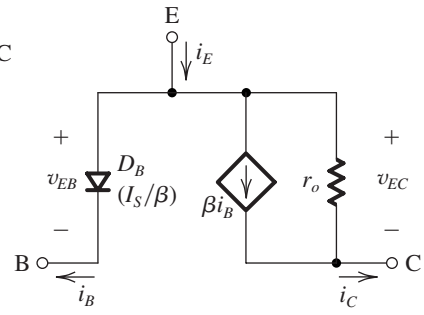
Current-Voltage Relationships

- $i_C = I_S e^{v_{BE}/V_T}$
- $i_B = i_C/\beta \quad \Leftrightarrow \quad i_C = \beta i_B$
- $i_E = i_C/\alpha \quad \Leftrightarrow \quad i_C = \alpha i_E$
- $\beta = \dfrac{\alpha}{1-\alpha} \quad \Leftrightarrow \quad \alpha = \dfrac{\beta}{\beta+1}$
- $\beta = \beta_F,\ \alpha = \alpha_F$
- I_S = Transistor scale current; proportional to EBJ area; doubles for every 5°C rise in temperature.
- V_T = Thermal voltage = $kT/q \cong 25$ mV at room temperature.
- At a constant I_E, $|V_{BE}|$ decreases by 2 mV for every 1°C rise in temperature.

- $i_C = I_S e^{v_{EB}/V_T}$

Large-Signal Equivalent-Circuit Model (Including the Early Effect)





$$i_B = \left(\frac{I_S}{\beta}\right) e^{v_{BE}/V_T}$$

$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

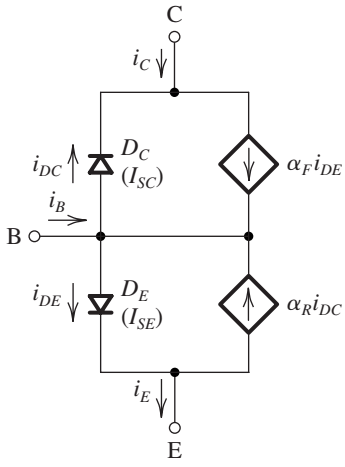
$$r_o = V_A/(I_S e^{V_{BE}/V_T})$$

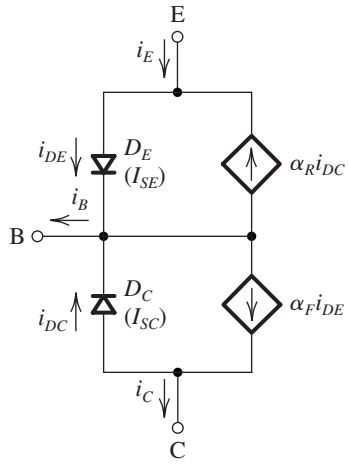
$$i_B = \left(\frac{I_S}{\beta}\right) e^{v_{EB}/V_T}$$

$$i_C = I_S e^{v_{EB}/V_T}\left(1 + \frac{v_{EC}}{|V_A|}\right)$$

$$r_o = |V_A|/(I_S e^{V_{EB}/V_T})$$

Ebers-Moll Model





$$i_{DE} = (I_{SE}e^{v_{BE}/V_T} - 1) \qquad i_{DE} = (I_{SE}e^{v_{EB}/V_T} - 1)$$

$$i_{DC} = (I_{SC}e^{v_{BC}/V_T} - 1) \qquad i_{DC} = (I_{SC}e^{v_{CB}/V_T} - 1)$$

$$\alpha_F I_{SE} = \alpha_R I_{SC} = I_S$$

$$\frac{I_{SC}}{I_{SE}} = \frac{\alpha_F}{\alpha_R} = \frac{\text{CBJ Area}}{\text{EBJ Area}}$$

Operation in the Saturation Mode

Conditions:

1. EBJ Forward-Biased

$v_{BE} > V_{BEon}$; $V_{BEon} \cong 0.5$ V — $v_{EB} > V_{EBon}$; $V_{EBon} \cong 0.5$ V

Typically, $v_{BE} = 0.7$–0.8 V — Typically, $v_{EB} = 0.7$–0.8 V

2. CBJ Forward-Biased

$v_{BC} \geq V_{BCon}$; $V_{BCon} \cong 0.4$ V — $v_{CB} \geq V_{CBon}$; $V_{CBon} \cong 0.4$ V

Typically, $v_{BC} = 0.5$–0.6 V — Typically, $v_{CB} = 0.5$–0.6 V

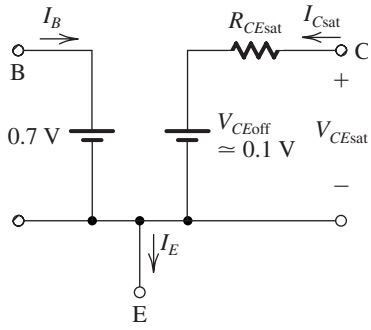
$\Rightarrow v_{CE} = V_{CEsat} = 0.1$–$0.2$ V — $\Rightarrow v_{EC} = V_{ECsat} = 0.1$–$0.2$ V

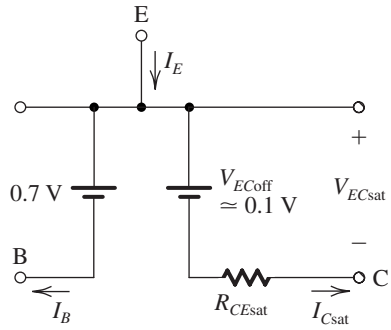
Currents

$$I_{Csat} = \beta_{forced} I_B$$

$$\beta_{forced} \leq \beta_F, \quad \frac{\beta_F}{\beta_{forced}} = \text{Overdrive factor}$$

Equivalent Circuits





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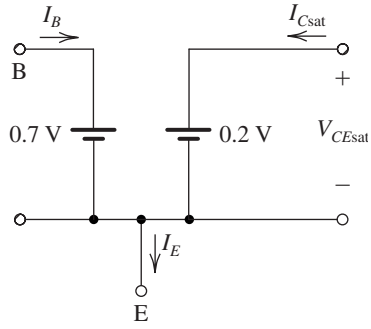
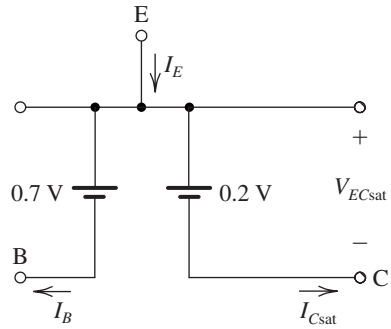


Or approximately:



$$|V_{CEsat}| = V_T \ln\left[\frac{1 + (\beta_{forced} + 1)/\beta_F}{1 - \beta_{forced}/\beta_F}\right]$$

For $\beta_{forced} = \beta_F/2$: $\quad R_{CEsat} = 1/10\beta_F I_B$

5.3 THE BJT AS AN AMPLIFIER AND AS A SWITCH

Having studied the terminal characteristics of the BJT, we are now ready to consider its two major areas of application: as a signal amplifier,[6] and as a digital-circuit switch. The basis for the amplifier application is that when the BJT is operated in the active mode, it acts as a voltage-controlled current source: Changes in the base–emitter voltage v_{BE} give rise to changes in the collector current i_C. Thus in the active mode the BJT can be used to implement a transconductance amplifier (see Section 1.5). Voltage amplification can be obtained simply by passing the collector current through a resistance R_C, as will be seen shortly.

Since we are particularly interested in linear amplification, we will have to devise a way to achieve it in the face of the highly nonlinear behavior of the transistor, namely, that the collector current i_C is exponentially related to v_{BE}. We will use the approach described in general terms in Section 1.4. Specifically, we will **bias** the transistor to operate at a dc base–emitter voltage V_{BE} and a corresponding dc collector current I_C. Then we will superimpose the signal to be amplified, v_{be}, on the dc voltage V_{BE}. By keeping the amplitude of the signal v_{be} small, we will be able to constrain the transistor to operate on a short, almost linear segment of the i_C–v_{BE} characteristic; thus, the change in collector current, i_c, will be linearly related to v_{be}. We will study the small-signal operation of the BJT later in this section and in greater detail in Section 5.5. First, however, we will look at the "big picture": We will study the total or large-signal operation of a BJT amplifier. From the transfer characteristic of the circuit, we will be able to see clearly the region over which the circuit can be operated as a linear amplifier. We also will be able to see how the BJT can be employed as a switch.

5.3.1 Large-Signal Operation—The Transfer Characteristic

Figure 5.26(a) shows the basic structure (skeleton) of the most commonly used BJT amplifier, the **grounded-emitter** or **common-emitter (CE)** circuit. The total input voltage v_I (bias + signal) is applied between base and emitter; that is, $v_{BE} = v_I$. The total output voltage v_O (bias + signal) is taken between collector and ground; that is, $v_O = v_{CE}$. Resistor R_C has two functions: to establish a desired dc bias voltage at the collector, and to convert the collector signal current i_c to an output voltage, v_{ce} or v_o. The supply voltage V_{CC} is needed to bias the BJT as well as to supply the power needed for the operation of the amplifier.

Figure 5.26(b) shows the voltage transfer characteristic of the CE circuit of Fig. 5.26(a). To understand how this characteristic arises, we first express v_O as

$$v_O = v_{CE} = V_{CC} - R_C i_C \tag{5.50}$$

Next, we observe that since $v_{BE} = v_I$, the transistor will be effectively cutoff for $v_I < 0.5$ V or so. Thus, for the range $0 < v_I < 0.5$ V, i_C will be negligibly small, and v_O will be equal to the supply voltage V_{CC} (segment XY of the transfer curve).

As v_I is increased above 0.5 V, the transistor begins to conduct, and i_C increases. From Eq. (5.50), we see that v_O decreases. However, since initially v_O will be large, the BJT will

[6] An introduction to amplifiers from an external-terminals point of view was presented in Sections 1.4 and 1.5, and it would be helpful for readers who are not familiar with basic amplifier concepts to review this material before proceeding with the study of BJT amplifiers.

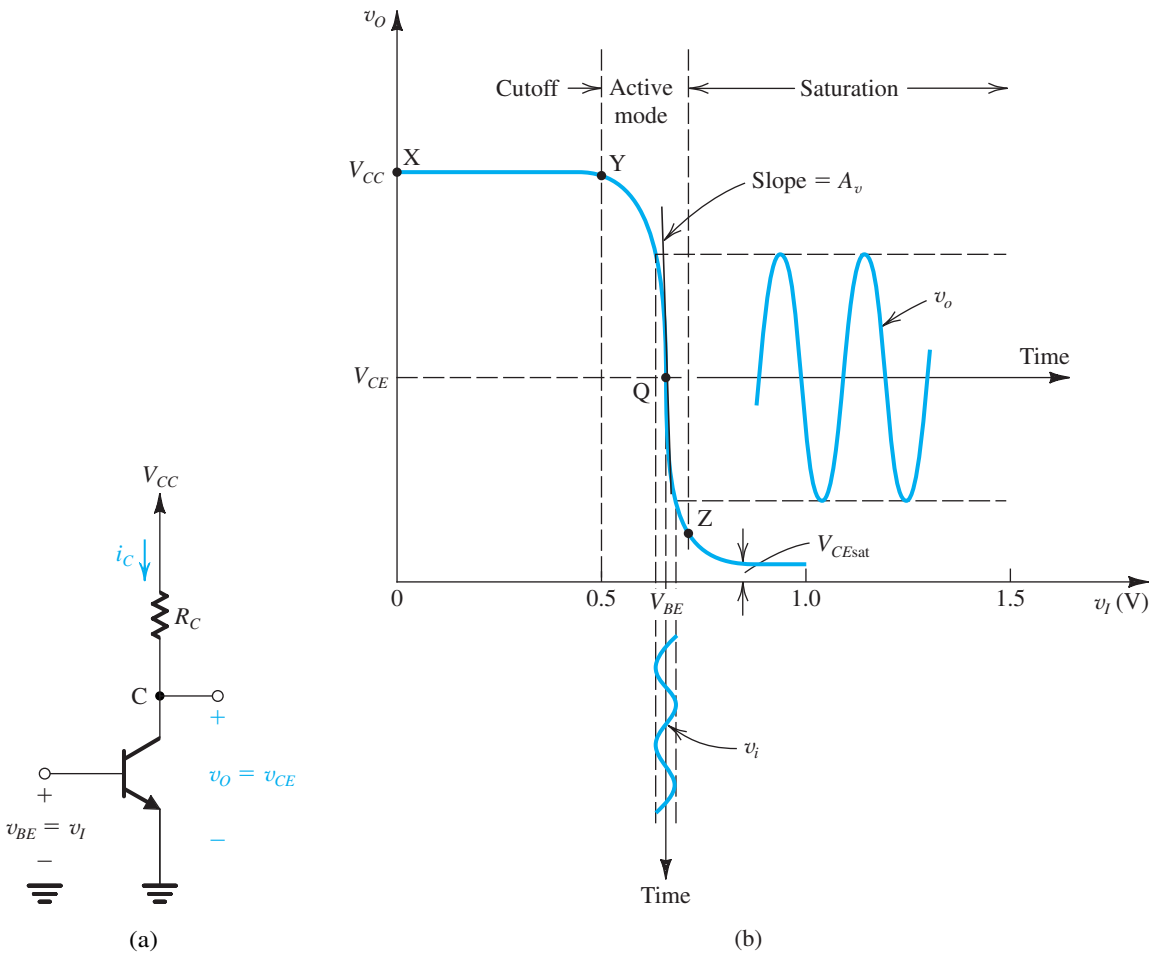


FIGURE 5.26 **(a)** Basic common-emitter amplifier circuit. **(b)** Transfer characteristic of the circuit in (a). The amplifier is biased at a point Q, and a small voltage signal v_i is superimposed on the dc bias voltage V_{BE}. The resulting output signal v_o appears superimposed on the dc collector voltage V_{CE}. The amplitude of v_o is larger than that of v_i by the voltage gain A_v.

be operating in the active mode, which gives rise to the sharply descending segment YZ of the voltage transfer curve. The equation for this segment can be obtained by substituting in Eq. (5.50) the active-mode expression for i_C, namely,

$$i_C \cong I_S e^{v_{BE}/V_T}$$
$$= I_S e^{v_I/V_T}$$

where we have, for simplicity, neglected the Early effect. Thus we obtain

$$v_O = V_{CC} - R_C I_S e^{v_I/V_T} \tag{5.51}$$

We observe that the exponential term in this equation gives rise to the steep slope of the YZ segment of the transfer curve. Active-mode operation ends when the collector voltage (v_O or v_{CE})

falls by 0.4 V or so below that of the base (v_I or v_{BE}). At this point, the CBJ turns on, and the transistor enters the saturation region. This is indicated by point Z on the transfer curve. Observe that further increases in v_{BE} cause v_{CE} to decrease only slightly: In the saturation region, $v_{CE} = V_{CEsat}$, which falls in the narrow range of 0.1 V to 0.2 V. It is the almost-constant V_{CEsat} that gives this region of BJT operation the name *saturation*. The collector current will also remain nearly constant at the value I_{Csat},

$$I_{Csat} = \frac{V_{CC} - V_{CEsat}}{R_C} \tag{5.52}$$

We recall from our study of the saturation region of operation in the previous section that the saturated BJT exhibit a very small resistance R_{CEsat} between its collector and emitter. Thus, when saturated, the transistor in Fig. 5.26 provides a low-resistance path between the collector node C and ground and hence can be thought of as a closed switch. On the other hand, when the BJT is cutoff, it conducts negligibly small (ideally zero) current and thus acts as an open switch, effectively disconnecting node C from ground. The status of the switch (i.e., open or closed) is determined by the value of the control voltage v_{BE}. Very shortly, we will show that the BJT switch can also be controlled by the base current.

5.3.2 Amplifier Gain

To operate the BJT as a linear amplifier, it must be biased at a point in the active region. Figure 5.26(b) shows such a bias point, labeled Q (for **quiescent point**), and characterized by a dc base–emitter voltage V_{BE} and a dc collector–emitter voltage V_{CE}. If the collector current at this value of V_{BE} is denoted I_C, that is,

$$I_C = I_S e^{V_{BE}/V_T} \tag{5.53}$$

then from the circuit in Fig. 5.26(a) we can write

$$V_{CE} = V_{CC} - R_C I_C \tag{5.54}$$

Now, if the signal to be amplified, v_i, is superimposed on V_{BE} and kept sufficiently small, as indicated in Fig. 5.26(b), the instantaneous operating point will be constrained to a relatively short, almost-linear segment of the transfer curve around the bias point Q. The slope of this linear segment will be equal to the slope of the tangent to the transfer curve at Q. This slope is the voltage gain of the amplifier for small-input signals around Q. An expression for the small-signal gain A_v can be found by differentiating the expression in Eq. (5.51) and evaluating the derivative at point Q; that is, for $v_I = V_{BE}$,

$$A_v \equiv \left.\frac{dv_O}{dv_I}\right|_{v_I = V_{BE}} \tag{5.55}$$

Thus,

$$A_v = -\frac{1}{V_T} I_S e^{V_{BE}/V_T} R_C$$

Now, using Eq. (5.53) we can express A_v in compact form:

$$A_v = -\frac{I_C R_C}{V_T} = -\frac{V_{RC}}{V_T} \tag{5.56}$$

where V_{RC} is the dc voltage drop across R_C,

$$V_{RC} = V_{CC} - V_{CE} \tag{5.57}$$

Observe that the CE amplifier is inverting; that is, the output signal is 180° out of phase relative to the input signal. The simple expression in Eq. (5.56) indicates that the voltage gain of the common-emitter amplifier is the ratio of the dc voltage drop across R_C to the thermal voltage V_T (≅ 25 mV at room temperature). It follows that to maximize the voltage gain we should use as large a voltage drop across R_C as possible. For a given value of V_{CC}, Eq. (5.57) indicates that to increase V_{RC} we have to operate at a lower V_{CE}. However, reference to Fig. 5.26(b) shows that a lower V_{CE} means a bias point Q close to the end of the active-region segment, which might not leave sufficient room for the negative-output signal swing without the amplifier entering the saturation region. If this happens, the negative peaks of the waveform of v_o will be clipped off. Indeed, it is the need to allow sufficient room for output signal swing that determines the placement of the bias point Q on the active-region segment, YZ, of the transfer curve. Placing Q too high on this segment not only results in reduced gain (because V_{RC} is lower) but could possibly limit the allowable range of positive signal swing. At this end, the limitation is imposed by the BJT cutting off, in which event the positive-output peaks would be clipped off at a level equal to V_{CC}. Finally, it is useful to note that the theoretical maximum gain A_v is obtained by biasing the BJT at the edge of saturation, which of course would not leave any room for negative signal swing. The resulting gain is given by

$$A_v = -\frac{V_{CC} - V_{CEsat}}{V_T} \tag{5.58}$$

Thus,

$$A_{v\max} \cong -\frac{V_{CC}}{V_T} \tag{5.59}$$

Although the gain can be increased by using a larger supply voltage, other considerations come into play when determining an appropriate value for V_{CC}. In fact, the trend has been toward using lower and lower supply voltages, currently approaching 1 V or so. At such low supply voltages, large gain values can be obtained by replacing the resistance R_C with a constant-current source, as will be seen in Chapter 6.

EXAMPLE 5.2

Consider a common-emitter circuit with a BJT having $I_S = 10^{-15}$ A, a collector resistance $R_C = 6.8$ kΩ, and a power supply $V_{CC} = 10$ V.

(a) Determine the value of the bias voltage V_{BE} required to operate the transistor at $V_{CE} = 3.2$ V. What is the corresponding value of I_C?

(b) Find the voltage gain A_v at this bias point. If an input sine-wave signal of 5-mV peak amplitude is superimposed on V_{BE}, find the amplitude of the output sine-wave signal (assume linear operation).

(c) Find the positive increment in v_{BE} (above V_{BE}) that drives the transistor to the edge of saturation with $v_{CE} = 0.3$ V.

(d) Find the negative increment in v_{BE} that drives the transistor to within 1% of cutoff (i.e., $v_O = 0.99V_{CC}$).

Solution

(a)

$$I_C = \frac{V_{CC} - V_{CE}}{R_C}$$
$$= \frac{10 - 3.2}{6.8} = 1 \text{ mA}$$

The value of V_{BE} can be determined from

$$1 \times 10^{-3} = 10^{-15} e^{V_{BE}/V_T}$$

which results in

$$V_{BE} = 690.8 \text{ mV}$$

(b)

$$A_v = -\frac{V_{CC} - V_{CE}}{V_T}$$
$$= -\frac{10 - 3.2}{0.025} = -272 \text{ V/V}$$
$$\hat{V}_o = 272 \times 0.005 = 1.36 \text{ V}$$

(c) For $v_{CE} = 0.3$ V,

$$i_C = \frac{10 - 0.3}{6.8} = 1.617 \text{ mA}$$

To increase i_C from 1 mA to 1.617 mA, v_{BE} must be increased by

$$\Delta v_{BE} = V_T \ln\left(\frac{1.617}{1}\right)$$
$$= 12 \text{ mV}$$

(d) For $v_O = 0.99V_{CC} = 9.9$ V,

$$i_C = \frac{10 - 9.9}{6.8} = 0.0147 \text{ mA}$$

To decrease i_C from 1 mA to 0.0147 mA, v_{BE} must change by

$$\Delta v_{BE} = V_T \ln\left(\frac{0.0147}{1}\right)$$
$$= -105.5 \text{ mV}$$

EXERCISE

5.19 While keeping I_C unchanged at 1 mA, find the value of R_C that will result in a voltage gain of −320 V/V. What is the largest negative signal swing allowed at the output (assume that v_{CE} is not to decrease below 0.3 V)? What approximately is the corresponding input signal amplitude? (Assume linear operation).

Ans. 8 kΩ; 1.7 V; 5.3 mV

5.3.3 Graphical Analysis

Although formal graphical methods are of little practical value in the analysis and design of most transistor circuits, it is illustrative to portray graphically the operation of a simple transistor amplifier circuit. Consider the circuit of Fig. 5.27, which is similar to the circuit we have been studying except for an added resistance in the base lead, R_B. A graphical analysis of the operation of this circuit can be performed as follows: First, we have to determine the dc bias point. Toward that end we set $v_i = 0$ and use the technique illustrated in Fig. 5.28 to determine the dc base current I_B. We next move to the i_C–v_{CE} characteristics, shown in Fig. 5.29. We know that the operating point will lie on the i_C–v_{CE} curve corresponding to

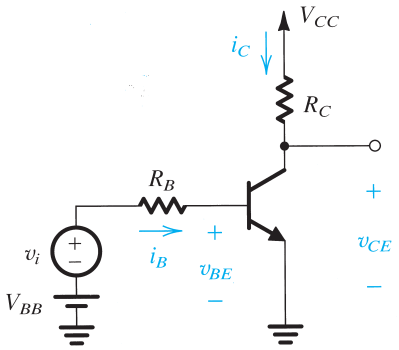


FIGURE 5.27 Circuit whose operation is to be analyzed graphically.

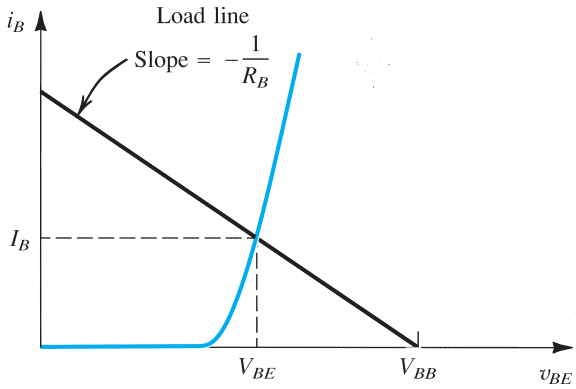


FIGURE 5.28 Graphical construction for the determination of the dc base current in the circuit of Fig. 5.27.

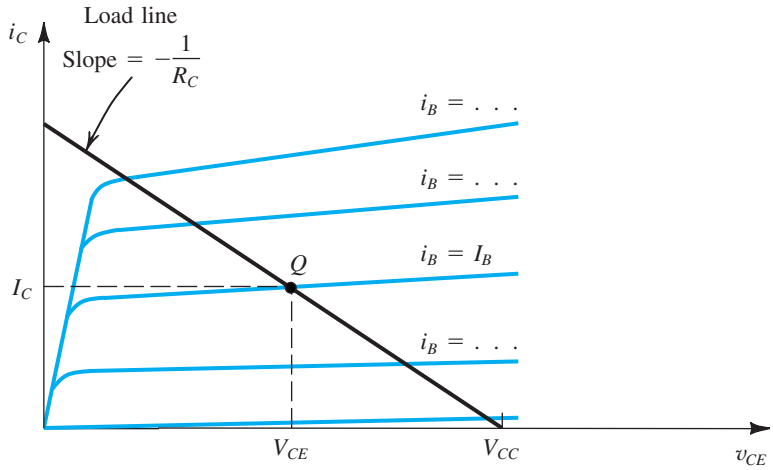


FIGURE 5.29 Graphical construction for determining the dc collector current I_C and the collector-to-emitter voltage V_{CE} in the circuit of Fig. 5.27.

the value of base current we have determined (the curve for $i_B = I_B$). Where it lies on the curve will be determined by the collector circuit. Specifically, the collector circuit imposes the constraint

$$v_{CE} = V_{CC} - i_C R_C$$

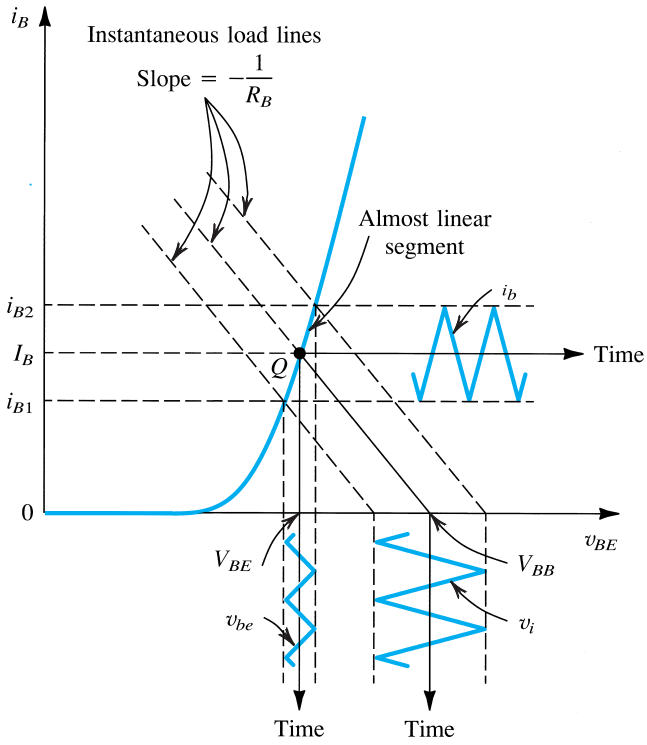
which can be rewritten as

$$i_C = \frac{V_{CC}}{R_C} - \frac{1}{R_C} v_{CE}$$

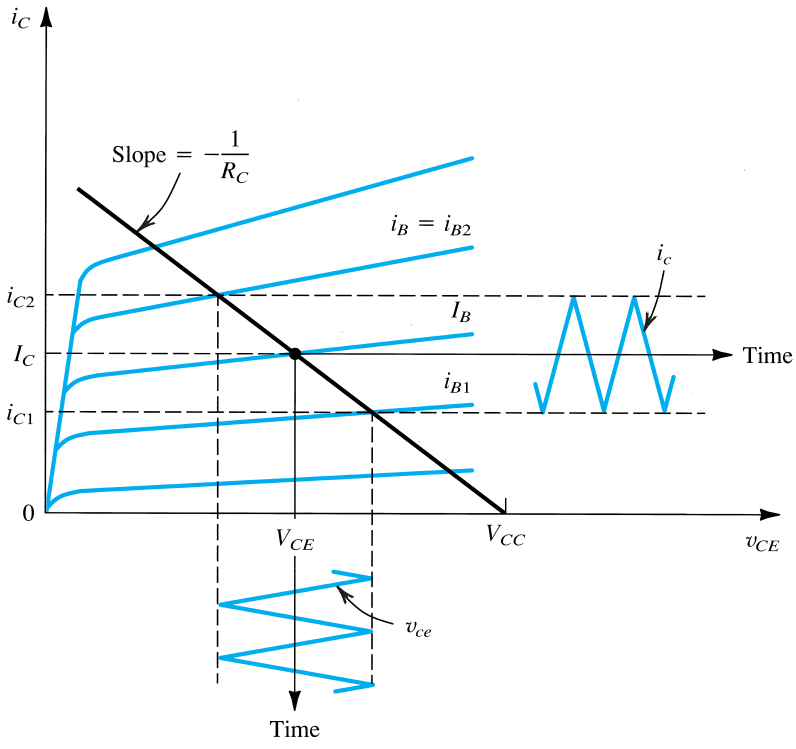
which represents a linear relationship between v_{CE} and i_C. This relationship can be represented by a straight line, as shown in Fig. 5.29. Since R_C can be considered the amplifier load, the straight line of slope $-1/R_C$ is known as the load line.[7] The dc bias point, or quiescent point, Q will be at the intersection of the load line and the i_C–v_{CE} curve corresponding to the base current I_B. The coordinates of point Q give the dc collector current I_C and the dc collector-to-emitter voltage V_{CE}. Observe that for amplifier operation, Q should be in the active region and furthermore should be located so as to allow for a reasonable signal swing as the input signal v_i is applied. This will become clearer shortly.

The situation when v_i is applied is illustrated in Fig. 5.30. Consider first Fig. 5.30(a), which shows a signal v_i having a triangular waveform being superimposed on the dc voltage V_{BB}. Corresponding to each instantaneous value of $V_{BB} + v_i(t)$, one can draw a straight line with slope $-1/R_B$. Such an "instantaneous load line" intersects the i_B–v_{BE} curve at a point whose coordinates give the total instantaneous values of i_B and v_{BE} corresponding to the particular value of $V_{BB} + v_i(t)$. As an example, Fig. 5.30(a) shows the straight lines corresponding to $v_i = 0$, v_i at its positive peak, and v_i at its negative peak. Now, if the amplitude of v_i is sufficiently small so that the instantaneous operating point is confined to an almost-linear segment of the i_B–v_{BE} curve, then the resulting signals i_b and v_{be} will be triangular in waveform, as indicated in the figure. This, of course, is the small-signal approximation. In summary,

[7] The term *load line* is also employed for the straight line in Fig. 5.28.



(a)



(b)

FIGURE 5.30 Graphical determination of the signal components v_{be}, i_b, i_c, and v_{ce} when a signal component v_i is superimposed on the dc voltage V_{BB} (see Fig. 5.27).

the graphical construction in Fig. 5.30(a) can be used to determine the total instantaneous value of i_B corresponding to each value of v_i.

Next, we move to the i_C–v_{CE} characteristics of Fig. 5.30(b). The operating point will move along the load line of slope $-1/R_C$ as i_B goes through the instantaneous values determined from Fig. 5.30(a). For example, when v_i is at its positive peak, $i_B = i_{B2}$ (from Fig. 5.30(a)), and the instantaneous operating point in the i_C–v_{CE} plane will be at the intersection of the load line and the curve corresponding to $i_B = i_{B2}$. In this way, one can determine the waveforms of i_C and v_{CE} and hence of the signal components i_c and v_{ce}, as indicated in Fig. 5.30(b).

Effects of Bias-Point Location on Allowable Signal Swing The location of the dc bias point in the i_C–v_{CE} plane significantly affects the maximum allowable signal swing at the collector. Refer to Fig. 5.30(b) and observe that the positive peaks of v_{ce} cannot go beyond V_{CC}, otherwise the transistor enters the cutoff region. Similarly, the negative peaks of v_{ce} cannot extend below a few tenths of a volt (usually, 0.3 V), otherwise the transistor enters the saturation region. The location of the bias point in Fig. 5.30(b) allows for an approximately equal swing in each direction.

Next consider Fig. 5.31. Here we show load lines corresponding to two values of R_C. Line A corresponds to a low value of R_C and results in the operating point Q_A, where the value of V_{CE} is very close to V_{CC}. Thus the positive swing of v_{ce} will be severely limited; in this situation, it is said that there isn't sufficient "head room." On the other hand, line B, which corresponds to a large R_C, results in the bias point Q_B, whose V_{CE} is too low. Thus for line B, although there is ample room for the positive excursion of v_{ce} (there is a lot of head room), the negative signal swing is severely limited by the proximity to the saturation region (there is not sufficient "leg room"). A compromise between these two situations is obviously called for.

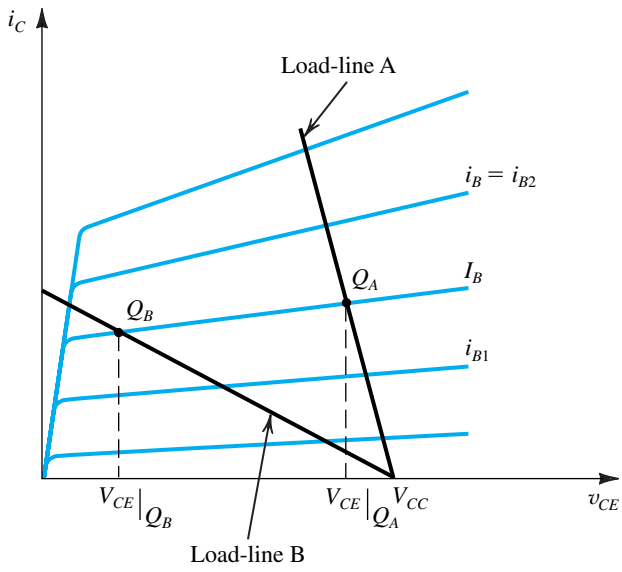


FIGURE 5.31 Effect of bias-point location on allowable signal swing: Load-line A results in bias point Q_A with a corresponding V_{CE} which is too close to V_{CC} and thus limits the positive swing of v_{CE}. At the other extreme, load-line B results in an operating point too close to the saturation region, thus limiting the negative swing of v_{CE}.

EXERCISE

5.20 Consider the circuit of Fig. 5.27 with $V_{BB} = 1.7$ V, $R_B = 100$ kΩ, $V_{CC} = 10$ V, and $R_C = 5$ kΩ. Let the transistor $\beta = 100$. The input signal v_i is a triangular wave of 0.4 V peak-to-peak. Refer to Fig. 5.30, and use the geometry of the graphical construction shown there to answer the following questions: (a) If $V_{BE} = 0.7$ V, find I_B. (b) Assuming operation on a straight line segment of the exponential i_B–v_{BE} curve, show that the inverse of its slope is V_T/I_B, and compute its value. (c) Find approximate values for the peak-to-peak amplitude of i_b and of v_{be}. (d) Assuming the i_C–v_{CE} curves to be horizontal (i.e., ignoring the Early effect), find I_C and V_{CE}. (e) Find the peak-to-peak amplitude of i_c and of v_{ce}. (f) What is the voltage gain of this amplifier?

Ans. (a) 10 μA; (b) 2.5 kΩ; (c) 4 μA, 10 mV; (d) 1 mA, 5 V; (e) 0.4 mA, 2 V; (f) –5 V/V

5.3.4 Operation as a Switch

To operate the BJT as a switch, we utilize the cutoff and the saturation modes of operation. To illustrate, consider once more the common-emitter circuit shown in Fig. 5.32 as the input v_I is varied. For v_I less than about 0.5 V, the transistor will be cutoff; thus $i_B = 0$, $i_C = 0$, and $v_C = V_{CC}$. In this state, node C is disconnected from ground; the switch is in the open position.

To turn the transistor on, we have to increase v_I above 0.5 V. In fact, for appreciable currents to flow, v_{BE} should be about 0.7 V and v_I should be higher. The base current will be

$$i_B = \frac{v_I - V_{BE}}{R_B} \tag{5.60}$$

and the collector current will be

$$i_C = \beta i_B \tag{5.61}$$

which applies only when the device is in the active mode. This will be the case as long as the CBJ is not forward biased, that is, as long as $v_C > v_B - 0.4$ V, where v_C is given by

$$v_C = V_{CC} - R_C i_C \tag{5.62}$$

Obviously, as v_I is increased, i_B will increase (Eq. 5.60), i_C will correspondingly increase (Eq. 5.61), and v_C will decrease (Eq. 5.62). Eventually, v_C will become lower than v_B by 0.4 V, at which point the transistor leaves the active region and enters the saturation region. This

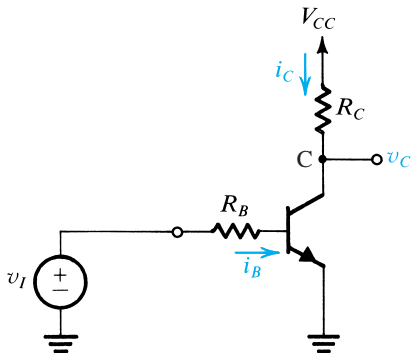


FIGURE 5.32 A simple circuit used to illustrate the different modes of operation of the BJT.

edge-of-saturation (EOS) point is defined by

$$I_{C(\text{EOS})} = \frac{V_{CC} - 0.3}{R_C} \tag{5.63}$$

where we have assumed that V_{BE} is approximately 0.7 V, and

$$I_{B(\text{EOS})} = \frac{I_{C(\text{EOS})}}{\beta} \tag{5.64}$$

The corresponding value of v_I required to drive the transistor to the edge-of-saturation can be found from

$$V_{I(\text{EOS})} = I_{B(\text{EOS})}R_B + V_{BE} \tag{5.65}$$

Increasing v_I above $V_{I(\text{EOS})}$ increases the base current, which drives the transistor deeper into saturation. The collector-to-emitter voltage, however, decreases only slightly. As a reasonable approximation, we shall usually assume that for a saturated transistor, $V_{CE\text{sat}} \cong 0.2$ V. The collector current then remains nearly constant at $I_{C\text{sat}}$,

$$I_{C\text{sat}} = \frac{V_{CC} - V_{CE\text{sat}}}{R_C} \tag{5.66}$$

Forcing more current in the base has very little effect on $I_{C\text{sat}}$ and $V_{CE\text{sat}}$. In this state the switch is closed, with a low closure resistance $R_{CE\text{sat}}$ and a small offset voltage $V_{CE\text{off}}$ (see Fig. 5.24c).

Finally, recall that in saturation one can force the transistor to operate at any desired β below the normal value; that is, the ratio of the collector current $I_{C\text{sat}}$ to the base current can be set at will and is therefore called the forced β,

$$\beta_{\text{forced}} \equiv \frac{I_{C\text{sat}}}{I_B} \tag{5.67}$$

Also recall that the ratio of I_B to $I_{B(\text{EOS})}$ is known as the overdrive factor.

EXAMPLE 5.3

The transistor in Fig. 5.33 is specified to have β in the range of 50 to 150. Find the value of R_B that results in saturation with an overdrive factor of at least 10.

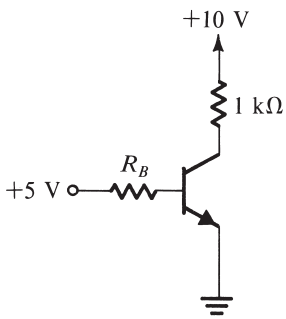


FIGURE 5.33 Circuit for Example 5.3.

Solution

When the transistor is saturated, the collector voltage will be

$$V_C = V_{CE\text{sat}} \simeq 0.2 \text{ V}$$

Thus the collector current is given by

$$I_{C\text{sat}} = \frac{+10 - 0.2}{1} = 9.8 \text{ mA}$$

To saturate the transistor with the lowest β, we need to provide a base current of at least

$$I_{B(\text{EOS})} = \frac{I_{C\text{sat}}}{\beta_{\min}} = \frac{9.8}{50} = 0.196 \text{ mA}$$

For an overdrive factor of 10, the base current should be

$$I_B = 10 \times 0.196 = 1.96 \text{ mA}$$

Thus we require a value of R_B such that

$$\frac{+5 - 0.7}{R_B} = 1.96$$

$$R_B = \frac{4.3}{1.94} = 2.2 \text{ k}\Omega$$

EXERCISE

5.21 Consider the circuit in Fig. 5.32 for the case $V_{CC} = +5$ V, $v_I = +5$ V, $R_B = R_C = 1$ kΩ, and $\beta = 100$. Calculate the base current, the collector current, and the collector voltage. If the transistor is saturated, find β_{forced}. What should R_B be raised to bring the transistor to the edge of saturation?

Ans. 4.3 mA; 4.8 mA; 0.2 V; 1.1; 91.5 kΩ

5.4 BJT CIRCUITS AT DC

We are now ready to consider the analysis of BJT circuits to which only dc voltages are applied. In the following examples we will use the simple model in which, $|V_{BE}|$ of a conducting transistor is 0.7 V and $|V_{CE}|$ of a saturated transistor is 0.2 V, and we will neglect the Early effect. Better models can, of course, be used to obtain more accurate results. This, however, is usually achieved at the expense of speed of analysis, and more importantly, it could impede the circuit designer's ability to gain insight regarding circuit behavior. Accurate results using elaborate models can be obtained using circuit simulation with SPICE, as we shall see in Section 5.11. This is almost always done in the final stages of a design and certainly before circuit fabrication. Computer simulation, however, is not a substitute for quick pencil-and-paper circuit analysis, an essential ability that aspiring circuit designers must muster. The following series of examples is a step in that direction.

As will be seen, in analyzing a circuit the first question that one must answer is: In which mode is the transistor operating? In some cases, the answer will be obvious. In many cases, however, it will not. Needless to say, as the reader gains practice and experience in transistor circuit analysis and design, the answer will be obvious in a much larger proportion of problems. The answer, however, can always be determined by utilizing the following procedure:

Assume that the transistor is operating in the active mode, and proceed to determine the various voltages and currents. Then check for consistency of the results with the assumption of active-mode operation; that is, is v_{CB} of an *npn* transistor greater than –0.4 V (or v_{CB} of a *pnp* transistor lower than 0.4 V)? If the answer is yes, then our task is complete. If the answer

is no, assume saturation-mode operation, and proceed to determine currents and voltages and to check for consistency of the results with the assumption of saturation-mode operation. Here the test is usually to compute the ratio I_C/I_B and to verify that it is lower than the transistor β; i.e., $\beta_{\text{forced}} < \beta$. Since β for a given transistor varies over a wide range, one should use the lowest specified β for this test. Finally, note that the order of these two assumptions can be reversed.

EXAMPLE 5.4

Consider the circuit shown in Fig. 5.34(a), which is redrawn in Fig. 5.34(b) to remind the reader of the convention employed throughout this book for indicating connections to dc sources. We wish to analyze this circuit to determine all node voltages and branch currents. We will assume that β is specified to be 100.

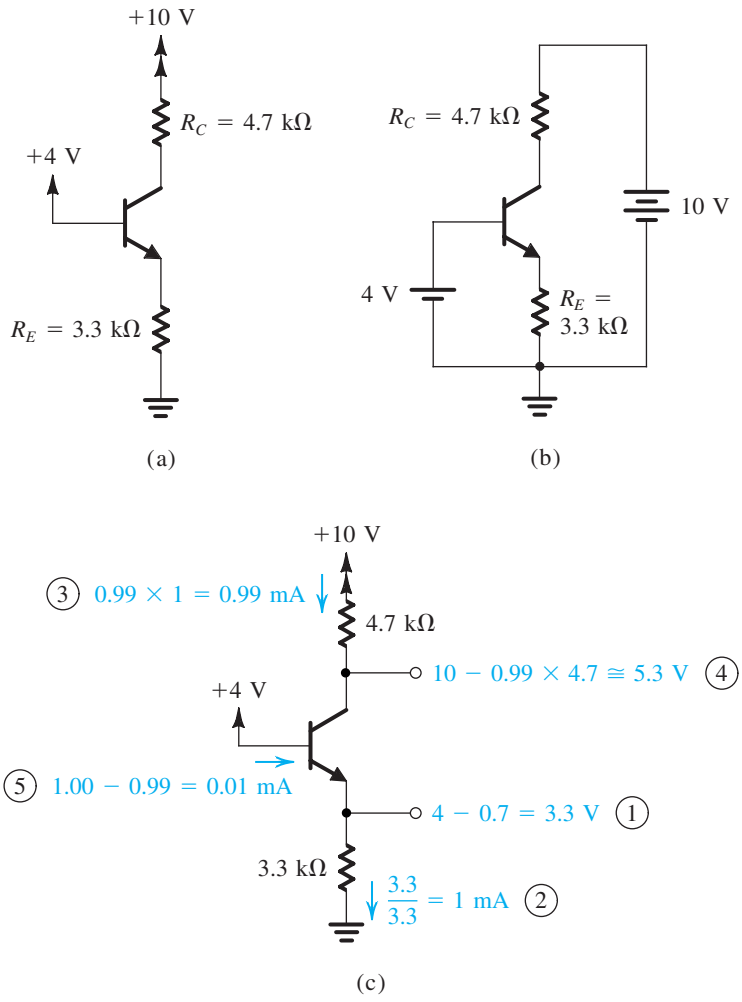


FIGURE 5.34 Analysis of the circuit for Example 5.4: **(a)** circuit; **(b)** circuit redrawn to remind the reader of the convention used in this book to show connections to the power supply; **(c)** analysis with the steps numbered.

Solution

Glancing at the circuit in Fig. 5.34(a), we note that the base is connected to +4 V and the emitter is connected to ground through a resistance R_E. It therefore is safe to conclude that the base–emitter junction will be forward biased. Assuming that this is the case and assuming that V_{BE} is approximately 0.7 V, it follows that the emitter voltage will be

$$V_E = 4 - V_{BE} \simeq 4 - 0.7 = 3.3 \text{ V}$$

We are now in an opportune position; we know the voltages at the two ends of R_E and thus can determine the current I_E through it,

$$I_E = \frac{V_E - 0}{R_E} = \frac{3.3}{3.3} = 1 \text{ mA}$$

Since the collector is connected through R_C to the +10-V power supply, it appears possible that the collector voltage will be higher than the base voltage, which is essential for active-mode operation. Assuming that this is the case, we can evaluate the collector current from

$$I_C = \alpha I_E$$

The value of α is obtained from

$$\alpha = \frac{\beta}{\beta + 1} = \frac{100}{101} \simeq 0.99$$

Thus I_C will be given by

$$I_C = 0.99 \times 1 = 0.99 \text{ mA}$$

We are now in a position to use Ohm's law to determine the collector voltage V_C,

$$V_C = 10 - I_C R_C = 10 - 0.99 \times 4.7 \simeq +5.3 \text{ V}$$

Since the base is at +4 V, the collector–base junction is reverse biased by 1.3 V, and the transistor is indeed in the active mode as assumed.

It remains only to determine the base current I_B, as follows:

$$I_B = \frac{I_E}{\beta + 1} = \frac{1}{101} \simeq 0.01 \text{ mA}$$

Before leaving this example we wish to emphasize strongly the value of carrying out the analysis directly on the circuit diagram. Only in this way will one be able to analyze complex circuits in a reasonable length of time. Figure 5.34(c) illustrates the above analysis on the circuit diagram, with the order of the analysis steps indicated by the circled numbers.

EXAMPLE 5.5

We wish to analyze the circuit of Fig. 5.35(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that of Fig. 5.34 except that the voltage at the base is now +6 V. Assume that the transistor β is specified to be *at least* 50.

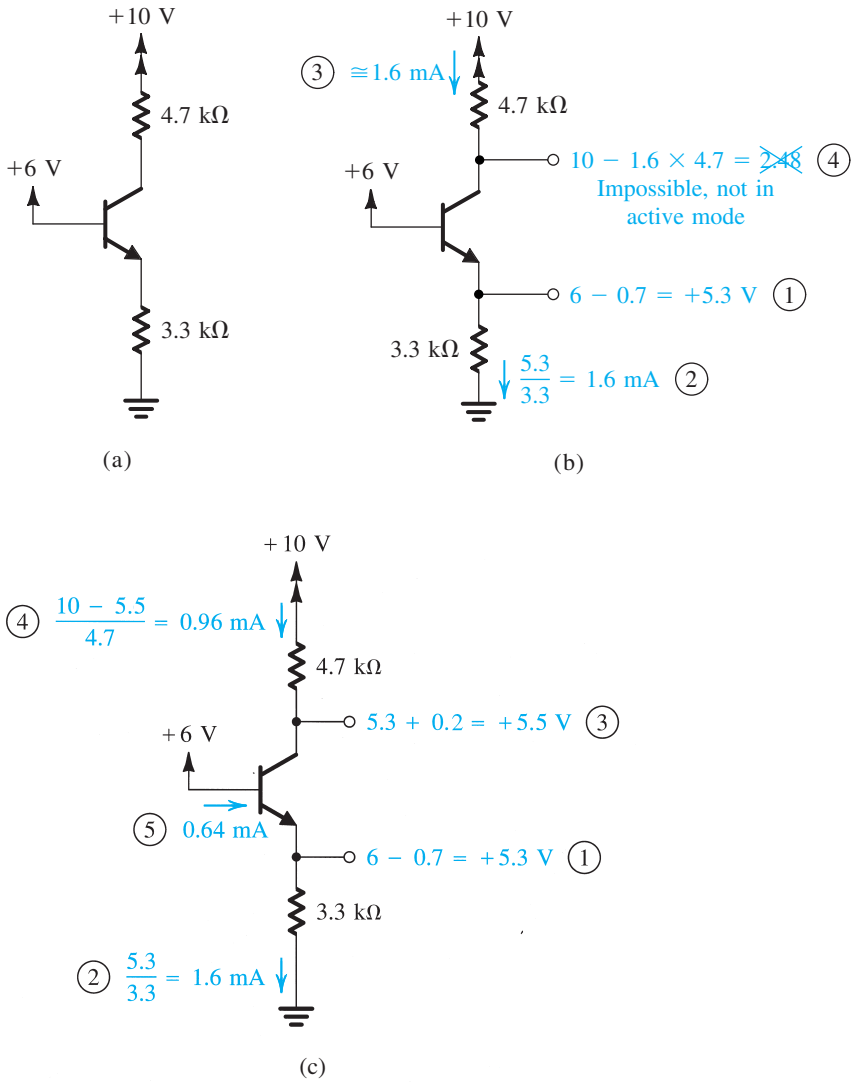


FIGURE 5.35 Analysis of the circuit for Example 5.5. Note that the circled numbers indicate the order of the analysis steps.

Solution

Assuming active-mode operation, we have

$$V_E = +6 - V_{BE} \simeq 6 - 0.7 = 5.3 \text{ V}$$

$$I_E = \frac{5.3}{3.3} = 1.6 \text{ mA}$$

$$V_C = +10 - 4.7 \times I_C \simeq 10 - 7.52 = 2.48 \text{ V}$$

The details of the analysis performed above are illustrated in Fig. 5.35(b).

Since the collector voltage calculated appears to be less than the base voltage by 3.52 V, it follows that our original assumption of active-mode operation is incorrect. In fact, the transistor has to be in the *saturation* mode. Assuming this to be the case, we have

$$V_E = +6 - 0.7 = +5.3 \text{ V}$$

$$I_E = \frac{V_E}{3.3} = \frac{5.3}{3.3} = 1.6 \text{ mA}$$

$$V_C = V_E + V_{CE\text{sat}} \simeq +5.3 + 0.2 = +5.5 \text{ V}$$

$$I_C = \frac{+10 - 5.5}{4.7} = 0.96 \text{ mA}$$

$$I_B = I_E - I_C = 1.6 - 0.96 = 0.64 \text{ mA}$$

Thus the transistor is operating at a forced β of

$$\beta_{\text{forced}} = \frac{I_C}{I_B} = \frac{0.96}{0.64} = 1.5$$

Since β_{forced} is less than the *minimum* specified value of β, the transistor is indeed saturated. We should emphasize here that in testing for saturation the minimum value of β should be used. By the same token, if we are designing a circuit in which a transistor is to be saturated, the design should be based on the minimum specified β. Obviously, if a transistor with this minimum β is saturated, then transistors with higher values of β will also be saturated. The details of the analysis are shown in Fig. 5.35(c), where the order of the steps used is indicated by the circled numbers.

EXAMPLE 5.6

We wish to analyze the circuit in Fig. 5.36(a) to determine the voltages at all nodes and the currents through all branches. Note that this circuit is identical to that considered in Examples 5.4 and 5.5 except that now the base voltage is zero.

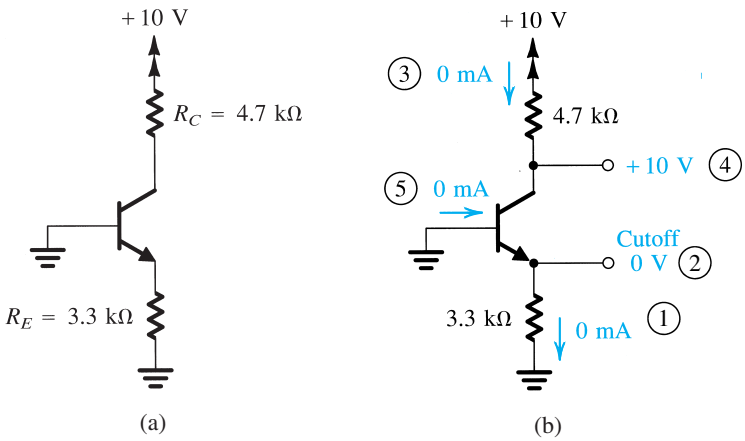


FIGURE 5.36 Example 5.6: **(a)** circuit; **(b)** analysis with the order of the analysis steps indicated by circled numbers.

Solution

Since the base is at zero volts, the emitter–base junction cannot conduct and the emitter current is zero. Also, the collector–base junction cannot conduct since the n-type collector is connected through R_C to the positive power supply while the p-type base is at ground. It follows that the collector current will be zero. The base current will also have to be zero, and the transistor is in the *cutoff* mode of operation.

The emitter voltage will obviously be zero, while the collector voltage will be equal to +10 V, since the voltage drop across R_C is zero. Figure 5.36(b) shows the analysis details.

EXERCISES

D5.22 For the circuit in Fig. 5.34(a), find the highest voltage to which the base can be raised while the transistor remains in the active mode. Assume $\alpha \simeq 1$.

Ans. +4.7 V

D5.23 Redesign the circuit of Fig. 5.35(a) (i.e., find new values for R_E and R_C) to establish a collector current of 0.5 mA and a reverse-bias voltage on the collector–base junction of 2 V. Assume $\alpha \simeq 1$.

Ans. $R_E = 6.6\ \text{k}\Omega$; $R_C = 8\ \text{k}\Omega$

5.24 For the circuit in Fig. 5.35(a), find the value to which the base voltage should be changed to so that the transistor operates in saturation with a forced β of 5.

Ans. +5.18 V

EXAMPLE 5.7

We desire to analyze the circuit of Fig. 5.37(a) to determine the voltages at all nodes and the currents through all branches.

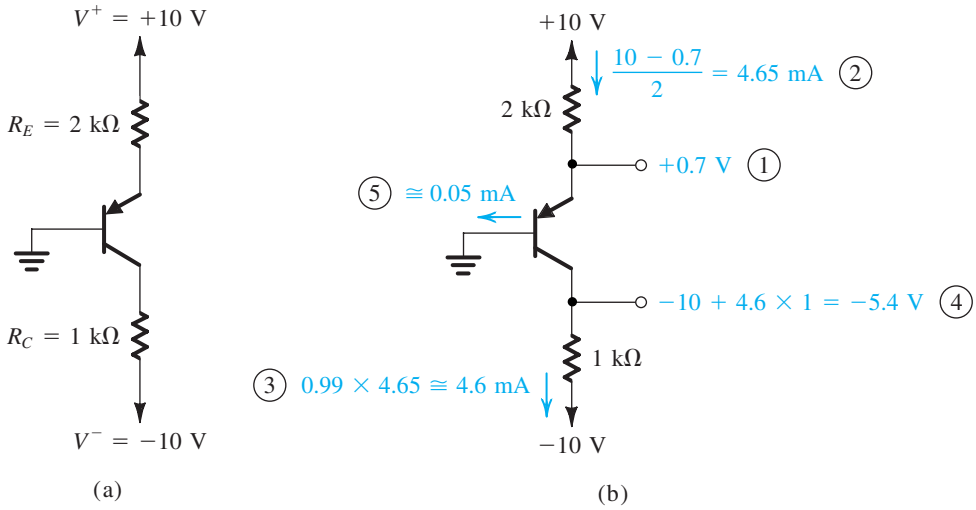


FIGURE 5.37 Example 5.7: **(a)** circuit; **(b)** analysis with the steps indicated by circled numbers.

Solution

The base of this *pnp* transistor is grounded, while the emitter is connected to a positive supply ($V^+ = +10$ V) through R_E. It follows that the emitter–base junction will be forward biased with

$$V_E = V_{EB} \simeq 0.7 \text{ V}$$

Thus the emitter current will be given by

$$I_E = \frac{V^+ - V_E}{R_E} = \frac{10 - 0.7}{2} = 4.65 \text{ mA}$$

Since the collector is connected to a negative supply (more negative than the base voltage) through R_C, it is *possible* that this transistor is operating in the active mode. Assuming this to be the case, we obtain

$$I_C = \alpha I_E$$

Since no value for β has been given, we shall assume $\beta = 100$, which results in $\alpha = 0.99$. Since large variations in β result in small differences in α, this assumption will not be critical as far as determining the value of I_C is concerned. Thus,

$$I_C = 0.99 \times 4.65 = 4.6 \text{ mA}$$

The collector voltage will be

$$\begin{aligned} V_C &= V^- + I_C R_C \\ &= -10 + 4.6 \times 1 = -5.4 \text{ V} \end{aligned}$$

Thus the collector–base junction is reverse biased by 5.4 V, and the transistor is indeed in the active mode, which supports our original assumption.

It remains only to calculate the base current,

$$I_B = \frac{I_E}{\beta + 1} = \frac{4.65}{101} \simeq 0.05 \text{ mA}$$

Obviously, the value of β critically affects the base current. Note, however, that in this circuit the value of β will have no effect on the mode of operation of the transistor. Since β is generally an ill-specified parameter, this circuit represents a good design. As a rule, one should strive to *design the circuit such that its performance is as insensitive to the value of β as possible.* The analysis details are illustrated in Fig. 5.37(b).

EXERCISES

D5.25 For the circuit in Fig. 5.37(a), find the largest value to which R_C can be raised while the transistor remains in the active mode.

Ans. 2.26 kΩ

D5.26 Redesign the circuit of Fig. 5.37(a) (i.e., find new values for R_E and R_C) to establish a collector current of 1 mA and a reverse bias on the collector–base junction of 4 V. Assume $\alpha \simeq 1$.

Ans. $R_E = 9.3$ kΩ; $R_C = 6$ kΩ

EXAMPLE 5.8

We want to analyze the circuit in Fig. 5.38(a) to determine the voltages at all nodes and the currents in all branches. Assume $\beta = 100$.

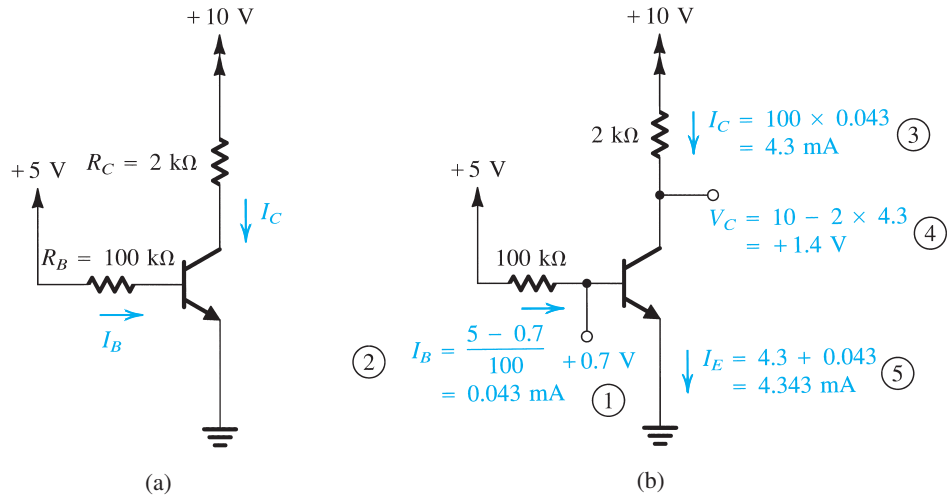


FIGURE 5.38 Example 5.8: **(a)** circuit; **(b)** analysis with the steps indicated by the circled numbers.

Solution

The base–emitter junction is clearly forward biased. Thus,

$$I_B = \frac{+5 - V_{BE}}{R_B} \simeq \frac{5 - 0.7}{100} = 0.043 \text{ mA}$$

Assume that the transistor is operating in the active mode. We now can write

$$I_C = \beta I_B = 100 \times 0.043 = 4.3 \text{ mA}$$

The collector voltage can now be determined as

$$V_C = +10 - I_C R_C = 10 - 4.3 \times 2 = +1.4 \text{ V}$$

Since the base voltage V_B is

$$V_B = V_{BE} \simeq +0.7 \text{ V}$$

it follows that the collector–base junction is reverse-biased by 0.7 V and the transistor is indeed in the active mode. The emitter current will be given by

$$I_E = (\beta + 1) I_B = 101 \times 0.043 \simeq 4.3 \text{ mA}$$

We note from this example that the collector and emitter currents depend critically on the value of β. In fact, if β were 10% higher, the transistor would leave the active mode and enter saturation. Therefore this clearly is a bad design. The analysis details are illustrated in Fig. 5.38(b).

EXERCISE

D5.27 The circuit of Fig. 5.38(a) is to be fabricated using a transistor type whose β is specified to be in the range of 50 to 150. That is, individual units of this same transistor type can have β values anywhere in this range. Redesign the circuit by selecting a new value for R_C so that all fabricated circuits are guaranteed to be in the active mode. What is the range of collector voltages that the fabricated circuits may exhibit?

Ans. $R_C = 1.5$ kΩ; $V_C = 0.3$ V to 6.8 V

EXAMPLE 5.9

We want to analyze the circuit of Fig. 5.39 to determine the voltages at all nodes and the currents through all branches. The minimum value of β is specified to be 30.

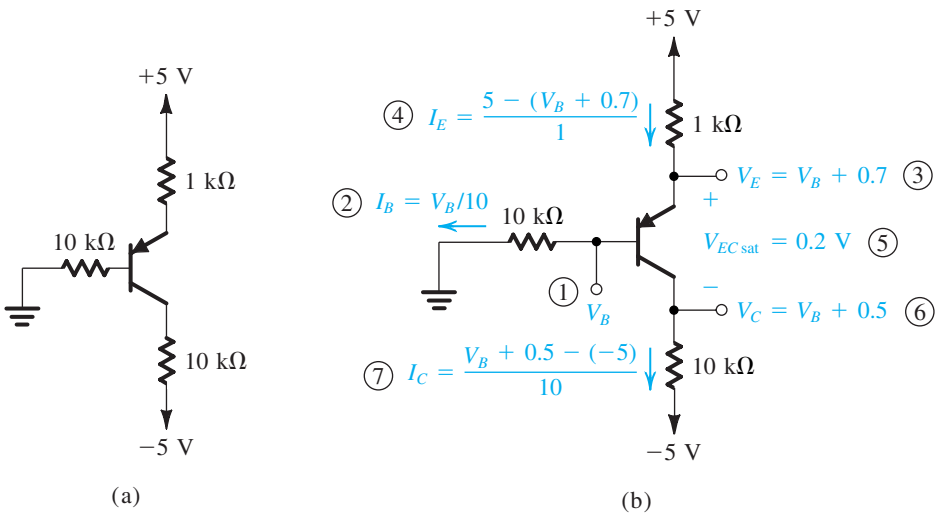


FIGURE 5.39 Example 5.9: **(a)** circuit; **(b)** analysis with steps numbered.

Solution

A quick glance at this circuit reveals that the transistor will be either active or saturated. Assuming active-mode operation and neglecting the base current, we see that the base voltage will be approximately zero volts, the emitter voltage will be approximately +0.7 V, and the emitter current will be approximately 4.3 mA. Since the maximum current that the collector can support while the transistor remains in the active mode is approximately 0.5 mA, it follows that the transistor is definitely saturated.

Assuming that the transistor is saturated and denoting the voltage at the base by V_B (refer to Fig. 5.39b), it follows that

$$V_E = V_B + V_{EB} \simeq V_B + 0.7$$

$$V_C = V_E - V_{EC\,sat} \simeq V_B + 0.7 - 0.2 = V_B + 0.5$$

$$I_E = \frac{+5 - V_E}{1} = \frac{5 - V_B - 0.7}{1} = 4.3 - V_B \text{ mA}$$

$$I_B = \frac{V_B}{10} = 0.1V_B \text{ mA}$$

$$I_C = \frac{V_C - (-5)}{10} = \frac{V_B + 0.5 + 5}{10} = 0.1V_B + 0.55 \text{ mA}$$

Using the relationship $I_E = I_B + I_C$, we obtain

$$4.3 - V_B = 0.1V_B + 0.1V_B + 0.55$$

which results in

$$V_B = \frac{3.75}{1.2} \simeq 3.13 \text{ V}$$

Substituting in the equations above, we obtain

$$V_E = 3.83 \text{ V}$$
$$V_C = 3.63 \text{ V}$$
$$I_E = 1.17 \text{ mA}$$
$$I_C = 0.86 \text{ mA}$$
$$I_B = 0.31 \text{ mA}$$

It is clear that the transistor is saturated, since the value of forced β is

$$\beta_{\text{forced}} = \frac{0.86}{0.31} \simeq 2.8$$

which is much smaller than the specified minimum β.

EXAMPLE 5.10

We want to analyze the circuit of Fig. 5.40(a) to determine the voltages at all nodes and the currents through all branches. Assume $\beta = 100$.

Solution

The first step in the analysis consists of simplifying the base circuit using Thévenin's theorem. The result is shown in Fig. 5.40(b), where

$$V_{BB} = +15\frac{R_{B2}}{R_{B1} + R_{B2}} = 15\frac{50}{100 + 50} = +5 \text{ V}$$

$$R_{BB} = (R_{B1} \,//\, R_{B2}) = (100 \,//\, 50) = 33.3 \text{ k}\Omega$$

To evaluate the base or the emitter current, we have to write a loop equation around the loop marked L in Fig. 5.40(b). Note, though, that the current through R_{BB} is different from the current through R_E. The loop equation will be

$$V_{BB} = I_B R_{BB} + V_{BE} + I_E R_E$$

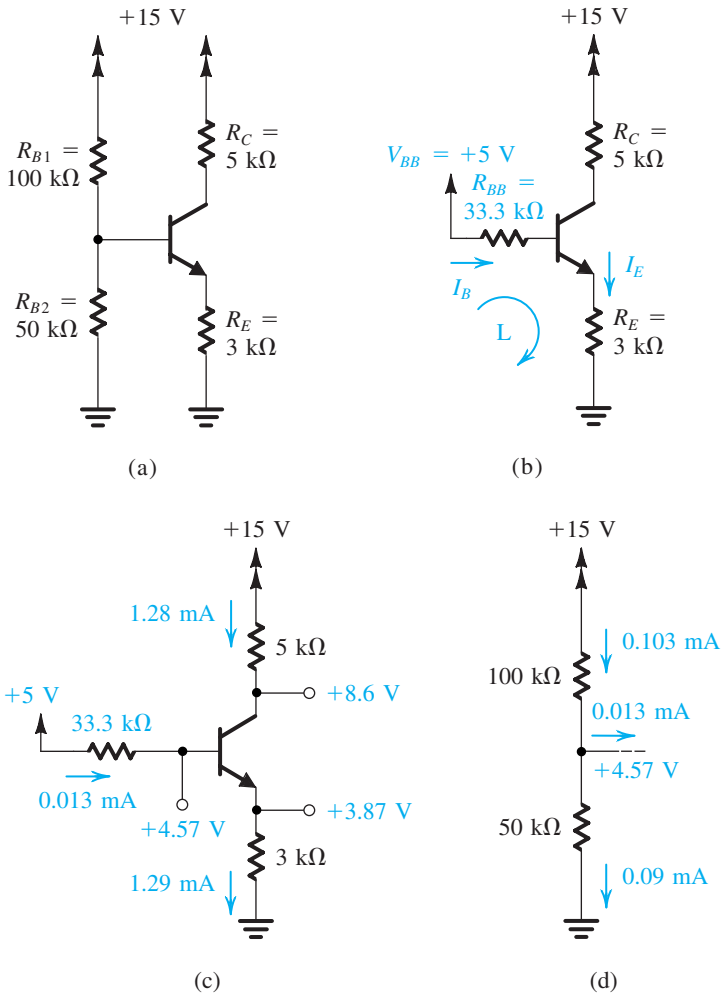


FIGURE 5.40 Circuits for Example 5.10.

Substituting for I_B by

$$I_B = \frac{I_E}{\beta + 1}$$

and rearranging the equation gives

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + [R_{BB}/(\beta + 1)]}$$

For the numerical values given we have

$$I_E = \frac{5 - 0.7}{3 + (33.3/101)} = 1.29 \text{ mA}$$

The base current will be

$$I_B = \frac{1.29}{101} = 0.0128 \text{ mA}$$

The base voltage is given by

$$V_B = V_{BE} + I_E R_E$$
$$= 0.7 + 1.29 \times 3 = 4.57 \text{ V}$$

Assume active-mode operation. We can evaluate the collector current as

$$I_C = \alpha I_E = 0.99 \times 1.29 = 1.28 \text{ mA}$$

The collector voltage can now be evaluated as

$$V_C = +15 - I_C R_C = 15 - 1.28 \times 5 = 8.6 \text{ V}$$

It follows that the collector is higher in potential than the base by 4.03 V, which means that the transistor is in the active mode, as had been assumed. The results of the analysis are given in Fig. 5.40(c).

EXERCISE

5.28 If the transistor in the circuit of Fig. 5.40(a) is replaced with another having half the value of β (i.e., $\beta = 50$), find the new value of I_C, and express the change in I_C as a percentage.

Ans. $I_C = 1.15$ mA; -10%

EXAMPLE 5.11

We wish to analyze the circuit in Fig. 5.41(a) to determine the voltages at all nodes and the currents through all branches.

Solution

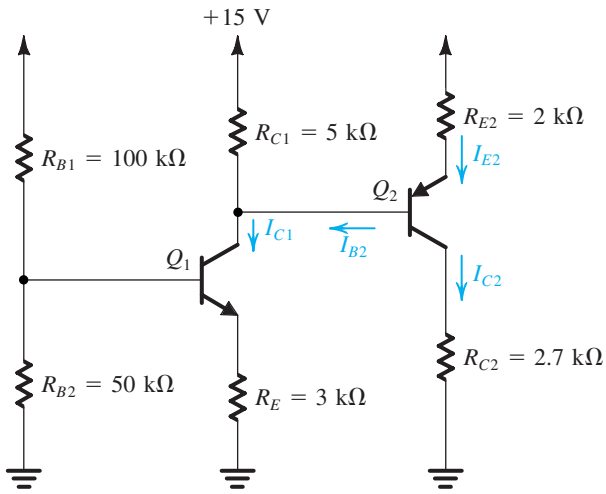
We first recognize that part of this circuit is identical to the circuit we analyzed in Example 5.10—namely, the circuit of Fig. 5.40(a). The difference, of course, is that in the new circuit we have an additional transistor Q_2 together with its associated resistors R_{E2} and R_{C2}. Assume that Q_1 is still in the active mode. The following values will be identical to those obtained in the previous example:

$$V_{B1} = +4.57 \text{ V} \qquad I_{E1} = 1.29 \text{ mA}$$
$$I_{B1} = 0.0128 \text{ mA} \qquad I_{C1} = 1.28 \text{ mA}$$

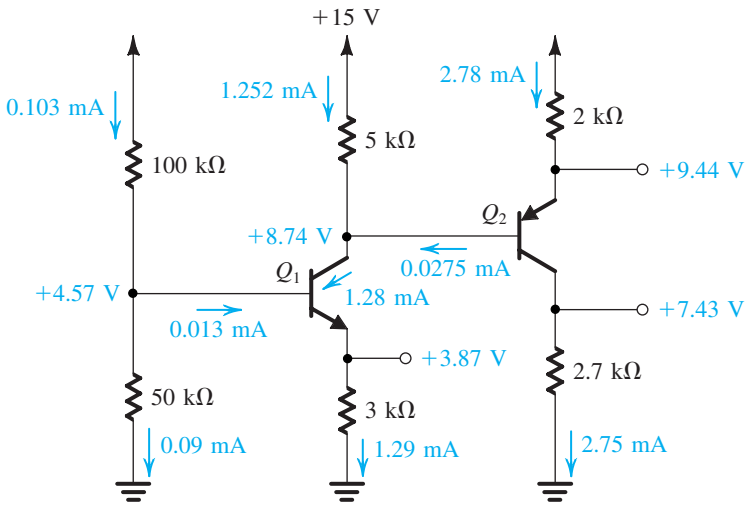
However, the collector voltage will be different than previously calculated since part of the collector current I_{C1} will flow in the base lead of Q_2 (I_{B2}). As a first approximation we may assume that I_{B2} is much smaller than I_{C1}; that is, we may assume that the current through R_{C1} is almost equal to I_{C1}. This will enable us to calculate V_{C1}:

$$V_{C1} \simeq +15 - I_{C1} R_{C1}$$
$$= 15 - 1.28 \times 5 = +8.6 \text{ V}$$

Thus Q_1 is in the active mode, as had been assumed.



(a)



(b)

FIGURE 5.41 Circuits for Example 5.11.

As far as Q_2 is concerned, we note that its emitter is connected to +15 V through R_{E2}. It is therefore safe to assume that the emitter–base junction of Q_2 will be forward biased. Thus the emitter of Q_2 will be at a voltage V_{E2} given by

$$V_{E2} = V_{C1} + V_{EB}|_{Q_2} \simeq 8.6 + 0.7 = +9.3 \text{ V}$$

The emitter current of Q_2 may now be calculated as

$$I_{E2} = \frac{+15 - V_{E2}}{R_{E2}} = \frac{15 - 9.3}{2} = 2.85 \text{ mA}$$

Since the collector of Q_2 is returned to ground via R_{C2}, it is possible that Q_2 is operating in the active mode. Assume this to be the case. We now find I_{C2} as

$$\begin{aligned} I_{C2} &= \alpha_2 I_{E2} \\ &= 0.99 \times 2.85 = 2.82 \text{ mA} \quad (\text{assuming } \beta_2 = 100) \end{aligned}$$

The collector voltage of Q_2 will be

$$V_{C2} = I_{C2} R_{C2} = 2.82 \times 2.7 = 7.62 \text{ V}$$

which is lower than V_{B2} by 0.98 V. Thus Q_2 is in the active mode, as assumed.

It is important at this stage to find the magnitude of the error incurred in our calculations by the assumption that I_{B2} is negligible. The value of I_{B2} is given by

$$I_{B2} = \frac{I_{E2}}{\beta_2 + 1} = \frac{2.85}{101} = 0.028 \text{ mA}$$

which is indeed much smaller than I_{C1} (1.28 mA). If desired, we can obtain more accurate results by iterating one more time, assuming I_{B2} to be 0.028 mA. The new values will be

$$\begin{aligned} \text{Current in } R_{C1} &= I_{C1} - I_{B2} = 1.28 - 0.028 = 1.252 \text{ mA} \\ V_{C1} &= 15 - 5 \times 1.252 = 8.74 \text{ V} \\ V_{E2} &= 8.74 + 0.7 = 9.44 \text{ V} \\ I_{E2} &= \frac{15 - 9.44}{2} = 2.78 \text{ mA} \\ I_{C2} &= 0.99 \times 2.78 = 2.75 \text{ mA} \\ V_{C2} &= 2.75 \times 2.7 = 7.43 \text{ V} \\ I_{B2} &= \frac{2.78}{101} = 0.0275 \text{ mA} \end{aligned}$$

Note that the new value of I_{B2} is very close to the value used in our iteration, and no further iterations are warranted. The final results are indicated in Fig. 5.41(b).

The reader justifiably might be wondering about the necessity for using an iterative scheme in solving a linear (or linearized) problem. Indeed, we can obtain the exact solution (if we can call anything we are doing with a first-order model exact!) by writing appropriate equations. The reader is encouraged to find this solution and then compare the results with those obtained above. It is important to emphasize, however, that in most such problems it is quite sufficient to obtain an approximate solution, provided that we can obtain it quickly and, of course, correctly.

In the above examples, we frequently used a precise value of α to calculate the collector current. Since $\alpha \simeq 1$, the error in such calculations will be very small if one assumes $\alpha = 1$ and $i_C = i_E$. Therefore, except in calculations that depend critically on the value of α (e.g., the calculation of base current), one usually assumes $\alpha \simeq 1$.

EXERCISES

5.29 For the circuit in Fig. 5.41, find the total current drawn from the power supply. Hence find the power dissipated in the circuit.

Ans. 4.135 mA; 62 mW

5.30 The circuit in Fig. E5.30 is to be connected to the circuit in Fig. 5.41(a) as indicated; specifically, the base of Q_3 is to be connected to the collector of Q_2. If Q_3 has $\beta = 100$, find the new value of V_{C2} and the values of V_{E3} and I_{C3}.

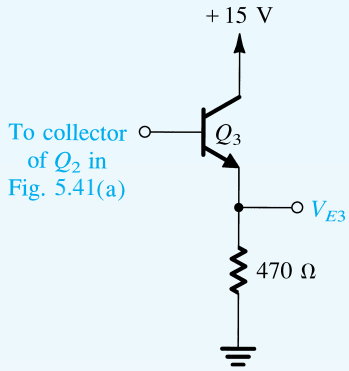


FIGURE E5.30

Ans. +7.06 V; +6.36 V; 13.4 mA

EXAMPLE 5.12

We desire to evaluate the voltages at all nodes and the currents through all branches in the circuit of Fig. 5.42(a). Assume $\beta = 100$.

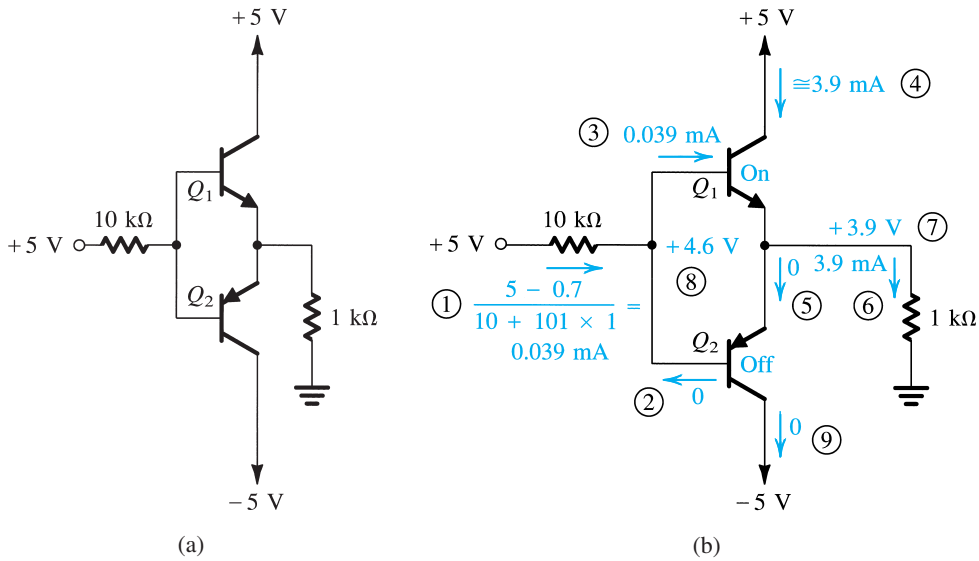


FIGURE 5.42 Example 5.12: **(a)** circuit; **(b)** analysis with the steps numbered.

Solution

By examining the circuit we conclude that the two transistors Q_1 and Q_2 cannot be simultaneously conducting. Thus if Q_1 is on, Q_2 will be off, and vice versa. Assume that Q_2 is on. It

follows that current will flow from ground through the 1-kΩ load resistor into the emitter of Q_2. Thus the base of Q_2 will be at a negative voltage, and base current will be flowing out of the base through the 10-kΩ resistor and into the +5-V supply. This is impossible, since if the base is negative, current in the 10-kΩ resistor will have to flow into the base. Thus we conclude that our original assumption—that Q_2 is on—is incorrect. It follows that Q_2 will be off and Q_1 will be on.

The question now is whether Q_1 is active or saturated. The answer in this case is obvious. Since the base is fed with a +5-V supply and since base current flows into the base of Q_1, it follows that the base of Q_1 will be at a voltage lower than +5 V. Thus the collector–base junction of Q_1 is reverse biased and Q_1 is in the active mode. It remains only to determine the currents and voltages using techniques already described in detail. The results are given in Fig. 5.42(b).

EXERCISE

5.31 Solve the problem in Example 5.12 with the voltage feeding the bases changed to +10 V. Assume that $\beta_{\text{min}} = 30$, and find V_E, V_B, I_{C1}, and I_{C2}.

Ans. +4.8 V; +5.5 V; 4.35 mA; 0

5.5 BIASING IN BJT AMPLIFIER CIRCUITS

The biasing problem is that of establishing a constant dc current in the collector of the BJT. This current has to be calculable, predictable, and insensitive to variations in temperature and to the large variations in the value of β encountered among transistors of the same type. Another important consideration in bias design is locating the dc bias point in the i_C–v_{CE} plane to allow for maximum output signal swing (see the discussion in Section 5.3.3). In this section, we shall deal with various approaches to solving the bias problem in transistor circuits designed with discrete devices. Bias methods for integrated-circuit design are presented in Chapter 6.

Before presenting the "good" biasing schemes, we should point out why two obvious arrangements are not good. First, attempting to bias the BJT by fixing the voltage V_{BE} by, for instance, using a voltage divider across the power supply V_{CC}, as shown in Fig. 5.43(a), is not a viable approach: The very sharp exponential relationship i_C–v_{BE} means that any small and inevitable differences in V_{BE} from the desired value will result in large differences in I_C and in V_{CE}. Second, biasing the BJT by establishing a constant current in the base, as shown in Fig. 5.43(b), where $I_B \cong (V_{CC} - 0.7)/R_B$, is also not a recommended approach. Here the typically large variations in the value of β among units of the same device type will result in correspondingly large variations in I_C and hence in V_{CE}.

5.5.1 Classical Discrete-Circuit Bias Arrangement

Figure 5.44(a) shows the arrangement most commonly used for biasing a discrete-circuit transistor amplifier if only a single power supply is available. The technique consists of supplying the base of the transistor with a fraction of the supply voltage V_{CC} through the voltage divider R_1, R_2. In addition, a resistor R_E is connected to the emitter.

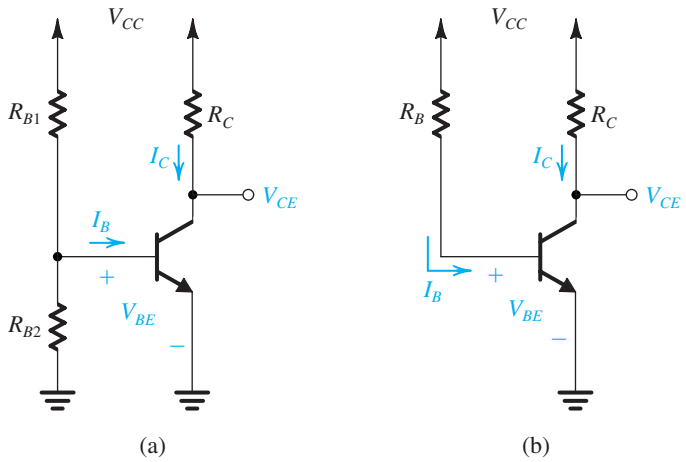


FIGURE 5.43 Two obvious schemes for biasing the BJT: **(a)** by fixing V_{BE}; **(b)** by fixing I_B. Both result in wide variations in I_C and hence in V_{CE} and therefore are considered to be "bad." Neither scheme is recommended.

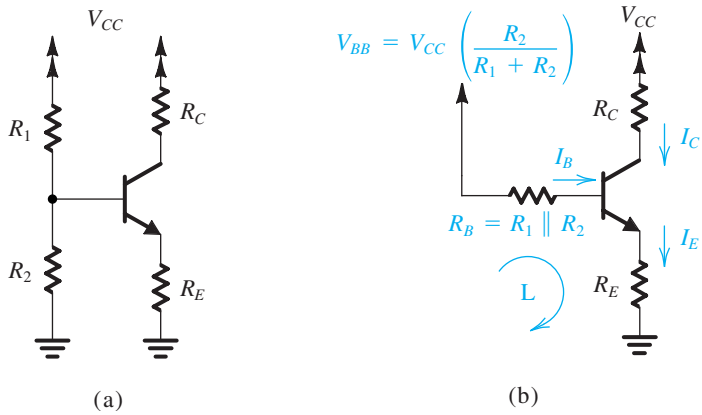


FIGURE 5.44 Classical biasing for BJTs using a single power supply: **(a)** circuit; **(b)** circuit with the voltage divider supplying the base replaced with its Thévenin equivalent.

Figure 5.44(b) shows the same circuit with the voltage-divider network replaced by its Thévenin equivalent,

$$V_{BB} = \frac{R_2}{R_1 + R_2} V_{CC} \tag{5.68}$$

$$R_B = \frac{R_1 R_2}{R_1 + R_2} \tag{5.69}$$

The current I_E can be determined by writing a Kirchhoff loop equation for the base–emitter–ground loop, labeled L, and substituting $I_B = I_E/(\beta + 1)$:

$$I_E = \frac{V_{BB} - V_{BE}}{R_E + R_B/(\beta + 1)} \tag{5.70}$$

To make I_E insensitive to temperature and β variation,[8] we design the circuit to satisfy the following two constraints:

$$V_{BB} \gg V_{BE} \tag{5.71}$$

$$R_E \gg \frac{R_B}{\beta + 1} \tag{5.72}$$

Condition (5.71) ensures that small variations in V_{BE} (≈0.7 V) will be swamped by the much larger V_{BB}. There is a limit, however, on how large V_{BB} can be: For a given value of the supply voltage V_{CC}, the higher the value we use for V_{BB}, the lower will be the sum of voltages across R_C and the collector–base junction (V_{CB}). On the other hand, we want the voltage across R_C to be large in order to obtain high voltage gain and large signal swing (before transistor cutoff). We also want V_{CB} (or V_{CE}) to be large to provide a large signal swing (before transistor saturation). Thus, as is the case in any design problem, we have a set of conflicting requirements, and the solution must be a compromise. As a rule of thumb, one designs for V_{BB} about $\frac{1}{3}V_{CC}$, V_{CB} (or V_{CE}) about $\frac{1}{3}V_{CC}$, and $I_C R_C$ about $\frac{1}{3}V_{CC}$.

Condition (5.72) makes I_E insensitive to variations in β and could be satisfied by selecting R_B small. This in turn is achieved by using low values for R_1 and R_2. Lower values for R_1 and R_2, however, will mean a higher current drain from the power supply and normally will result in a lowering of the input resistance of the amplifier (if the input signal is coupled to the base), which is the trade-off involved in this part of the design problem. It should be noted that Condition (5.72) means that we want to make the base voltage independent of the value of β and determined solely by the voltage divider. This will obviously be satisfied if the current in the divider is made much larger than the base current. Typically one selects R_1 and R_2 such that their current is in the range of I_E to $0.1I_E$.

Further insight regarding the mechanism by which the bias arrangement of Fig. 5.44(a) stabilizes the dc emitter (and hence collector) current is obtained by considering the feedback action provided by R_E. Consider that for some reason the emitter current increases. The voltage drop across R_E, and hence V_E will increase correspondingly. Now, if the base voltage is determined primarily by the voltage divider R_1, R_2, which is the case if R_B is small, it will remain constant, and the increase in V_E will result in a corresponding decrease in V_{BE}. This in turn reduces the collector (and emitter) current, a change opposite to that originally assumed. Thus R_E provides a *negative feedback* action that stabilizes the bias current. We shall study negative feedback formally in Chapter 9.

EXAMPLE 5.13

We wish to design the bias network of the amplifier in Fig. 5.44 to establish a current $I_E = 1$ mA using a power supply $V_{CC} = +12$ V. The transistor is specified to have a nominal β value of 100.

Solution

We shall follow the rule of thumb mentioned above and allocate one-third of the supply voltage to the voltage drop across R_2 and another one-third to the voltage drop across R_C, leaving one-third

[8] Bias design seeks to stabilize either I_E or I_C since $I_C = \alpha I_E$ and α varies very little. That is, a stable I_E will result in an equally stable I_C, and vice versa.

for possible signal swing at the collector. Thus,

$$V_B = +4 \text{ V}$$

$$V_E = 4 - V_{BE} \simeq 3.3 \text{ V}$$

and R_E is determined from

$$R_E = \frac{V_E}{I_E} = 3.3 \text{ k}\Omega$$

From the discussion above we select a voltage-divider current of $0.1I_E = 0.1 \times 1 = 0.1$ mA. Neglecting the base current, we find

$$R_1 + R_2 = \frac{12}{0.1} = 120 \text{ k}\Omega$$

and

$$\frac{R_2}{R_1 + R_2} V_{CC} = 4 \text{ V}$$

Thus $R_2 = 40$ kΩ and $R_1 = 80$ kΩ.

At this point, it is desirable to find a more accurate estimate for I_E, taking into account the nonzero base current. Using Eq. (5.70),

$$I_E = \frac{4 - 0.7}{3.3(\text{k}\Omega) + \dfrac{(80 \,//\, 40)(\text{k}\Omega)}{101}} = 0.93 \text{ mA}$$

This is quite a bit lower than the value we are aiming for of 1 mA. It is easy to see from the above equation that a simple way to restore I_E to its nominal value would be to reduce R_E from 3.3 kΩ by the magnitude of the second term in the denominator (0.267 kΩ). Thus a more suitable value for R_E in this case would be $R_E = 3$ kΩ, which results in $I_E = 1.01$ mA $\simeq 1$ mA.

It should be noted that if we are willing to draw a higher current from the power supply and to accept a lower input resistance for the amplifier, then we may use a voltage-divider current equal, say, to I_E (i.e., 1 mA), resulting in $R_1 = 8$ kΩ and $R_2 = 4$ kΩ. We shall refer to the circuit using these latter values as design 2, for which the actual value of I_E using the initial value of R_E of 3.3 kΩ will be

$$I_E = \frac{4 - 0.7}{3.3 + 0.027} = 0.99 \simeq 1 \text{ mA}$$

In this case, design 2, we need not change the value of R_E.

Finally, the value of R_C can be determined from

$$R_C = \frac{12 - V_C}{I_C}$$

Substituting $I_C = \alpha I_E = 0.99 \times 1 = 0.99$ mA $\simeq 1$ mA results, for both designs, in

$$R_C = \frac{12 - 8}{1} = 4 \text{ k}\Omega$$

EXERCISE

5.32 For design 1 in Example 5.13, calculate the expected range of I_E if the transistor used has β in the range of 50 to 150. Express the range of I_E as a percentage of the nominal value ($I_E \simeq 1$ mA) obtained for $\beta = 100$. Repeat for design 2.

Ans. For design 1: 0.94 mA to 1.04 mA a 10% range; for design 2: 0.984 mA to 0.995 mA, a 1.1% range.

5.5.2 A Two Power-Supply Version of the Classical Bias Arrangement

A somewhat simpler bias arrangement is possible if two power supplies are available, as shown in Fig. 5.45. Writing a loop equation for the loop labeled L gives

$$I_E = \frac{V_{EE} - V_{BE}}{R_E + R_B/(\beta + 1)} \tag{5.73}$$

This equation is identical to Eq. (5.70) except for V_{EE} replacing V_{BB}. Thus the two constraints of Eqs. (5.71) and (5.72) apply here as well. Note that if the transistor is to be used with the base grounded (i.e., in the common-base configuration), then R_B can be eliminated altogether. On the other hand, if the input signal is to be coupled to the base, then R_B is needed. We shall study the various BJT amplifier configurations in Section 5.7.

EXERCISE

D5.33 The bias arrangement of Fig. 5.45 is to be used for a common-base amplifier. Design the circuit to establish a dc emitter current of 1 mA and provide the highest possible voltage gain while allowing for a maximum signal swing at the collector of ±2 V. Use +10-V and −5-V power supplies.

Ans. $R_B = 0$; $R_E = 4.3$ kΩ; $R_C = 8.4$ kΩ

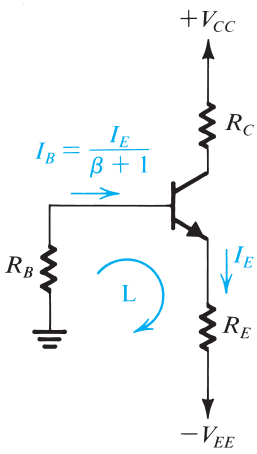


FIGURE 5.45 Biasing the BJT using two power supplies. Resistor R_B is needed only if the signal is to be coupled to the base. Otherwise, the base can be connected directly to ground, resulting in almost total independence of the bias current with regard to the value of β.

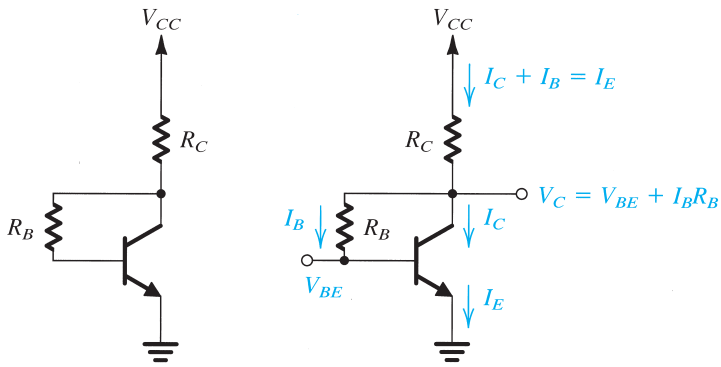


FIGURE 5.46 **(a)** A common-emitter transistor amplifier biased by a feedback resistor R_B. **(b)** Analysis of the circuit in (a).

5.5.3 Biasing Using a Collector-to-Base Feedback Resistor

Figure 5.46(a) shows a simple but effective alternative biasing arrangement suitable for common-emitter amplifiers. The circuit employs a resistor R_B connected between the collector and the base. Resistor R_B provides negative feedback, which helps to stabilize the bias point of the BJT. We shall study feedback formally in Chapter 9.

Analysis of the circuit is shown in Fig. 5.46(b), from which we can write

$$\begin{aligned} V_{CC} &= I_E R_C + I_B R_B + V_{BE} \\ &= I_E R_C + \frac{I_E}{\beta + 1} R_B + V_{BE} \end{aligned}$$

Thus the emitter bias current is given by

$$I_E = \frac{V_{CC} - V_{BE}}{R_C + R_B/(\beta + 1)} \tag{5.74}$$

It is interesting to note that this equation is identical to Eq. (5.70), which governs the operation of the traditional bias circuit, except that V_{CC} replaces V_{BB} and R_C replaces R_E. It follow that to obtain a value of I_E that is insensitive to variation of β, we select $R_B/(\beta + 1) \ll R_C$. Note, however, that the value of R_B determines the allowable signal swing at the collector since

$$V_{CB} = I_B R_B = I_E \frac{R_B}{\beta + 1} \tag{5.75}$$

EXERCISE

D5.34 Design the circuit of Fig. 5.46 to obtain a dc emitter current of 1 mA and to ensure a ±2-V signal swing at the collector; that is, design for $V_{CE} = +2.4$ V. Let $V_{CC} = 10$ V and $\beta = 100$.

Ans. $R_B = 172$ kΩ; $R_C = 7.6$ kΩ. Note that if standard 5% resistor values are used (Appendix H) we select $R_B = 180$ kΩ and $R_C = 7.5$ kΩ. This results in $I_E = 1.00$ mA and $V_C = +2.5$ V.

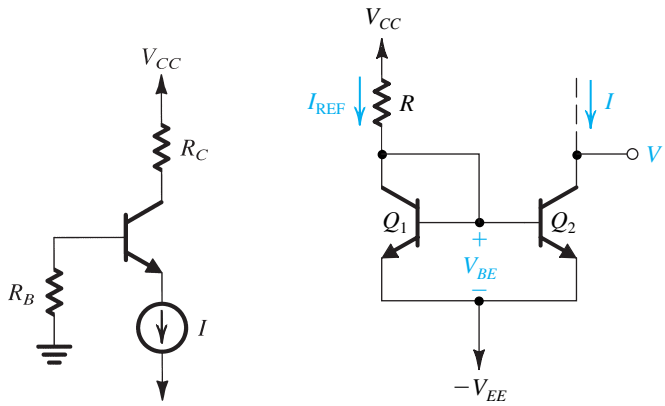


FIGURE 5.47 **(a)** A BJT biased using a constant-current source I. **(b)** Circuit for implementing the current source I.

5.5.4 Biasing Using a Constant-Current Source

The BJT can be biased using a constant-current source I as indicated in the circuit of Fig. 5.47(a). This circuit has the advantage that the emitter current is independent of the values of β and R_B. Thus R_B can be made large, enabling an increase in the input resistance at the base without adversely affecting bias stability. Further, current-source biasing leads to significant design simplification, as will become obvious in later sections and chapters.

A simple implementation of the constant-current source I is shown in Fig. 4.47(b). The circuit utilizes a pair of matched transistors Q_1 and Q_2, with Q_1 connected as a diode by shorting its collector to its base. If we assume that Q_1 and Q_2 have high β values, we can neglect their base currents. Thus the current through Q_1 will be approximately equal to I_{REF},

$$I_{\text{REF}} = \frac{V_{CC} - (-V_{EE}) - V_{BE}}{R} \tag{5.76}$$

Now, since Q_1 and Q_2 have the same V_{BE}, their collector currents will be equal, resulting in

$$I = I_{\text{REF}} = \frac{V_{CC} + V_{EE} - V_{BE}}{R} \tag{5.77}$$

Neglecting the Early effect in Q_2, the collector current will remain constant at the value given by this equation as long as Q_2 remains in the active region. This can be guaranteed by keeping the voltage at the collector V greater than that at the base $(-V_{EE} + V_{BE})$. The connection of Q_1 and Q_2 in Fig. 4.47(b) is known as a **current mirror.** We will study current mirrors in detail in Chapter 6.

EXERCISE

5.35 For the circuit in Fig. 5.47(a) with $V_{CC} = 10$ V, $I = 1$ mA, $\beta = 100$, $R_B = 100$ kΩ, and $R_C = 7.5$ kΩ, find the dc voltage at the base, the emitter, and the collector. For $V_{EE} = 10$ V, find the value of R in the circuit of Fig. 5.47(b).

Ans. −1 V; −1.7 V; +2.6 V; 19.3 kΩ

5.6 SMALL-SIGNAL OPERATION AND MODELS

Having learned how to bias the BJT to operate as an amplifier, we now take a closer look at the small-signal operation of the transistor. Toward that end, consider the *conceptual* circuit shown in Fig. 5.48(a). Here the base–emitter junction is forward biased by a dc voltage V_{BE} (battery). The reverse bias of the collector–base junction is established by connecting the collector to another power supply of voltage V_{CC} through a resistor R_C. The input signal to be amplified is represented by the voltage source v_{be} that is superimposed on V_{BE}.

We consider first the dc bias conditions by setting the signal v_{be} to zero. The circuit reduces to that in Fig. 5.48(b), and we can write the following relationships for the dc currents and voltages:

$$I_C = I_S e^{V_{BE}/V_T} \tag{5.78}$$

$$I_E = I_C/\alpha \tag{5.79}$$

$$I_B = I_C/\beta \tag{5.80}$$

$$V_C = V_{CE} = V_{CC} - I_C R_C \tag{5.81}$$

Obviously, for active-mode operation, V_C should be greater than $(V_B - 0.4)$ by an amount that allows for a reasonable signal swing at the collector.

5.6.1 The Collector Current and the Transconductance

If a signal v_{be} is applied as shown in Fig. 5.48(a), the total instantaneous base–emitter voltage v_{BE} becomes

$$v_{BE} = V_{BE} + v_{be}$$

Correspondingly, the collector current becomes

$$i_C = I_S e^{v_{BE}/V_T} = I_S e^{(V_{BE}+v_{be})/V_T}$$
$$= I_S e^{(V_{BE}/V_T)} e^{(v_{be}/V_T)}$$

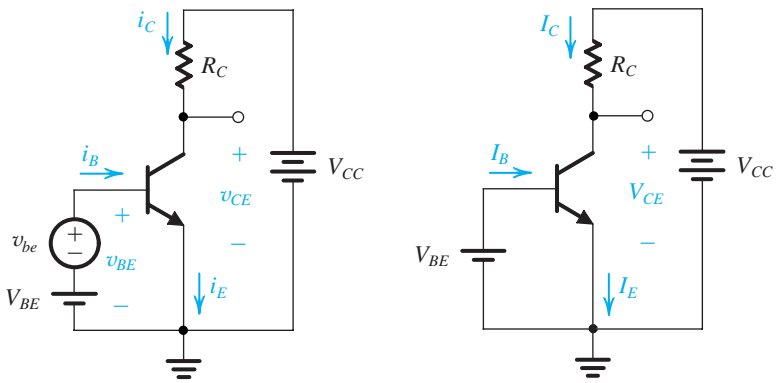


FIGURE 5.48 **(a)** Conceptual circuit to illustrate the operation of the transistor as an amplifier. **(b)** The circuit of (a) with the signal source v_{be} eliminated for dc (bias) analysis.

Use of Eq. (5.78) yields

$$i_C = I_C e^{v_{be}/V_T} \tag{5.82}$$

Now, if $v_{be} \ll V_T$, we may approximate Eq. (5.82) as

$$i_C \simeq I_C\left(1 + \frac{v_{be}}{V_T}\right) \tag{5.83}$$

Here we have expanded the exponential in Eq. (5.82) in a series and retained only the first two terms. This approximation, which is valid only for v_{be} less than approximately 10 mV, is referred to as the **small-signal approximation.** Under this approximation the total collector current is given by Eq. (5.83) and can be rewritten

$$i_C = I_C + \frac{I_C}{V_T} v_{be} \tag{5.84}$$

Thus the collector current is composed of the dc bias value I_C and a signal component i_c,

$$i_c = \frac{I_C}{V_T} v_{be} \tag{5.85}$$

This equation relates the signal current in the collector to the corresponding base–emitter signal voltage. It can be rewritten as

$$i_c = g_m v_{be} \tag{5.86}$$

where g_m is called the **transconductance,** and from Eq. (5.85), it is given by

$$g_m = \frac{I_C}{V_T} \tag{5.87}$$

We observe that the transconductance of the BJT is directly proportional to the collector bias current I_C. Thus to obtain a constant predictable value for g_m, we need a constant predictable I_C. Finally, we note that BJTs have relatively high transconductance (as compared to MOSFETs, which we studied in Chapter 4); for instance, at $I_C = 1$ mA, $g_m \simeq 40$ mA/V.

A graphical interpretation for g_m is given in Fig. 5.49, where it is shown that g_m is equal to the slope of the i_C–v_{BE} characteristic curve at $i_C = I_C$ (i.e., at the bias point Q). Thus,

$$g_m = \left.\frac{\partial i_C}{\partial v_{BE}}\right|_{i_C = I_C} \tag{5.88}$$

The small-signal approximation implies keeping the signal amplitude sufficiently small so that *operation is restricted to an almost-linear segment of the i_C–v_{BE} exponential curve.* Increasing the signal amplitude will result in the collector current having components nonlinearly related to v_{be}. This, of course, is the same approximation we discussed in the context of the amplifier transfer curve in Section 5.3.

The analysis above suggests that for small signals ($v_{be} \ll V_T$), the transistor behaves as a voltage-controlled current source. The input port of this controlled source is between base and emitter, and the output port is between collector and emitter. The transconductance of the controlled source is g_m, and the output resistance is infinite. The latter ideal property is a result of our first-order model of transistor operation in which the collector voltage has no effect on the collector current in the active mode. As we have seen in Section 5.2, practical

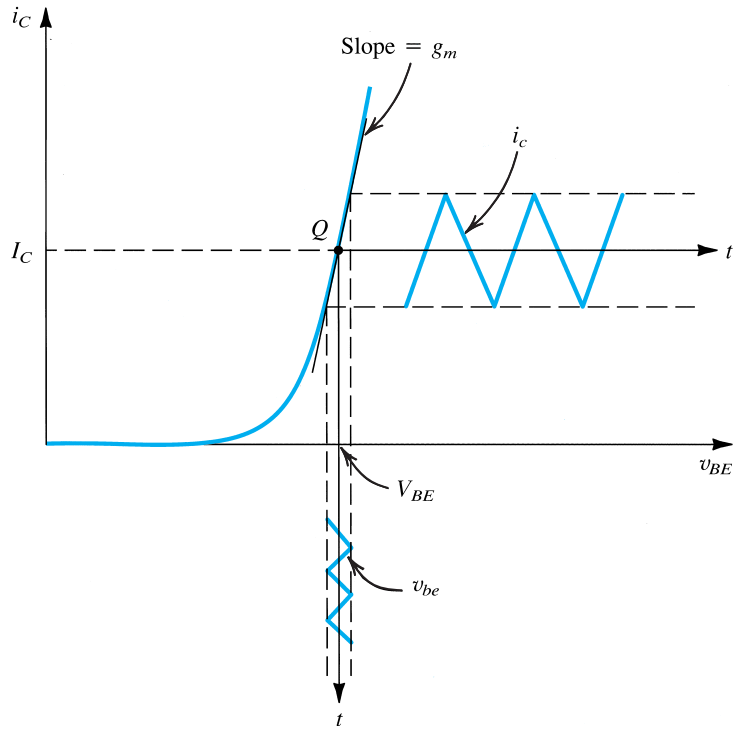


FIGURE 5.49 Linear operation of the transistor under the small-signal condition: A small signal v_{be} with a triangular waveform is superimposed on the dc voltage V_{BE}. It gives rise to a collector signal current i_c, also of triangular waveform, superimposed on the dc current I_C. $i_c = g_m v_{be}$, where g_m is the slope of the i_C–v_{BE} curve at the bias point Q.

BJTs have finite output resistance because of the Early effect. The effect of the output resistance on amplifier performance will be considered later.

EXERCISE

5.36 Use Eq. (5.88) to derive the expression for g_m in Eq. (5.87).

5.6.2 The Base Current and the Input Resistance at the Base

To determine the resistance seen by v_{be}, we first evaluate the total base current i_B using Eq. (5.84), as follows:

$$i_B = \frac{i_C}{\beta} = \frac{I_C}{\beta} + \frac{1}{\beta}\frac{I_C}{V_T} v_{be}$$

Thus,

$$i_B = I_B + i_b \tag{5.89}$$

where I_B is equal to I_C/β and the signal component i_b is given by

$$i_b = \frac{1}{\beta}\frac{I_C}{V_T} v_{be} \tag{5.90}$$

Substituting for I_C/V_T by g_m gives

$$i_b = \frac{g_m}{\beta} v_{be} \tag{5.91}$$

The small-signal input resistance between base and emitter, *looking into the base,* is denoted by r_π and is defined as

$$r_\pi \equiv \frac{v_{be}}{i_b} \tag{5.92}$$

Using Eq. (5.91) gives

$$r_\pi = \frac{\beta}{g_m} \tag{5.93}$$

Thus r_π is directly dependent on β and is inversely proportional to the bias current I_C. Substituting for g_m in Eq. (5.93) from Eq. (5.87) and replacing I_C/β by I_B gives an alternative expression for r_π,

$$r_\pi = \frac{V_T}{I_B} \tag{5.94}$$

5.6.3 The Emitter Current and the Input Resistance at the Emitter

The total emitter current i_E can be determined from

$$i_E = \frac{i_C}{\alpha} = \frac{I_C}{\alpha} + \frac{i_c}{\alpha}$$

Thus,

$$i_E = I_E + i_e \tag{5.95}$$

where I_E is equal to I_C/α and the signal current i_e is given by

$$i_e = \frac{i_c}{\alpha} = \frac{I_C}{\alpha V_T} v_{be} = \frac{I_E}{V_T} v_{be} \tag{5.96}$$

If we denote the small-signal resistance between base and emitter, *looking into the emitter,* by r_e, it can be defined as

$$r_e \equiv \frac{v_{be}}{i_e} \tag{5.97}$$

Using Eq. (5.96) we find that r_e, called the **emitter resistance,** is given by

$$r_e = \frac{V_T}{I_E} \tag{5.98}$$

Comparison with Eq. (5.87) reveals that

$$r_e = \frac{\alpha}{g_m} \simeq \frac{1}{g_m} \tag{5.99}$$

The relationship between r_π and r_e can be found by combining their respective definitions in Eqs. (5.92) and (5.97) as

$$v_{be} = i_b r_\pi = i_e r_e$$

Thus,

$$r_\pi = (i_e/i_b)r_e$$

which yields

$$r_\pi = (\beta+1)r_e \tag{5.100}$$

EXERCISE

5.37 A BJT having $\beta = 100$ is biased at a dc collector current of 1 mA. Find the value of g_m, r_e, and r_π at the bias point.

Ans. 40 mA/V; 25 Ω; 2.5 kΩ

5.6.4 Voltage Gain

In the preceding section we have established only that the transistor senses the base–emitter signal v_{be} and causes a proportional current $g_m v_{be}$ to flow in the collector lead at a high (ideally infinite) impedance level. In this way the transistor is acting as a voltage-controlled current source. To obtain an output voltage signal, we may force this current to flow through a resistor, as is done in Fig. 5.48(a). Then the total collector voltage v_C will be

$$\begin{aligned} v_C &= V_{CC} - i_C R_C \\ &= V_{CC} - (I_C + i_c)R_C \\ &= (V_{CC} - I_C R_C) - i_c R_C \\ &= V_C - i_c R_C \end{aligned} \tag{5.101}$$

Here the quantity V_C is the dc bias voltage at the collector, and the signal voltage is given by

$$\begin{aligned} v_c &= -i_c R_C = -g_m v_{be} R_C \\ &= (-g_m R_C) v_{be} \end{aligned} \tag{5.102}$$

Thus the voltage gain of this amplifier A_v is

$$A_v \equiv \frac{v_c}{v_{be}} = -g_m R_C \tag{5.103}$$

Here again we note that because g_m is directly proportional to the collector bias current, the gain will be as stable as the collector bias current is made. Substituting for g_m from Eq. (5.87) enables us to express the gain in the form

$$A_v = -\frac{I_C R_C}{V_T} \tag{5.104}$$

which is identical to the expression we derived in Section 5.3 (Eq. 5.56).

EXERCISE

5.38 In the circuit of Fig. 5.48(a), V_{BE} is adjusted to yield a dc collector current of 1 mA. Let $V_{CC} = 15$ V, $R_C = 10$ kΩ, and $\beta = 100$. Find the voltage gain v_c/v_{be}. If $v_{be} = 0.005 \sin \omega t$ volts, find $v_C(t)$ and $i_B(t)$.

Ans. –400 V/V; $5 - 2 \sin \omega t$ volts; $10 + 2 \sin \omega t$ μA

5.6.5 Separating the Signal and the DC Quantities

The analysis above indicates that every current and voltage in the amplifier circuit of Fig. 5.48(a) is composed of two components: a dc component and a signal component. For instance, $v_{BE} = V_{BE} + v_{be}$, $I_C = I_C + i_c$, and so on. The dc components are determined from the dc circuit given in Fig. 5.48(b) and from the relationships imposed by the transistor (Eqs. 5.78 through 5.81). On the other hand, a representation of the signal operation of the BJT can be obtained by eliminating the dc sources, as shown in Fig. 5.50. Observe that since the voltage of an ideal dc supply does not change, the signal voltage across it will be zero. For this reason we have replaced V_{CC} and V_{BE} with short circuits. Had the circuit contained ideal dc current sources, these would have been replaced by open circuits. Note, however, that the circuit of Fig. 5.50 is useful only in so far as it shows the various signal currents and voltages; it is *not* an actual amplifier circuit since the dc bias circuit is not shown.

Figure 5.50 also shows the expressions for the current increments i_c, i_b, and i_e obtained when a small signal v_{be} is applied. These relationships can be represented by a circuit. Such a circuit should have three terminals—C, B, and E—and should yield the same terminal currents indicated in Fig. 5.50. The resulting circuit is then *equivalent to the transistor as far as small-signal operation is concerned,* and thus it can be considered an equivalent small-signal circuit model.

5.6.6 The Hybrid-π Model

An equivalent circuit model for the BJT is shown in Fig. 5.51(a). This model represents the BJT as a voltage-controlled current source and explicitly includes the input resistance looking into

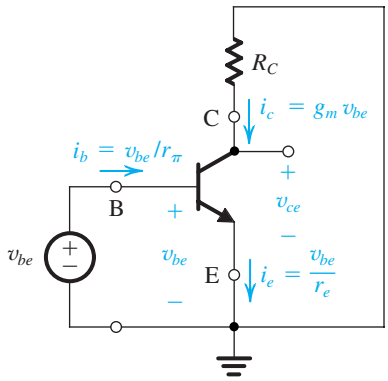


FIGURE 5.50 The amplifier circuit of Fig. 5.48(a) with the dc sources V_{BE} and V_{CC} eliminated (short circuited). Thus only the signal components are present. Note that this is a representation of the signal operation of the BJT and not an actual amplifier circuit.

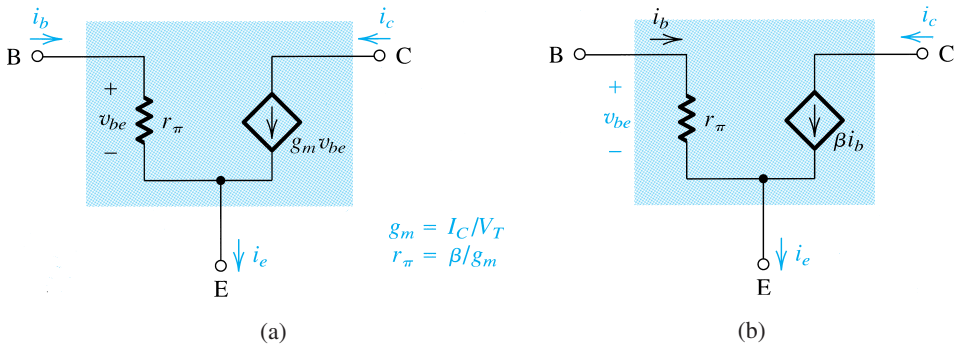


FIGURE 5.51 Two slightly different versions of the simplified hybrid-π model for the small-signal operation of the BJT. The equivalent circuit in **(a)** represents the BJT as a voltage-controlled current source (a transconductance amplifier), and that in **(b)** represents the BJT as a current-controlled current source (a current amplifier).

the base, r_π. The model obviously yields $i_c = g_m v_{be}$ and $i_b = v_{be}/r_\pi$. Not so obvious, however, is the fact that the model also yields the correct expression for i_e. This can be shown as follows: At the emitter node we have

$$\begin{aligned} i_e &= \frac{v_{be}}{r_\pi} + g_m v_{be} = \frac{v_{be}}{r_\pi}(1 + g_m r_\pi) \\ &= \frac{v_{be}}{r_\pi}(1+\beta) = v_{be}\Big/\left(\frac{r_\pi}{1+\beta}\right) \\ &= v_{be}/r_e \end{aligned}$$

A slightly different equivalent circuit model can be obtained by expressing the current of the controlled source ($g_m v_{be}$) in terms of the base current i_b as follows:

$$\begin{aligned} g_m v_{be} &= g_m(i_b r_\pi) \\ &= (g_m r_\pi) i_b = \beta i_b \end{aligned}$$

This results in the alternative equivalent circuit model shown in Fig. 5.51(b). Here the transistor is represented as a current-controlled current source, with the control current being i_b.

The two models of Fig. 5.51 are simplified versions of what is known as the hybrid-π model. This is the most widely used model for the BJT.

It is important to note that the small-signal equivalent circuits of Fig. 5.51 model the operation of the BJT at a given bias point. This should be obvious from the fact that the model parameters g_m and r_π depend on the value of the dc bias current I_C, as indicated in Fig. 5.51. Finally, although the models have been developed for an *npn* transistor, they apply equally well to *pnp* transistors *with no change of polarities*.

5.6.7 The T Model

Although the hybrid-π model (in one of its two variants shown in Fig. 5.51) can be used to carry out small-signal analysis of all transistor circuits, there are situations in which an alternative model, shown in Fig. 5.52, is much more convenient. This model, called the **T model,** is shown

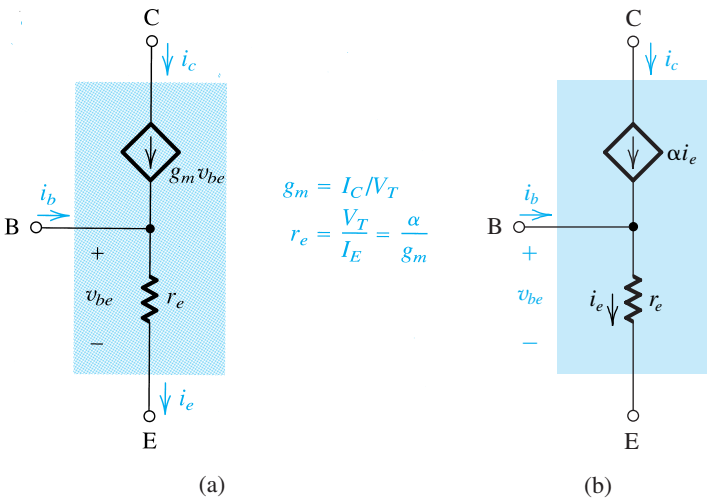


FIGURE 5.52 Two slightly different versions of what is known as the *T model* of the BJT. The circuit in **(a)** is a voltage-controlled current source representation and that in **(b)** is a current-controlled current source representation. These models explicitly show the emitter resistance r_e rather than the base resistance r_π featured in the hybrid-π model.

in two versions in Fig. 5.52. The model of Fig. 5.52(a) represents the BJT as a voltage-controlled current source with the control voltage being v_{be}. Here, however, the resistance between base and emitter, looking into the emitter, is explicitly shown. From Fig. 5.52(a) we see clearly that the model yields the correct expressions for i_c and i_e. For i_b we note that at the base node we have

$$\begin{aligned} i_b &= \frac{v_{be}}{r_e} - g_m v_{be} = \frac{v_{be}}{r_e}(1 - g_m r_e) \\ &= \frac{v_{be}}{r_e}(1-\alpha) = \frac{v_{be}}{r_e}\left(1 - \frac{\beta}{\beta+1}\right) \\ &= \frac{v_{be}}{(\beta+1)r_e} = \frac{v_{be}}{r_\pi} \end{aligned}$$

as should be the case.

If in the model of Fig. 5.52(a) the current of the controlled source is expressed in terms of the emitter current as follows:

$$\begin{aligned} g_m v_{be} &= g_m(i_e r_e) \\ &= (g_m r_e) i_e = \alpha i_e \end{aligned}$$

we obtain the alternative T model shown in Fig. 5.52(b). Here the BJT is represented as a current-controlled current source but with the control signal being i_e.

5.6.8 Application of the Small-Signal Equivalent Circuits

The availability of the small-signal BJT circuit models makes the analysis of transistor amplifier circuits a systematic process. The process consists of the following steps:

1. Determine the dc operating point of the BJT and in particular the dc collector current I_C.
2. Calculate the values of the small-signal model parameters: $g_m = I_C/V_T$, $r_\pi = \beta/g_m$, and $r_e = V_T/I_E \cong 1/g_m$.
3. Eliminate the dc sources by replacing each dc voltage source with a short circuit and each dc current source with an open circuit.
4. Replace the BJT with one of its small-signal equivalent circuit models. Although any one of the models can be used, one might be more convenient than the others for the particular circuit being analyzed. This point will be made clearer later in this chapter.
5. Analyze the resulting circuit to determine the required quantities (e.g., voltage gain, input resistance). The process will be illustrated by the following examples.

EXAMPLE 5.14

We wish to analyze the transistor amplifier shown in Fig. 5.53(a) to determine its voltage gain. Assume $\beta = 100$.

Solution

The first step in the analysis consists of determining the quiescent operating point. For this purpose we assume that $v_i = 0$. The dc base current will be

$$\begin{aligned} I_B &= \frac{V_{BB} - V_{BE}}{R_{BB}} \\ &\simeq \frac{3 - 0.7}{100} = 0.023 \text{ mA} \end{aligned}$$

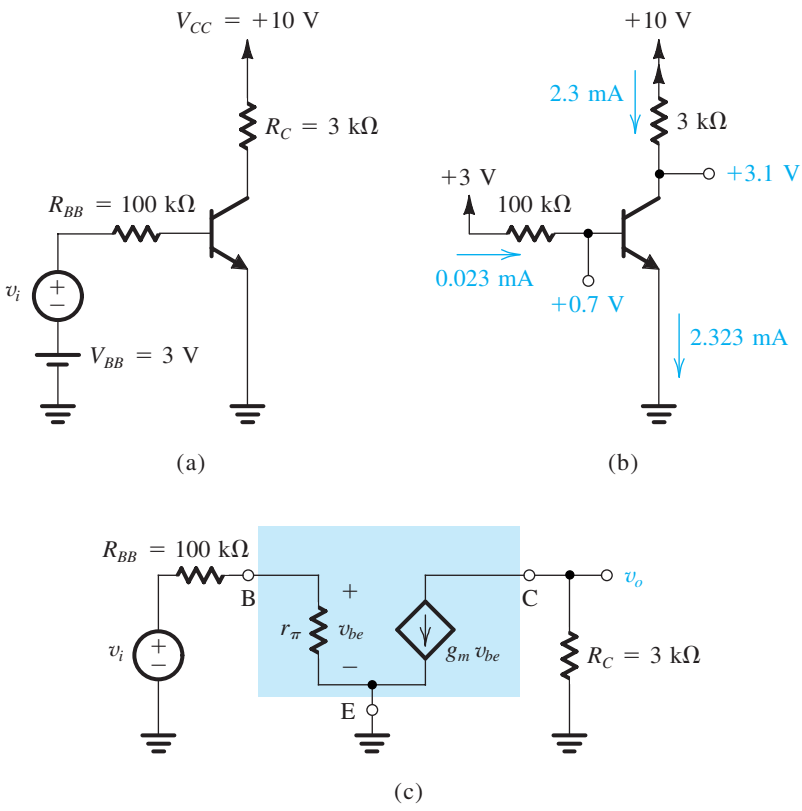


FIGURE 5.53 Example 5.14: **(a)** circuit; **(b)** dc analysis; **(c)** small-signal model.

The dc collector current will be

$$I_C = \beta I_B = 100 \times 0.023 = 2.3 \text{ mA}$$

The dc voltage at the collector will be

$$\begin{aligned} V_C &= V_{CC} - I_C R_C \\ &= +10 - 2.3 \times 3 = +3.1 \text{ V} \end{aligned}$$

Since V_B at +0.7 V is less than V_C, it follows that in the quiescent condition the transistor will be operating in the active mode. The dc analysis is illustrated in Fig. 5.53(b).

Having determined the operating point, we may now proceed to determine the small-signal model parameters:

$$r_e = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{(2.3/0.99) \text{ mA}} = 10.8 \ \Omega$$

$$g_m = \frac{I_C}{V_T} = \frac{2.3 \text{ mA}}{25 \text{ mV}} = 92 \text{ mA/V}$$

$$r_\pi = \frac{\beta}{g_m} = \frac{100}{92} = 1.09 \text{ k}\Omega$$

To carry out the small-signal analysis it is equally convenient to employ either of the two hybrid-π equivalent circuit models of Fig. 5.51. Using the first results in the amplifier equivalent

circuit given in Fig. 5.53(c). Note that no dc quantities are included in this equivalent circuit. It is most important to note that the dc supply voltage V_{CC} has been replaced by a *short circuit* in the signal equivalent circuit because the circuit terminal connected to V_{CC} will always have a constant voltage. That is, the signal voltage at this terminal will be zero. In other words, *a circuit terminal connected to a constant dc source can always be considered as a signal ground.*

Analysis of the equivalent circuit in Fig. 5.53(c) proceeds as follows:

$$\begin{aligned} v_{be} &= v_i \frac{r_\pi}{r_\pi + R_{BB}} \\ &= v_i \frac{1.09}{101.09} = 0.011\, v_i \end{aligned} \tag{5.105}$$

The output voltage v_o is given by

$$\begin{aligned} v_o &= -g_m v_{be} R_C \\ &= -92 \times 0.011\, v_i \times 3 = -3.04\, v_i \end{aligned}$$

Thus the voltage gain will be

$$A_v = \frac{v_o}{v_i} = -3.04 \text{ V/V} \tag{5.106}$$

where the minus sign indicates a phase reversal.

EXAMPLE 5.15

To gain more insight into the operation of transistor amplifiers, we wish to consider the waveforms at various points in the circuit analyzed in the previous example. For this purpose assume that v_i has a triangular waveform. First determine the maximum amplitude that v_i is allowed to have. Then, with the amplitude of v_i set to this value, give the waveforms of $i_B(t)$, $v_{BE}(t)$, $i_C(t)$, and $v_C(t)$.

Solution

One constraint on signal amplitude is the small-signal approximation, which stipulates that v_{be} should not exceed about 10 mV. If we take the triangular waveform v_{be} to be 20 mV peak-to-peak and work backward, Eq. (5.105) can be used to determine the maximum possible peak of v_i,

$$\hat{V}_i = \frac{\hat{V}_{be}}{0.011} = 0.91 \text{ V}$$

To check whether or not the transistor remains in the active mode with v_i having a peak value $\hat{V}_i = 0.91$ V, we have to evaluate the collector voltage. The voltage at the collector will consist of a triangular wave v_c superimposed on the dc value $V_C = 3.1$ V. The peak voltage of the triangular waveform will be

$$\hat{V}_c = \hat{V}_i \times \text{gain} = 0.91 \times 3.04 = 2.77 \text{ V}$$

It follows that when the output swings negative, the collector voltage reaches a minimum of $3.1 - 2.77 = 0.33$ V, which is lower than the base voltage by less than 0.4 V. Thus the transistor will remain in the active mode with v_i having a peak value of 0.91 V. Nevertheless, we will use a somewhat lower value for $\hat{V}_i$ of approximately 0.8 V, as shown in Fig. 5.54(a), and complete the analysis of this problem. The signal current in the base will be triangular, with a peak value $\hat{I}_b$ of

$$\hat{I}_b = \frac{\hat{V}_i}{R_{BB} + r_\pi} = \frac{0.8}{100 + 1.09} = 0.008 \text{ mA}$$

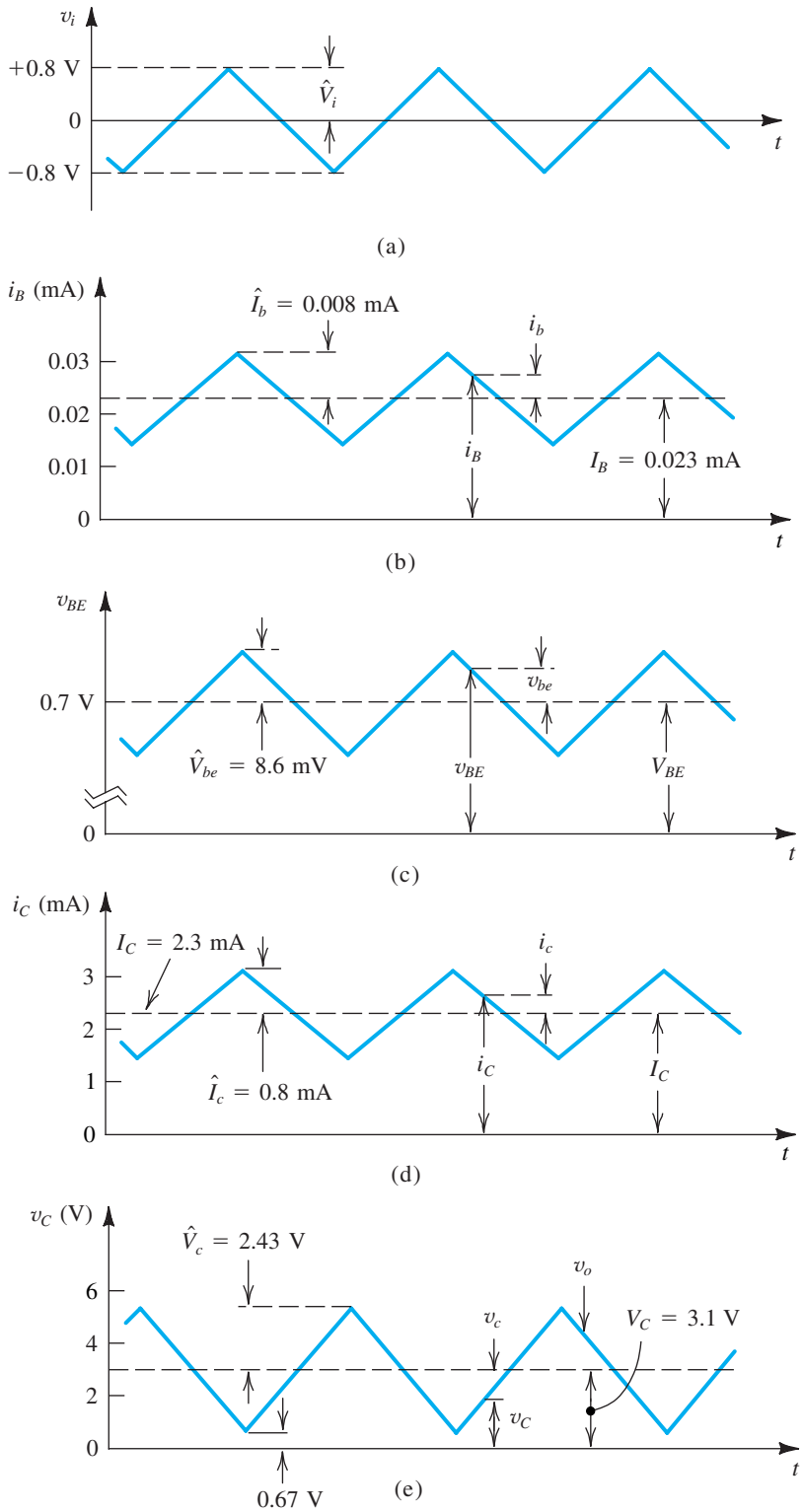


FIGURE 5.54 Signal waveforms in the circuit of Fig. 5.53.

This triangular-wave current will be superimposed on the quiescent base current I_B, as shown in Fig. 5.54(b). The base–emitter voltage will consist of a triangular-wave component superimposed on the dc V_{BE} that is approximately 0.7 V. The peak value of the triangular waveform will be

$$\hat{V}_{be} = \hat{V}_i \frac{r_\pi}{r_\pi + R_{BB}} = 0.8 \frac{1.09}{100 + 1.09} = 8.6 \text{ mV}$$

The total v_{BE} is sketched in Fig. 5.54(c).

The signal current in the collector will be triangular in waveform, with a peak value $\hat{I}_c$ given by

$$\hat{I}_c = \beta \hat{I}_b = 100 \times 0.008 = 0.8 \text{ mA}$$

This current will be superimposed on the quiescent collector current I_C (=2.3 mA), as shown in Fig. 5.54(d).

Finally, the signal voltage at the collector can be obtained by multiplying v_i by the voltage gain; that is,

$$\hat{V}_c = 3.04 \times 0.8 = 2.43 \text{ V}$$

Figure 5.54(e) shows a sketch of the total collector voltage v_C versus time. Note the phase reversal between the input signal v_i and the output signal v_c.

EXAMPLE 5.16

We need to analyze the circuit of Fig. 5.55(a) to determine the voltage gain and the signal waveforms at various points. The capacitor C is a coupling capacitor whose purpose is to couple the signal v_i to the emitter while blocking dc. In this way the dc bias established by V^+ and V^- together with R_E and R_C will not be disturbed when the signal v_i is connected. For the purpose of this example, C will be assumed to be very large and ideally infinite—that is, acting as a perfect short circuit at signal frequencies of interest. Similarly, another very large capacitor is used to couple the output signal v_o to other parts of the system.

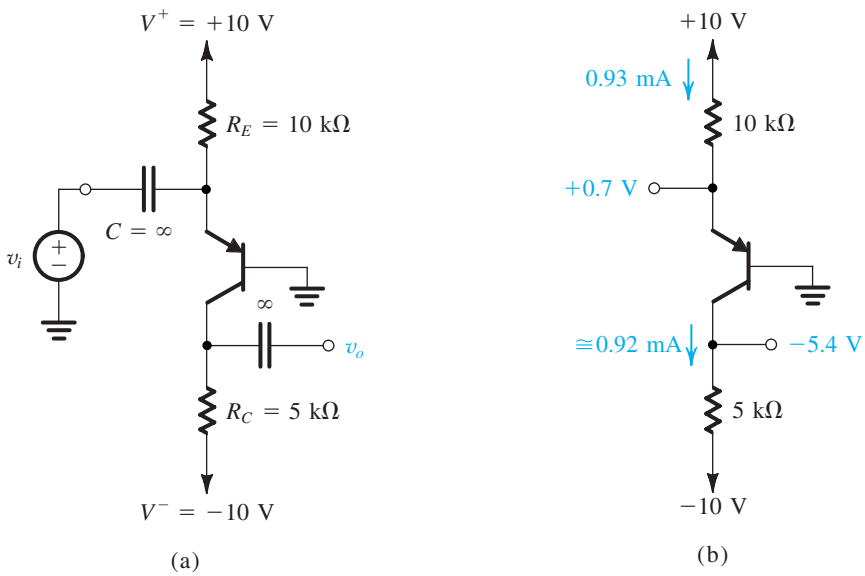
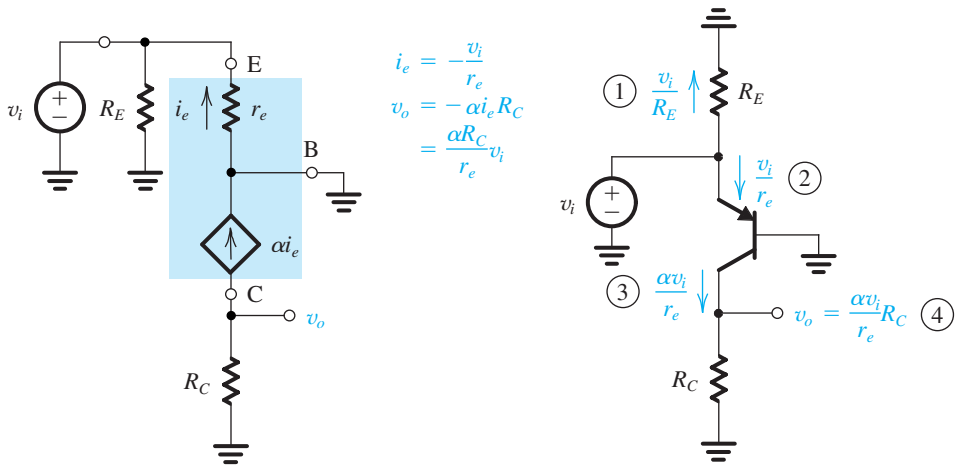


FIGURE 5.55 Example 5.16: **(a)** circuit; **(b)** dc analysis;



(c) (d)

FIGURE 5.55 *(Continued)* **(c)** small-signal model; **(d)** small-signal analysis performed directly on the circuit.

Solution

We shall start by determining the dc operating point as follows (see Fig. 5.55b):

$$I_E = \frac{+10 - V_E}{R_E} \simeq \frac{+10 - 0.7}{10} = 0.93 \text{ mA}$$

Assuming $\beta = 100$, then $\alpha = 0.99$, and

$$\begin{aligned} I_C &= 0.99 I_E = 0.92 \text{ mA} \\ V_C &= -10 + I_C R_C \\ &= -10 + 0.92 \times 5 = -5.4 \text{ V} \end{aligned}$$

Thus the transistor is in the active mode. Furthermore, the collector signal can swing from –5.4 V to +0.4 V (which is 0.4 V above the base voltage) without the transistor going into saturation. However, a negative 5.8-V swing in the collector voltage will (theoretically) cause the minimum collector voltage to be –11.2 V, which is more negative than the power-supply voltage. It follows that if we attempt to apply an input that results in such an output signal, the transistor will cut off and the negative peaks of the output signal will be clipped off, as illustrated in Fig. 5.56. The waveform in Fig. 5.56, however, is shown to be linear (except for the clipped peak); that is, the effect of the nonlinear i_C–v_{BE} characteristic is not taken into account. This is not correct, since if we are driving the transistor into cutoff at the negative signal peaks, then we will surely be exceeding the small-signal limit, as will be shown later.

Let us now proceed to determine the small-signal voltage gain. Toward that end, we eliminate the dc sources and replace the BJT with its T equivalent circuit of Fig. 5.52(b). Note that because the base is grounded, the T model is somewhat more convenient than the hybrid-π model. Nevertheless, identical results can be obtained using the latter.

Figure 5.55(c) shows the resulting small-signal equivalent circuit of the amplifier. The model parameters are

$$\alpha = 0.99$$

$$r_e = \frac{V_T}{I_E} = \frac{25 \text{ mV}}{0.93 \text{ mA}} = 27 \ \Omega$$

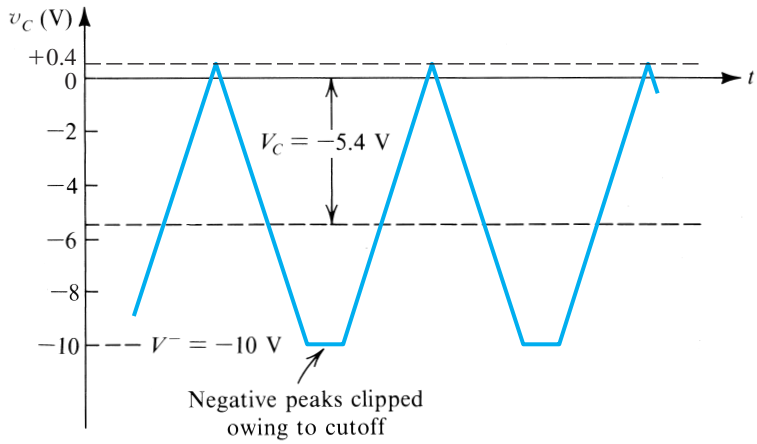


FIGURE 5.56 Distortion in output signal due to transistor cutoff. Note that it is assumed that no distortion due to transistor nonlinear characteristics is occurring.

Analysis of the circuit in Fig. 5.55(c) to determine the output voltage v_o and hence the voltage gain v_o/v_i is straightforward and is given in the figure. The result is

$$A_v = \frac{v_o}{v_i} = 183.3 \text{ V/V}$$

Note that the voltage gain is positive, indicating that the output is in phase with the input signal. This property is due to the fact that the input signal is applied to the emitter rather than to the base, as was done in Example 5.14. We should emphasize that the positive gain has nothing to do with the fact that the transistor used in this example is of the *pnp* type.

Returning to the question of allowable signal magnitude, we observe from Fig. 5.55(c) that $v_{eb} = v_i$. Thus, if small-signal operation is desired (for linearity), then the peak of v_i should be limited to approximately 10 mV. With $\hat{V}_i$ set to this value, as shown for a sine-wave input in Fig. 5.57,

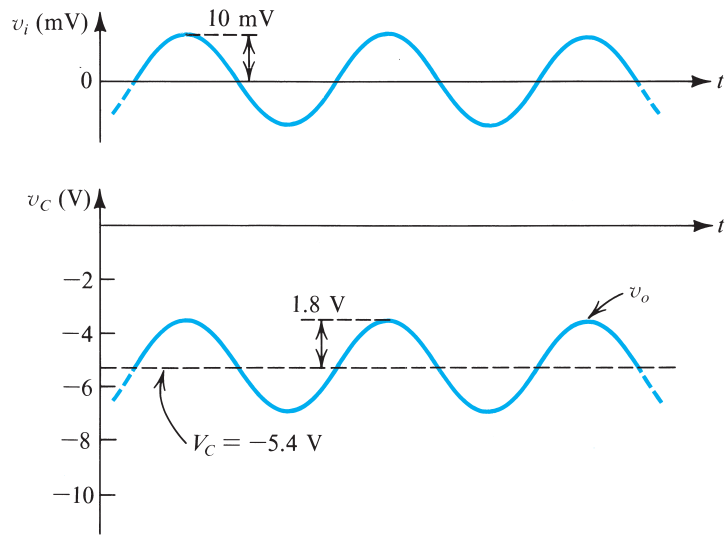


FIGURE 5.57 Input and output waveforms for the circuit of Fig. 5.55. Observe that this amplifier is noninverting, a property of the common-base configuration.

the peak amplitude at the collector, $\hat{V}_c$, will be

$$\hat{V}_c = 183.3 \times 0.01 = 1.833 \text{ V}$$

and the total instantaneous collector voltage $v_C(t)$ will be as depicted in Fig. 5.57(b).

EXERCISE

5.39 To increase the voltage gain of the amplifier analyzed in Example 5.16, the collector resistance R_C is increased to 7.5 kΩ. Find the new values of V_C, A_v, and the peak amplitude of the output sine wave corresponding to an input sine wave v_i of 10 mV peak.

Ans. –3.1 V; 275 V/V; 2.75 V

5.6.9 Performing Small-Signal Analysis Directly on the Circuit Diagram

In most cases one should explicitly replace each BJT with its small-signal model and analyze the resulting circuit, as we have done in the examples above. This systematic procedure is particularly recommended for beginning students. Experienced circuit designers, however, often perform a first-order analysis directly on the circuit. Figure 5.55(d) illustrates this process for the circuit we have just analyzed. The reader is urged to follow this direct analysis procedure (the steps are numbered). Observe that the equivalent circuit model is *implicitly* utilized; we are only saving the step of redrawing the circuit with the BJT replaced with its model. Direct analysis, however, has an additional very important benefit: It provides insight regarding the signal transmission through the circuit. Such insight can prove invaluable in design, particularly at the stage of selecting a circuit configuration appropriate for a given application.

5.6.10 Augmenting the Small-Signal Models to Account for the Early Effect

The Early effect, discussed in Section 5.2, causes the collector current to depend not only on v_{BE} but also on v_{CE}. The dependence on v_{CE} can be modeled by assigning a finite output resistance to the controlled current-source in the hybrid-π model, as shown in Fig. 5.58. The output resistance r_o was defined in Eq. (5.37); its value is given by $r_o = (V_A + V_{CE})/I_C \simeq V_A/I_C$, where V_A is the Early voltage and V_{CE} and I_C are the coordinates of the dc bias point. Note that in the models of Fig. 5.58 we have renamed v_{be} as v_π, in order to conform with the literature.

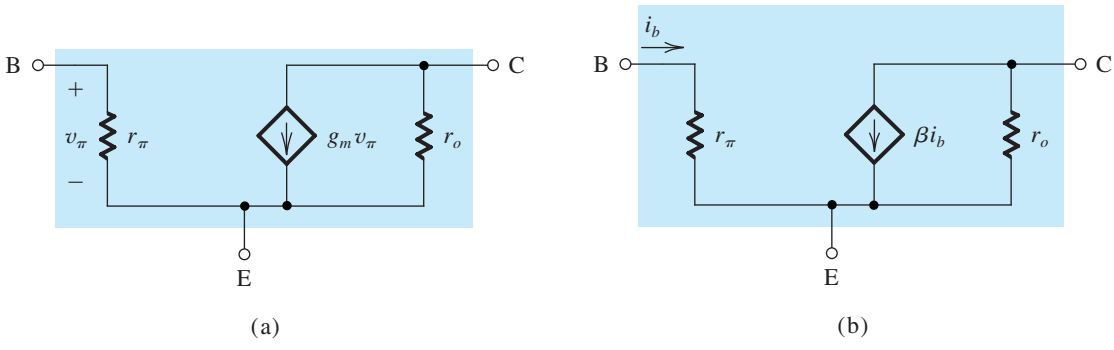


FIGURE 5.58 The hybrid-π small-signal model, in its two versions, with the resistance r_o included.

The question arises as to the effect of r_o on the operation of the transistor as an amplifier. In amplifier circuits in which the emitter is grounded (as in the circuit of Fig. 5.53), r_o simply appears in parallel with R_C. Thus, if we include r_o in the equivalent circuit of Fig. 5.53(c), for example, the output voltage v_o becomes

$$v_o = -g_m v_{be}(R_C \,//\, r_o)$$

Thus the gain will be somewhat reduced. Obviously if $r_o \gg R_C$, the reduction in gain will be negligible, and one can ignore the effect of r_o. In general, in such a configuration r_o can be neglected if it is greater than $10R_C$.

When the emitter of the transistor is not grounded, including r_o in the model can complicate the analysis. We will make comments regarding r_o and its inclusion or exclusion on frequent occasions throughout the book. We should also note that in integrated-circuit BJT amplifiers, r_o plays a dominant role, as will be seen in Chapter 6. Of course, if one is performing an accurate analysis of an almost-final design using computer-aided analysis, then r_o can be easily included (see Section 5.11).

Finally, it should be noted that either of the T models in Fig. 5.52 can be augmented to account for the Early effect by including r_o between collector and emitter.

5.6.11 Summary

The analysis and design of BJT amplifier circuits is greatly facilitated if the relationships between the various small-signal model parameters are at your fingertips. For easy reference, these are summarized in Table 5.4. Over time, however, we expect the reader to be able to recall these from memory.

EXERCISE

5.40 The transistor in Fig. E5.40 is biased with a constant current source $I = 1$ mA and has $\beta = 100$ and $V_A = 100$ V. (a) Find the dc voltages at the base, emitter, and collector. (b) Find g_m, r_π, and r_o. (c) If terminal Z is connected to ground, X to a signal source v_s with a source resistance $R_s = 2$ kΩ, and Y to an 8-kΩ load resistance, use the hybrid-π model of Fig. 5.58(a), to draw the small-signal equivalent circuit of the amplifier. (Note that the current source I should be replaced with an open circuit.) Calculate the overall voltage gain v_y/v_s. If r_o is neglected what is the error in estimating the gain magnitude? (*Note:* An infinite capacitance is used to indicate that the capacitance is sufficiently large that it acts as a short circuit at all signal frequencies of interest. However, the capacitor still blocks dc.)

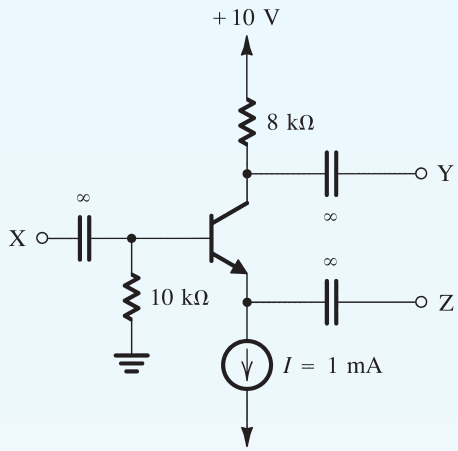


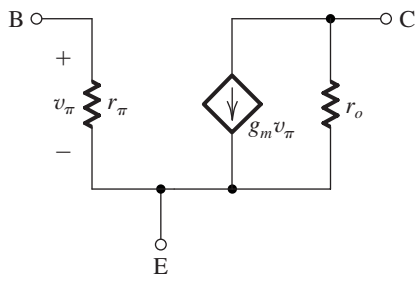
FIGURE E5.40

Ans. (a) –0.1 V, –0.8 V, +2 V; (b) 40 mA/V, 2.5 kΩ, 100 kΩ; (c) –77 V/V, +3.9%

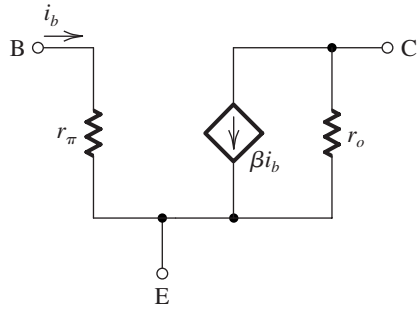
TABLE 5.4 Small-Signal Models of the BJT

Hybrid-π Model

- $(g_m v_\pi)$ Version

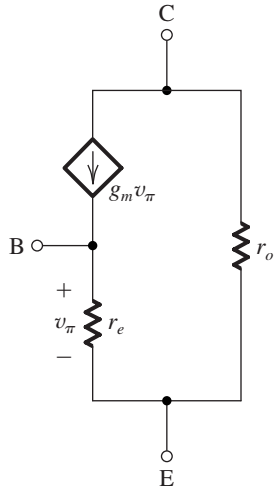


- (βi_b) Version

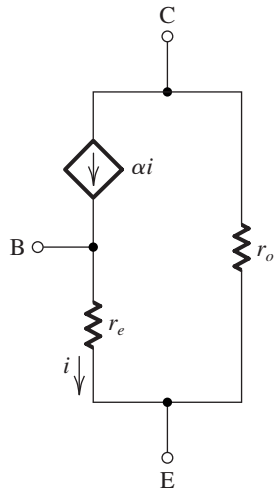


T Model

- $(g_m v_\pi)$ Version



- (αi) Version



Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\left(\frac{V_T}{I_C}\right) \qquad r_\pi = \frac{V_T}{I_B} = \beta\left(\frac{V_T}{I_C}\right) \qquad r_o = \frac{V_A}{I_C}$$

In Terms of g_m

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In Terms of r_e

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta+1)r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships Between α and β

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad \beta + 1 = \frac{1}{1-\alpha}$$

5.7 SINGLE-STAGE BJT AMPLIFIERS

We have studied the large-signal operation of BJT amplifiers in Section 5.3 and identified the region over which a properly biased transistor can be operated as a linear amplifier for small signals. Methods for dc biasing the BJT were studied in Section 5.5, and a detailed study of the small-signal amplifier operation was presented in Section 5.6. We are now ready to consider practical transistor amplifiers, and we will do so in this section for circuits suitable for discrete-circuit fabrication. The design of integrated-circuit BJT amplifiers will be studied in Chapter 6.

There are basically three configurations for implementing single-stage BJT amplifiers: the common-emitter, the common-base, and the common-collector configurations. All three are studied below, utilizing the same basic structure with the same biasing arrangement.

5.7.1 The Basic Structure

Figure 5.59 shows the basic circuit that we shall utilize to implement the various configurations of BJT amplifiers. Among the various biasing schemes possible for discrete BJT amplifiers (Section 5.5), we have selected, for simplicity and effectiveness, the one employing constant-current biasing. Figure 5.59 indicates the dc currents in all branches and the dc voltages at all nodes. We should note that one would want to select a large value for R_B in order to keep the input resistance at the base large. However, we also want to limit the dc voltage drop across R_B and even more importantly the variability of this dc voltage resulting from the variation in β values among transistors of the same type. The dc voltage V_B determines the allowable signal swing at the collector.

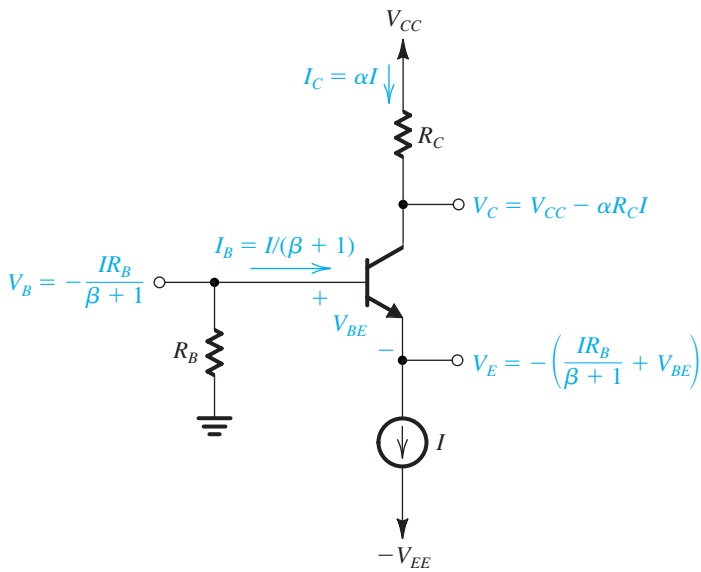


FIGURE 5.59 Basic structure of the circuit used to realize single-stage, discrete-circuit BJT amplifier configurations.

EXERCISE

5.41 Consider the circuit of Fig. 5.59 for the case $V_{CC} = V_{EE} = 10$ V, $I = 1$ mA, $R_B = 100$ kΩ, $R_C = 8$ kΩ, and $\beta = 100$. Find all dc currents and voltages. What are the allowable signal swings at the collector in both directions? How do these values change as β is changed to 50? To 200? Evaluate the values of the BJT small-signal parameters at the bias point (with $\beta = 100$). The Early voltage $V_A = 100$ V.

Ans. See Fig. E5.41. Signal swing: for $\beta = 100$, +8 V, –3.4 V; for $\beta = 50$, +8 V, –4.4 V; for $\beta = 200$, +8 V, –2.9 V.

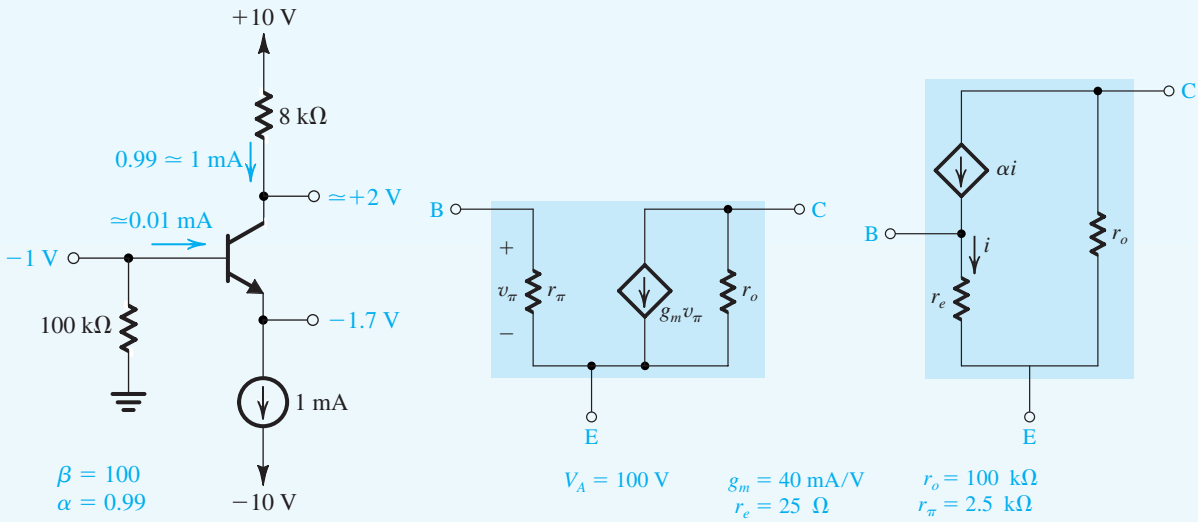


FIGURE E5.41

5.7.2 Characterizing BJT Amplifiers[9]

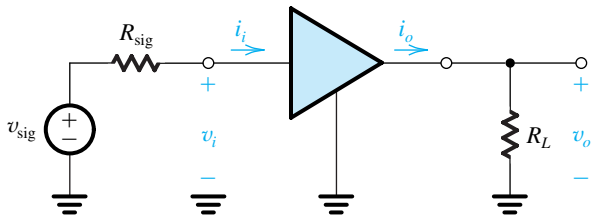
As we begin our study of BJT amplifier circuits, it is important to know how to characterize the performance of amplifiers as circuit building blocks. An introduction to this subject was presented in Section 1.5. However, the material of Section 1.5 was limited to **unilateral amplifiers.** A number of the amplifier circuits we shall study in this book are not unilateral; that is, they have internal feedback that may cause their input resistance to depend on the load resistance. Similarly, internal feedback may cause the output resistance to depend on the value of the resistance of the signal source feeding the amplifier. To accommodate **nonunilateral amplifiers,** we present in Table 5.5 a general set of parameters and equivalent circuits that we will employ in characterizing and comparing transistor amplifiers. A number of remarks are in order:

1. The amplifier in Table 5.5 is shown fed with a signal source having an open-circuit voltage v_{sig} and an internal resistance R_{sig}. These can be the parameters of an actual signal source or the Thévenin equivalent of the output circuit of another amplifier stage preceding the one under study in a cascade amplifier. Similarly, R_L can be an actual load resistance or the input resistance of a succeeding amplifier stage in a cascade amplifier.

[9] This section is identical to Section 4.7.2. Readers who studied Section 4.7.2 can skip this section.

TABLE 5.5 Characteristic Parameters of Amplifiers

Circuit



Definitions

- Input resistance with no load:

$$R_i \equiv \left.\frac{v_i}{i_i}\right|_{R_L=\infty}$$

- Input resistance:

$$R_{in} \equiv \frac{v_i}{i_i}$$

- Open-circuit voltage gain:

$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{R_L=\infty}$$

- Voltage gain:

$$A_v \equiv \frac{v_o}{v_i}$$

- Short-circuit current gain:

$$A_{is} \equiv \left.\frac{i_o}{i_i}\right|_{R_L=0}$$

- Current gain:

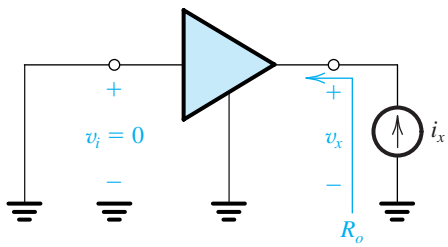
$$A_i \equiv \frac{i_o}{i_i}$$

- Short-circuit transconductance:

$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{R_L=0}$$

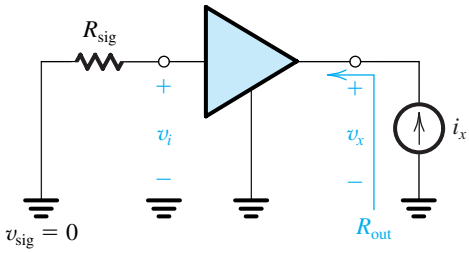
- Output resistance of amplifier proper:

$$R_o \equiv \left.\frac{v_x}{i_x}\right|_{v_i=0}$$



- Output resistance:

$$R_{\text{out}} \equiv \left.\frac{v_x}{i_x}\right|_{v_{\text{sig}}=0}$$



- Open-circuit overall voltage gain:

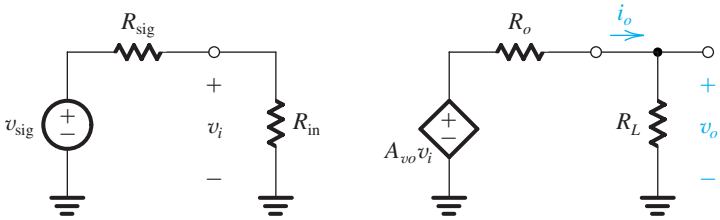
$$G_{vo} \equiv \left.\frac{v_o}{v_{\text{sig}}}\right|_{R_L=\infty}$$

- Overall voltage gain:

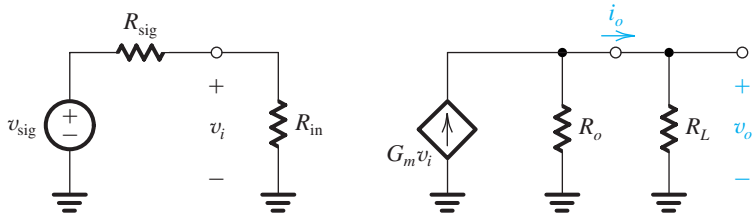
$$G_v \equiv \frac{v_o}{v_{\text{sig}}}$$

Equivalent Circuits

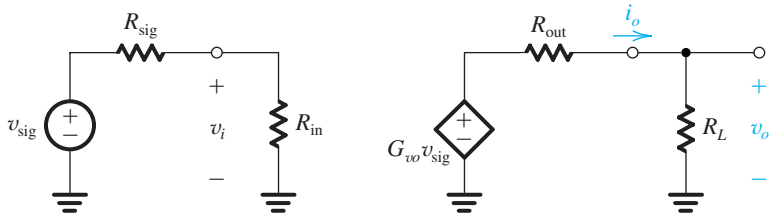
- A:



- B:



- C:



(Continued)

TABLE 5.5 *(Continued)*

Relationships

- $\frac{v_i}{v_{\text{sig}}} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}}$
- $A_v = A_{vo}\frac{R_L}{R_L + R_o}$
- $A_{vo} = G_m R_o$
- $G_v = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} A_{vo} \frac{R_L}{R_L + R_o}$
- $G_{vo} = \frac{R_i}{R_i + R_{\text{sig}}} A_{vo}$
- $G_v = G_{vo}\frac{R_L}{R_L + R_{\text{out}}}$

2. Parameters R_i, R_o, A_{vo}, A_{is}, and G_m pertain to the *amplifier proper;* that is, they do *not* depend on the values of R_{sig} and R_L. By contrast, R_{in}, R_{out}, A_v, A_i, G_{vo}, and G_v may depend on one or both of R_{sig} and R_L. Also, observe the relationships of related pairs of these parameters; for instance, $R_i = R_{\text{in}}|_{R_L=\infty}$, and $R_o = R_{\text{out}}|_{R_{\text{sig}}=0}$.
3. As mentioned above, for nonunilateral amplifiers, R_{in} may depend on R_L, and R_{out} may depend on R_{sig}. One such amplifier circuit is studied in Section 5.7.6. No such dependencies exist for unilateral amplifiers, for which $R_{\text{in}} = R_i$ and $R_{\text{out}} = R_o$.
4. The *loading* of the amplifier on the signal source is determined by the input resistance R_{in}. The value of R_{in} determines the current i_i that the amplifier draws from the signal source. It also determines the proportion of the signal v_{sig} that appears at the input of the amplifier proper, that is, v_i.
5. When evaluating the gain A_v from the open-circuit value A_{vo}, R_o is the output resistance to use. This is because A_v is based on feeding the amplifier with an ideal voltage signal v_i. This should be evident from Equivalent Circuit A in Table 5.5. On the other hand, if we are evaluating the overall voltage gain G_v from its open-circuit value G_{vo}, the output resistance to use is R_{out}. This is because G_v is based on feeding the amplifier with v_{sig}, which has an internal resistance R_{sig}. This should be evident from Equivalent Circuit C in Table 5.5.
6. We urge the reader to carefully examine and reflect on the definitions and the six relationships presented in Table 5.5. Example 5.17 should help in this regard.

EXAMPLE 5.17

A transistor amplifier is fed with a signal source having an open-circuit voltage v_{sig} of 10 mV and an internal resistance R_{sig} of 100 kΩ. The voltage v_i at the amplifier input and the output voltage v_o are measured both without and with a load resistance R_L = 10 kΩ connected to the amplifier output. The measured results are as follows:

	v_i (mV)	v_o (mV)
Without R_L	9	90
With R_L connected	8	70

Find all the amplifier parameters.

Solution

First, we use the data obtained for $R_L = \infty$ to determine

$$A_{vo} = \frac{90}{9} = 10 \text{ V/V}$$

and

$$G_{vo} = \frac{90}{10} = 9 \text{ V/V}$$

Now, since

$$G_{vo} = \frac{R_i}{R_i + R_{\text{sig}}} A_{vo}$$

$$9 = \frac{R_i}{R_i + 100} \times 10$$

which gives

$$R_i = 900 \text{ k}\Omega$$

Next, we use the data obtained when $R_L = 10$ kΩ is connected to the amplifier output to determine

$$A_v = \frac{70}{8} = 8.75 \text{ V/V}$$

and

$$G_v = \frac{70}{10} = 7 \text{ V/V}$$

The values of A_v and A_{vo} can be used to determine R_o as follows:

$$A_v = A_{vo} \frac{R_L}{R_L + R_o}$$

$$8.75 = 10 \frac{10}{10 + R_o}$$

which gives

$$R_o = 1.43 \text{ k}\Omega$$

Similarly, we use the values of G_v and G_{vo} to determine R_{out} from

$$G_v = G_{vo} \frac{R_L}{R_L + R_{\text{out}}}$$

$$7 = 9 \frac{10}{10 + R_{\text{out}}}$$

resulting in

$$R_{\text{out}} = 2.86 \text{ k}\Omega$$

The value of R_{in} can be determined from

$$\frac{v_i}{v_{\text{sig}}} = \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}}$$

Thus,

$$\frac{8}{10} = \frac{R_{\text{in}}}{R_{\text{in}} + 100}$$

which yields

$$R_{\text{in}} = 400\ \text{k}\Omega$$

The short-circuit transconductance G_m can be found as follows:

$$G_m = \frac{A_{vo}}{R_o} = \frac{10}{1.43} = 7\ \text{mA/V}$$

and the current gain A_i can be determined as follows:

$$A_i = \frac{v_o/R_L}{v_i/R_{\text{in}}} = \frac{v_o}{v_i}\frac{R_{\text{in}}}{R_L}$$

$$= A_v\frac{R_{\text{in}}}{R_L} = 8.75 \times \frac{400}{10} = 350\ \text{A/A}$$

Finally, we determine the short-circuit current gain A_{is} as follows. From Equivalent Circuit A, the short-circuit output current is

$$i_{osc} = A_{vo}v_i/R_o \tag{5.107}$$

However, to determine v_i we need to know the value of R_{in} obtained with $R_L = 0$. Toward this end, note that from Equivalent Circuit C, the output short-circuit current can be found as

$$i_{osc} = G_{vo}v_{\text{sig}}/R_{\text{out}} \tag{5.108}$$

Now, equating the two expressions for i_{osc} and substituting for G_{vo} by

$$G_{vo} = \frac{R_i}{R_i + R_{\text{sig}}}A_{vo}$$

and for v_i from

$$v_i = v_{\text{sig}}\frac{R_{\text{in}}|_{R_L=0}}{R_{\text{in}}|_{R_L=0} + R_{\text{sig}}}$$

results in

$$R_{\text{in}}|_{R_L=0} = R_{\text{sig}}\Big/\left[\left(1 + \frac{R_{\text{sig}}}{R_i}\right)\left(\frac{R_{\text{out}}}{R_o}\right) - 1\right]$$

$$= 81.8\ \text{k}\Omega$$

We now can use

$$i_{osc} = A_{vo}i_iR_{\text{in}}|_{R_L=0}/R_o$$

to obtain

$$A_{is} = \frac{i_{osc}}{i_i} = 10 \times 81.8/1.43 = 572\ \text{A/A}$$

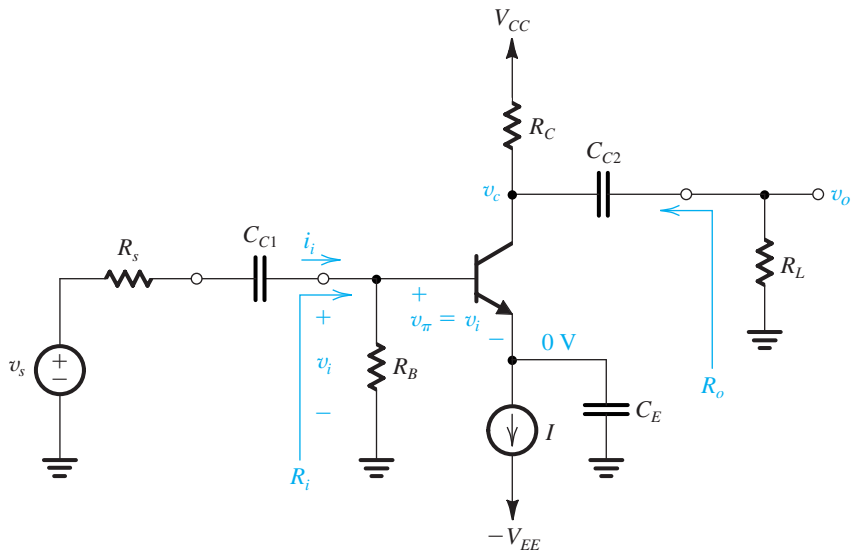
EXERCISE

5.42 Refer to the amplifier of Example 5.17. (a) If R_{sig} is doubled, find the values for R_{in}, G_v, and R_{out}. (b) Repeat for R_L doubled (but R_{sig} unchanged; i.e., 100 kΩ). (c) Repeat for both R_{sig} and R_L doubled.

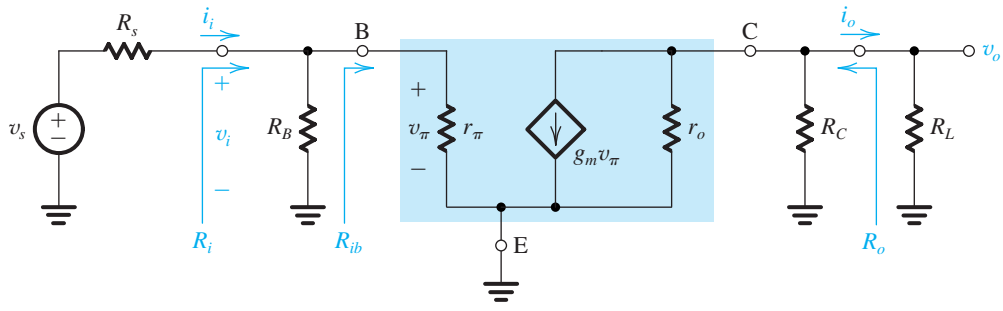
Ans. (a) 400 kΩ, 5.83 V/V, 4.03 kΩ; (b) 538 kΩ, 7.87 V/V, 2.86 kΩ; (c) 538 kΩ, 6.8 V/V, 4.03 kΩ

5.7.3 The Common-Emitter (CE) Amplifier

The CE configuration is the most widely used of all BJT amplifier circuits. Figure 5.60(a) shows a CE amplifier implemented using the circuit of Fig. 5.59. To establish a **signal ground** (or an **ac ground,** as it is sometimes called) at the emitter, a large capacitor C_E, usually in the μF or tens of μF range, is connected between emitter and ground. This capacitor



(a)



(b)

FIGURE 5.60 **(a)** A common-emitter amplifier using the structure of Fig. 5.59. **(b)** Equivalent circuit obtained by replacing the transistor with its hybrid-π model.

is required to provide a very low impedance to ground (ideally, zero impedance; i.e., in effect, a short circuit) at all signal frequencies of interest. In this way, the emitter signal current passes through C_E to ground and thus *bypasses* the output resistance of the current source I (and any other circuit component that might be connected to the emitter); hence C_E is called a **bypass capacitor.** Obviously, the lower the signal frequency, the less effective the bypass capacitor becomes. This issue will be studied in Section 5.9. For our purposes here we shall assume that C_E is acting as a perfect short circuit and thus is establishing a zero signal voltage at the emitter.

In order not to disturb the dc bias currents and voltages, the signal to be amplified, shown as a voltage source v_{sig} with an internal resistance R_{sig}, is connected to the base through a large capacitor C_{C1}. Capacitor C_{C1}, known as a **coupling capacitor,** is required to act as a perfect short circuit at all signal frequencies of interest while blocking dc. Here again we shall assume this to be the case and defer discussion of imperfect signal coupling as a result of the rise of the impedance of C_{C1} at low frequencies to Section 5.9. At this point we should point out that in situations where the signal source can provide a dc path for the dc base current I_B without significantly changing the bias point we may connect the source directly to the base, thus dispensing with C_{C1} as well as R_B. Eliminating R_B has the added beneficial effect of raising the input resistance of the amplifier.

The voltage signal resulting at the collector, v_c, is coupled to the load resistance R_L via another coupling capacitor C_{C2}. We shall assume that C_{C2} also acts a perfect short circuit at all signal frequencies of interest; thus the output voltage $v_o = v_c$. Note that R_L can be an actual load resistor to which the amplifier is required to provide its output voltage signal, or it can be the input resistance of a subsequent amplifier stage in cases where more than one stage of amplification is needed. (We will study multistage amplifiers in Chapter 7).

To determine the terminal characteristics of the CE amplifier, that is, its input resistance, voltage gain, and output resistance, we replace the BJT with its hybrid-π small-signal model. The resulting small-signal equivalent circuit of the CE amplifier is shown in Fig. 5.60(b). We observe at the outset that this amplifier is unilateral and thus $R_{\text{in}} = R_i$ and $R_{\text{out}} = R_o$. Analysis of this circuit is straightforward and proceeds in a step-by-step manner, from the signal source to the amplifier load. At the amplifier input we have

$$R_{\text{in}} \equiv \frac{v_i}{i_i} = R_B \parallel R_{ib} \tag{5.109}$$

where R_{ib} is the input resistance looking into the base. Since the emitter is grounded,

$$R_{ib} = r_\pi \tag{5.110}$$

Normally, we select $R_B \gg r_\pi$, with the result that

$$R_{\text{in}} \cong r_\pi \tag{5.111}$$

Thus, we note that the input resistance of the CE amplifier will typically be a few kilohms, which can be thought of as low to moderate. The fraction of source signal v_{sig} that appears across the input terminals of the amplifier proper can be found from

$$v_i = v_{\text{sig}} \frac{R_{\text{in}}}{R_{\text{in}} + R_{\text{sig}}} \tag{5.112}$$

$$= v_{\text{sig}} \frac{(R_B \parallel r_\pi)}{(R_B + r_\pi) + R_{\text{sig}}} \tag{5.113}$$

which for $R_B \gg r_\pi$ becomes

$$v_i \cong v_{\text{sig}} \frac{r_\pi}{r_\pi + R_{\text{sig}}} \tag{5.114}$$

Next we note that

$$v_\pi = v_i \tag{5.115}$$

At the output of the amplifier we have

$$v_o = -g_m v_\pi (r_o \parallel R_C \parallel R_L)$$

Replacing v_π by v_i we can write for the voltage gain of the amplifier proper; that is, the voltage gain from base to collector,

$$A_v = -g_m (r_o \parallel R_C \parallel R_L) \tag{5.116}$$

This equation simply says that the voltage gain from base to collector is found by multiplying g_m by the total resistance between collector and ground. The open-circuit voltage gain A_{vo} can be obtained by setting $R_L = \infty$ in Eq. (5.116); thus,

$$A_{vo} = -g_m (r_o \parallel R_C) \tag{5.117}$$

from which we note that the effect of r_o is simply to reduce the gain, usually only slightly since typically $r_o \gg R_C$, resulting in

$$A_{vo} \cong -g_m R_C \tag{5.118}$$

The output resistance R_{out} can be found from the equivalent circuit of Fig. 5.60(b) by looking back into the output terminal while short-circuiting the source v_{sig}. Since this will result in $v_\pi = 0$, we see that

$$R_{\text{out}} = R_C \parallel r_o \tag{5.119}$$

Thus r_o reduces the output resistance of the amplifier, again usually only slightly since typically $r_o \gg R_C$ and

$$R_{\text{out}} \cong R_C \tag{5.120}$$

Recalling that for this unilateral amplifier $R_o = R_{\text{out}}$, we can utilize A_{vo} and R_o to obtain the voltage gain A_v corresponding to any particular R_L,

$$A_v = A_{vo} \frac{R_L}{R_L + R_o}$$

The reader can easily verify that this approach does in fact lead to the expression for A_v in Eq. (5.116), which we have derived directly.

The overall voltage gain from source to load, G_v, can be obtained by multiplying (v_i / v_{sig}) from Eq. (5.114) by A_v from Eq. (5.116),

$$G_v = -\frac{(R_B \parallel r_\pi)}{(R_B \parallel r_\pi) + R_{\text{sig}}} g_m (r_o \parallel R_C \parallel R_L) \tag{5.121}$$

For the case $R_B \gg r_\pi$, this expression simplifies to

$$G_v \cong -\frac{\beta(R_C \parallel R_L \parallel r_o)}{r_\pi + R_{\text{sig}}} \tag{5.122}$$

From this expression we note that if $R_s \gg r_\pi$, the overall gain will be highly dependent on β. This is not a desirable property since β varies considerably between units of the same transistor type. At the other extreme, if $R_s \ll r_\pi$, we see that the expression for the overall voltage gain reduces to

$$G_v \cong -g_m(R_C \parallel R_L \parallel r_o) \tag{5.123}$$

which is the gain A_v; in other words, when R_s is small, the overall voltage gain is almost equal to the gain of the CE circuit proper, which is independent of β. Typically a CE amplifier can realize a voltage gain on the order of a few hundred, which is very significant. It follows that the CE amplifier is used to realize the bulk of the voltage gain required in a given amplifier design problem. Unfortunately, however, as we shall see in Section 5.9, the high-frequency response of the CE amplifier can be rather limited.

Before leaving the CE amplifier, we wish to evaluate its short-circuit current gain, A_{is}. This can be easily done by referring to the amplifier equivalent circuit in Fig. 5.60(b). When R_L is short circuited, the current through it will be equal to $-g_m v_\pi$,

$$i_{os} = -g_m v_\pi$$

Since v_π is related to i_i by

$$v_\pi = v_i = i_i R_{\text{in}}$$

the short-circuit current gain can be found as

$$A_{is} \equiv \frac{i_{os}}{i_i} = -g_m R_{\text{in}} \tag{5.124}$$

Substituting $R_{\text{in}} = R_B \parallel r_\pi$ we can see that in the case $R_B \gg r_\pi$, $|A_{is}|$ reduces to β, which is to be expected since β is, by definition, the short-circuit current gain of the common-emitter configuration.

In conclusion, the common-emitter configuration can provide large voltage and current gains, but R_{in} is relatively low and R_{out} is relatively high.

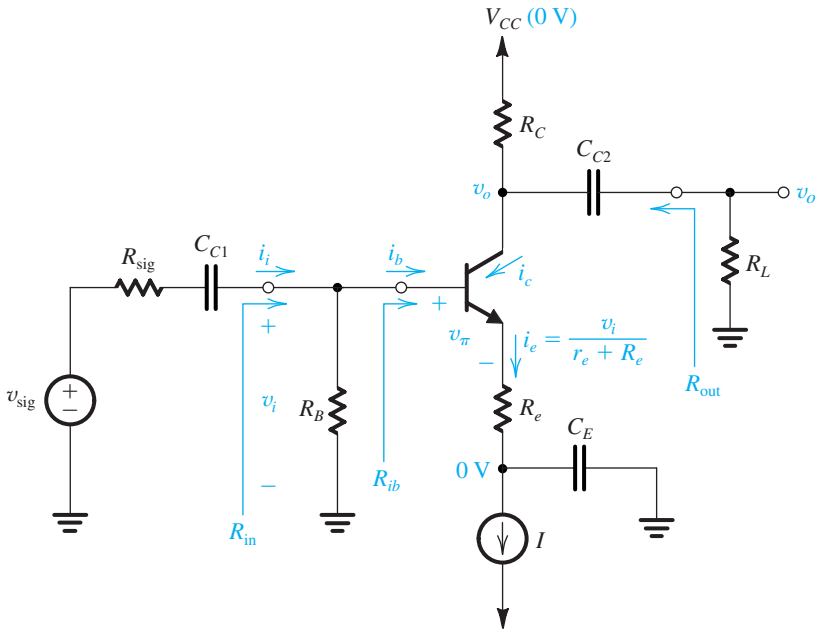
EXERCISE

5.43 Consider the CE amplifier of Fig. 5.60(a) when biased as in Exercise 5.41. In particular, refer to Fig. E5.41 for the bias currents and the values of the elements of the BJT model at the bias point. Evaluate R_{in} (without and with R_B taken into account), A_{vo} (without and with r_o taken into account), R_{out} (without and with r_o taken into account), and A_{is} (without and with R_B taken into account). For $R_L = 5$ kΩ, find A_v. If $R_s = 5$ kΩ, find the overall voltage gain G_v. If the sine-wave v_π is to be limited to 5 mV peak, what is the maximum allowed peak amplitude of v_{sig} and the corresponding peak amplitude of v_o.

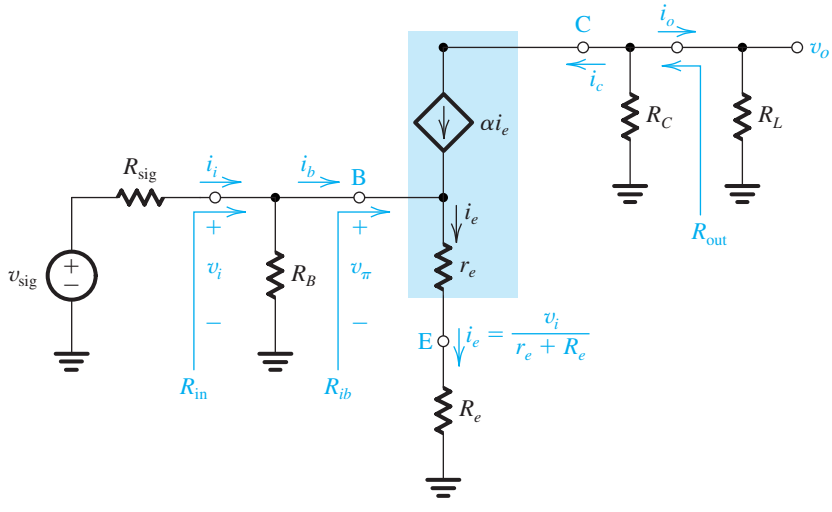
Ans. 2.5 kΩ, 2.4 kΩ; –320 V/V, –296 V/V; 8 kΩ, 7.4 kΩ; –100 A/A, –98 A/A; –119 V/V; –39 V/V; 15 mV; 0.6 V

5.7.4 The Common-Emitter Amplifier with an Emitter Resistance

Including a resistance in the signal path between emitter and ground, as shown in Fig. 5.61(a), can lead to significant changes in the amplifier characteristics. Thus such a resistor can be utilized by the designer as an effective design tool for tailoring the amplifier characteristics to fit the design requirements.



(a)



(b)

FIGURE 5.61 **(a)** A common-emitter amplifier with an emitter resistance R_e. **(b)** Equivalent circuit obtained by replacing the transistor with its T model.

Analysis of the circuit in Fig. 5.61(a) can be performed by replacing the BJT with one of its small-signal models. Although any one of the models of Figs. 5.51 and 5.52 can be used, the most convenient for this application is one of the two T models. This is because we have a resistance R_e in the emitter that will appear in series with the emitter resistance r_e of the T model and can thus be added to it, simplifying the analysis considerably. In fact, whenever there is a resistance in the emitter lead, the T model should prove more convenient to use than the hybrid-π model.

Replacing the BJT with the T model of Fig. 5.52(b) results in the amplifier small-signal equivalent-circuit model shown in Fig. 5.61(b). Note that we have *not* included the BJT output resistance r_o; including r_o complicates the analysis considerably. Since for the discrete amplifier at hand it turns out that the effect of r_o on circuit performance is small, we shall not include it in the analysis. This is not the case, however, for the IC version of this circuit, and we shall indeed take r_o into account in the analysis in Chapter 6.

To determine the amplifier input resistance R_{in}, we note from Fig. 5.61(b) that R_{in} is the parallel equivalent of R_B and the input resistance at the base R_{ib},

$$R_{\text{in}} = R_B \parallel R_{ib} \tag{5.125}$$

The input resistance at the base R_{ib} can be found from

$$R_{ib} \equiv \frac{v_i}{i_b}$$

where

$$i_b = (1-\alpha)i_e = \frac{i_e}{\beta+1}$$

and

$$i_e = \frac{v_i}{r_e + R_e} \tag{5.126}$$

Thus,

$$R_{ib} = (\beta+1)(r_e + R_e) \tag{5.127}$$

This is a very important result. It says that *the input resistance looking into the base is $(\beta+1)$ times the total resistance in the emitter*. Multiplication by the factor $(\beta+1)$ is known as the **resistance-reflection rule.** The factor $(\beta+1)$ arises because the base current is $1/(\beta+1)$ times the emitter current. The expression for R_{ib} in Eq. (5.127) shows clearly that including a resistance R_e in the emitter can substantially increase R_{ib}. Indeed the value of R_{ib} is increased by the ratio

$$\begin{aligned}\frac{R_{ib}\,(\text{with } R_e \text{ included})}{R_{ib}\,(\text{without } R_e)} &= \frac{(\beta+1)(r_e+R_e)}{(\beta+1)r_e} \\ &= 1 + \frac{R_e}{r_e} \cong 1 + g_m R_e \end{aligned} \tag{5.128}$$

Thus the circuit designer can use the value of R_e to control the value of R_{ib} and hence R_{in}. Of course, for this control to be effective, R_B must be much larger than R_{ib}; in other words, R_{ib} must dominate the input resistance.

To determine the voltage gain A_v, we see from Fig. 5.61(b) that

$$\begin{aligned} v_o &= -i_c(R_C \parallel R_L) \\ &= -\alpha i_e(R_C \parallel R_L) \end{aligned} \tag{5.129}$$

Substituting for i_e from Eq. (5.126) gives

$$A_v \equiv \frac{v_o}{v_i} = -\frac{\alpha(R_C \parallel R_L)}{r_e + R_e}$$

Since $\alpha \cong 1$,

$$A_v \cong -\frac{R_C \parallel R_L}{r_e + R_e} \tag{5.130}$$

This simple relationship is very useful and is definitely worth remembering: *The voltage gain from base to collector is equal to the ratio of the total resistance in the collector to the total resistance in the emitter.* This statement is a general one and applies to any amplifier circuit. The open-circuit voltage gain A_{vo} can be found by setting $R_L = \infty$ in Eq. (5.129),

$$A_{vo} = -\frac{\alpha R_C}{r_e + R_e} \tag{5.131}$$

which can be expressed alternatively as

$$A_{vo} = -\frac{\alpha}{r_e}\frac{R_C}{1 + R_e/r_e}$$

$$A_{vo} = -\frac{g_m R_C}{1 + (R_e/r_e)} \cong -\frac{g_m R_C}{1 + g_m R_e} \tag{5.132}$$

Including R_e thus reduces the voltage gain by the factor $(1 + g_m R_e)$, which is the same factor by which R_{ib} is increased. This points out an interesting trade-off between gain and input resistance, a trade-off the designer can exercise through the choice of an appropriate value for R_e.

The output resistance R_{out} can be found from the circuit in Fig. 5.61(b) by inspection:

$$R_{\text{out}} = R_C \tag{5.133}$$

At this point we should note that for this amplifier, $R_{\text{in}} = R_i$ and $R_{\text{out}} = R_o$.

The short-circuit current gain A_{is} can be found from the circuit in Fig. 5.61(b) as follows:

$$i_{os} = -\alpha i_e$$

$$i_i = v_i / R_{\text{in}}$$

Thus,

$$A_{is} = -\frac{\alpha R_{\text{in}} i_e}{v_i}$$

Substituting for i_e from Eq. (5.126) and for R_{in} from Eq. (5.125),

$$A_{is} = -\frac{\alpha(R_B \parallel R_{ib})}{r_e + R_e} \tag{5.134}$$

which for the case $R_B \gg R_{ib}$ reduces to

$$A_{is} = \frac{-\alpha(\beta + 1)(r_e + R_e)}{r_e + R_e} = -\beta$$

the same value as for the CE circuit.

The overall voltage gain from source to load can be obtained by multiplying A_v by (v_i/v_{sig}),

$$G_v = \frac{v_i}{v_s} \cdot A_v$$

Substituting for R_i by $R_B \| R_{ib}$, assuming that $R_B \gg R_{ib}$, and substituting for R_{ib} from Eq. (5.127) results in

$$G_v = -\frac{\beta(R_C \| R_L)}{R_{sig} + (\beta + 1)(r_e + R_e)} \tag{5.135}$$

We note that the gain is lower than that of the CE amplifier because of the additional term $(\beta + 1)R_e$ in the denominator. The gain, however, is less sensitive to the value of β, a desirable result.

Another important consequence of including the resistance R_e in the emitter is that it enables the amplifier to handle larger input signals without incurring nonlinear distortion. This is because only a fraction of the input signal at the base, v_i, appears between the base and the emitter. Specifically, from the circuit in Fig. 5.61(b), we see that

$$\frac{v_\pi}{v_i} = \frac{r_e}{r_e + R_e} \cong \frac{1}{1 + g_m R_e} \tag{5.136}$$

Thus, for the same v_π, the signal at the input terminal of the amplifier, v_i, can be greater than for the CE amplifier by the factor $(1 + g_m R_e)$.

To summarize, including a resistance R_e in the emitter of the CE amplifier results in the following characteristics:

1. The input resistance R_{ib} is increased by the factor $(1 + g_m R_e)$.
2. The voltage gain from base to collector, A_v, is reduced by the factor $(1 + g_m R_e)$.
3. For the same nonlinear distortion, the input signal v_i can be increased by the factor $(1 + g_m R_e)$.
4. The overall voltage gain is less dependant on the value of β.
5. The high-frequency response is significantly improved (as we shall see in Chapter 8).

With the exception of gain reduction, these characteristics represent performance improvements. Indeed, the reduction in gain is the price paid for obtaining the other performance improvements. In many cases this is a good bargain; it is the underlying principle for the use of negative feedback. That the resistance R_e introduces negative feedback in the amplifier circuit can be seen by reference to Fig. 5.61(a). If for some reason the collector current increases, the emitter current also will increase, resulting in an increased voltage drop across R_e. Thus the emitter voltage rises, and the base–emitter voltage decreases. The latter effect causes the collector current to decrease, counteracting the initially assumed change, an indication of the presence of negative feedback. In Chapter 9, where we shall study negative feedback formally, we will find that the factor $(1 - g_m R_e)$ which appears repeatedly, is the "amount of negative feedback" introduced by R_e. Finally, we note that the negative feedback action of R_e gives it the name **emitter degeneration resistance.**

Before leaving this circuit we wish to point out that we have shown a number of the circuit analysis steps directly on the circuit diagram in Fig. 5.61(a). With practice, the reader should be able to do all of the small-signal analysis directly on the circuit, thus dispensing with the task of drawing a complete small-signal equivalent-circuit model.

EXERCISE

5.44 Consider the emitter-degenerated CE circuit of Fig. 5.61 when biased as in Exercise 5.41. In particular refer to Fig. E5.41 for the bias currents and for the values of the elements of the BJT model at the bias point. Let the amplifier be fed with a source having $R_{sig} = 5$ kΩ, and let $R_L = 5$ kΩ. Find the value of R_e that results in R_{in} equal to four times the source resistance R_{sig}. For this value of R_e, find A_{vo}, R_{out}, A_v, G_v, and A_{is}. If v_π is to be limited to 5 mV, what is the maximum value v_{sig} can have with and without R_e included. Find the corresponding v_o.

Ans. 225 Ω; –32 V/V; 8 kΩ; –12.3 V/V; –9.8 V/V; 62.5 mV; 15 mV; 0.6 V

5.7.5 The Common-Base (CB) Amplifier

By establishing a signal ground on the base terminal of the BJT, a circuit configuration aptly named common-base or **grounded-base amplifier** is obtained. The input signal is applied to the emitter, and the output is taken at the collector, with the base forming a common terminal between the input and output ports. Figure 5.62(a) shows a CB amplifier based on the circuit of Fig. 5.59. Observe that since both the dc and ac voltages at the base are zero, we have connected the base directly to ground, thus eliminating resistor R_B altogether. Coupling capacitors C_{C1} and C_{C2} perform similar functions to those in the CE circuit.

The small-signal equivalent circuit model of the amplifier is shown in Fig. 5.62(b). Since resistor R_{sig} appears in series with the emitter terminal, we have elected to use the T model for the transistor. Although the hybrid-π model would yield identical results, the T model is more convenient in this case. We have not included r_o. This is because including r_o would complicate the analysis considerably, for it would appear between the output and input of the amplifier. Fortunately, it turns out that the effect of r_o on the performance of a discrete CB amplifier is very small. We will consider the effect of r_o when we study the IC form of the CB amplifier in Chapter 6.

From inspection of the equivalent circuit model in Fig. 5.62(b), we see that the input resistance is

$$R_{in} = r_e \tag{5.137}$$

This should have been expected since we are looking into the emitter and the base is grounded. Typically r_e is a few ohms to a few tens of ohms; thus the CB amplifier has a low input resistance.

To determine the voltage gain, we write at the collector node

$$v_o = -\alpha i_e (R_C \parallel R_L)$$

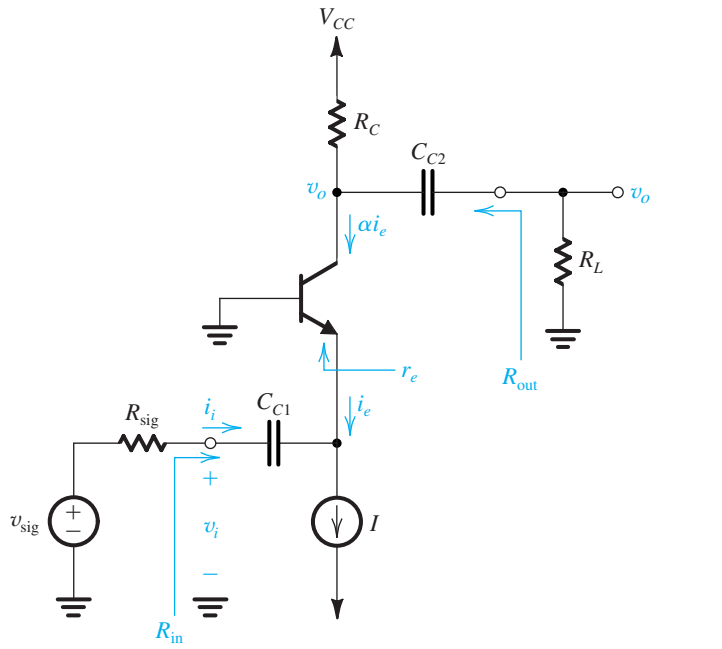
and substitute for the emitter current from

$$i_e = -\frac{v_i}{r_e}$$

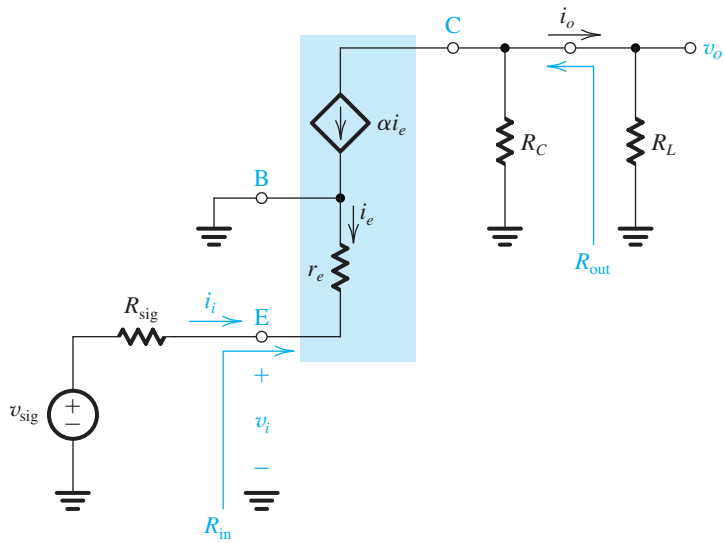
to obtain

$$A_v \equiv \frac{v_o}{v_i} = \frac{\alpha}{r_e}(R_C \parallel R_L) = g_m(R_C \parallel R_L) \tag{5.138}$$

which except for its positive sign is identical to the expression for A_v for the CE amplifier.



(a)



(b)

FIGURE 5.62 **(a)** A common-base amplifier using the structure of Fig. 5.59. **(b)** Equivalent circuit obtained by replacing the transistor with its T model.

The open-circuit voltage gain A_{vo} can be found from Eq. (5.138) by setting $R_L = \infty$:

$$A_{vo} = g_m R_C \tag{5.139}$$

Again, this is identical to A_{vo} for the CE amplifier except that the CB amplifier is noninverting. The output resistance of the CB circuit can be found by inspection from the circuit in

Fig. 5.62(b) as

$$R_{\text{out}} = R_C$$

which is similar to the case of the CE amplifier. Here we should note that the CB amplifier with r_o neglected is unilateral, with the result that $R_{\text{in}} = R_i$ and $R_{\text{out}} = R_o$.

The short-circuit current gain A_{is} is given by

$$A_{is} = \frac{-\alpha i_e}{i_i} = \frac{-\alpha i_e}{-i_e} = \alpha \tag{5.140}$$

which corresponds to our definition of α as the short-circuit current gain of the CB configuration.

Although the gain of the CB amplifier proper has the same magnitude as that of the CE amplifier, this is usually not the case as far as the overall voltage gain is concerned. The low input resistance of the CB amplifier can cause the input signal to be severely attenuated, specifically

$$\frac{v_i}{v_{\text{sig}}} = \frac{R_i}{R_{\text{sig}} + R_i} = \frac{r_e}{R_{\text{sig}} + r_e} \tag{5.141}$$

from which we see that except for situations in which R_{sig} is on the order of r_e, the signal transmission factor v_i/v_{sig} can be very small. It is useful at this point to mention that indeed one of the applications of the CB circuit is to amplify high-frequency signals that appear on a coaxial cable. To prevent signal reflection on the cable, the CB amplifier is required to have an input resistance equal to the characteristic resistance of the cable, which is usually in the range of 50 Ω to 75 Ω.

The overall voltage gain G_v of the CB amplifier can be obtained by multiplying the ratio v_i/v_{sig} of Eq. (5.141) by A_v from Eq. (5.138),

$$\begin{aligned} G_v &= \frac{r_e}{R_{\text{sig}} + r_e} g_m (R_C \parallel R_L) \\ &= \frac{\alpha (R_C \parallel R_L)}{R_{\text{sig}} + r_e} \end{aligned} \tag{5.142}$$

Since $\alpha \cong 1$, we see that the overall voltage gain is simply the ratio of the total resistance in the collector circuit to the total resistance in the emitter circuit. We also note that the overall voltage gain is almost independent of the value of β (except through the small dependence of α on β), a desirable property. Observe that for R_{sig} of the same order as R_C and R_L, the gain will be very small.

In summary, the CB amplifier exhibits a very low input resistance (r_e) a short-circuit current gain that is nearly unity (α), an open-circuit voltage gain that is positive and equal in magnitude to that of the CE amplifier ($g_m R_C$), and like the CE amplifier, a relatively high output resistance (R_C). Because of its very low input resistance, the CB circuit *alone* is not attractive as a voltage amplifier except in specialized applications, such as the cable amplifier mentioned above. The CB amplifier has excellent high-frequency performance as well, which as we shall see in Chapter 8 makes it useful together with other circuits in the implementation of high-frequency amplifiers. Finally, a very significant application of the CB circuit is as a unity-gain current amplifier or **current buffer:** It accepts an input signal current at a low input resistance and delivers a nearly equal current at very high output resistance at the collector (the output resistance excluding R_C and neglecting r_o is infinite). We shall study such an application in the context of the IC version of the CB circuit in Chapter 6.

EXERCISES

5.45 Consider the CB amplifier of Fig. 5.62(a) when designed using the BJT and component values specified in Exercise 5.41. Specifically, refer to Fig. E5.41 for the bias quantities and the values of the components of the BJT small-signal model. Let $R_{sig} = R_L = 5$ kΩ. Find the values of R_{in}, A_{vo}, R_o, A_v, v_i/v_s, and G_v. To what value should R_{sig} be reduced to obtain an overall voltage gain equal to that found for the CE amplifier in Exercise 5.43, that is, –39 V/V?

Ans. 25 Ω; +320 V/V; 8 kΩ; +123 V/V; 0.005 V/V; 0.6 V/V; 54 Ω

D5.46 It is required to design a CB amplifier for a signal delivered by a 50-Ω coaxial cable. The amplifier is to provide a "proper termination" for the cable and to provide an overall voltage gain of +100 V/V. Specify the value of the bias current I_E and the total resistance in the collector circuit.

Ans. 0.5 mA; 10 kΩ

5.7.6 The Common-Collector (CC) Amplifier or Emitter Follower

The last of the basic BJT amplifier configurations is the common-collector (CC) circuit, a very important circuit that finds frequent application in the design of both small-signal and large-signal amplifiers (Chapter 7) and even in digital circuits (Chapter 11). The circuit is more commonly known by the alternate name *emitter follower,* the reason for which will shortly become apparent.

An emitter-follower circuit based on the structure of Fig. 5.59 is shown in Fig. 5.63(a). Observe that since the collector is to be at signal ground, we have eliminated the collector resistance R_C. The input signal is capacitively coupled to the base, and the output signal is capacitively coupled from the emitter to a load resistance R_L.

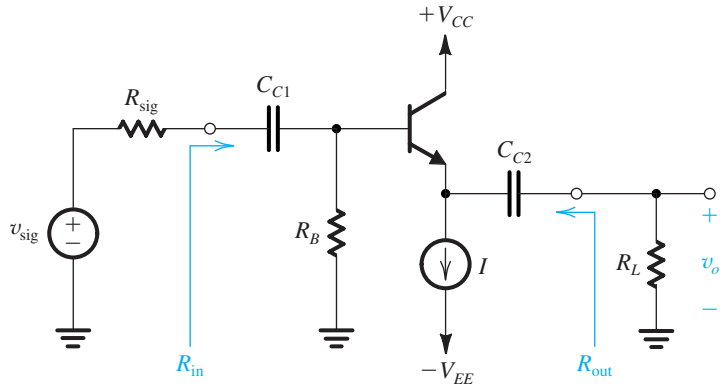
Since, as far as signals are concerned, resistance R_L is connected in series with the emitter, the T model of the BJT would be the more convenient one to use. Figure 5.63(b) shows the small-signal equivalent circuit of the emitter follower with the BJT replaced by its T model augmented to include r_o. Here it is relatively simple to take r_o into account, and we shall do so. Inspection of the circuit in Fig. 5.63(b) reveals that r_o appears in effect in parallel with R_L. Therefore the circuit is redrawn to emphasize this point, and indeed to simplify the analysis, in Fig. 5.63(c).

Unlike the CE and CB circuits we studied above, the emitter-follower circuit is *not unilateral;* that is, the input resistance depends on R_L, and the output resistance depends on R_{sig}. Care therefore must be exercised in characterizing the emitter follower. In the following we shall derive expressions for R_{in}, G_v, G_{vo}, and R_{out}. The expressions that we derive will shed light on the operation and characteristics of the emitter follower. More important than the actual expressions, however, are the methods we use to obtain them. That is what we hope the reader will become proficient in.

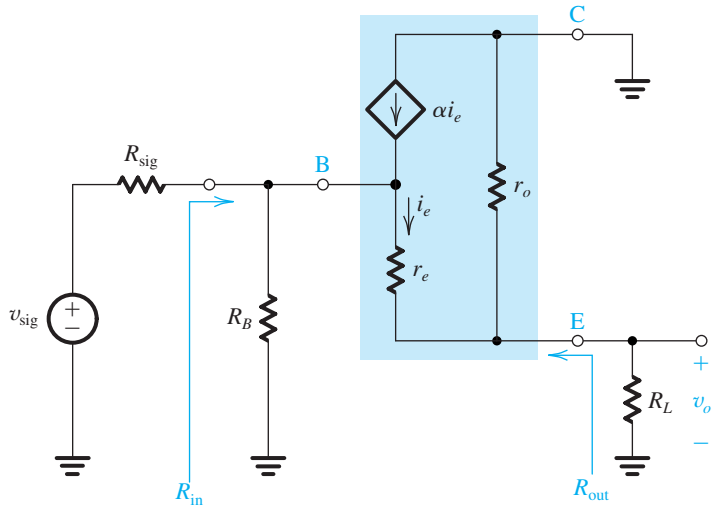
Reference to Fig. 5.63(c) reveals that the BJT has a resistance $(r_o \| R_L)$ in series with the emitter resistance r_e. Thus application of the resistance reflection rule results in the equivalent circuit shown in Fig. 5.64(a). Recall that in reflecting resistances to the base side, we multiply all resistances in the emitter by $(\beta + 1)$, the ratio of i_e to i_b. In this way the voltages remain unchanged.

Inspection of the circuit in Fig. 5.64(a) shows that the input resistance at the base, R_{ib}, is

$$R_{ib} = (\beta + 1)[r_e + (r_o \| R_L)] \tag{5.143}$$



(a)



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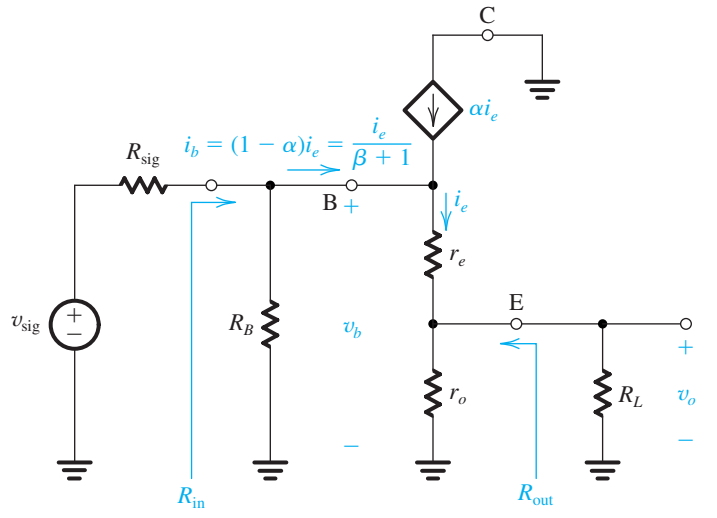


(c)

FIGURE 5.63 **(a)** An emitter-follower circuit based on the structure of Fig. 5.59. **(b)** Small-signal equivalent circuit of the emitter follower with the transistor replaced by its T model augmented with r_o. **(c)** The circuit in (b) redrawn to emphasize that r_o is in parallel with R_L. This simplifies the analysis considerably.

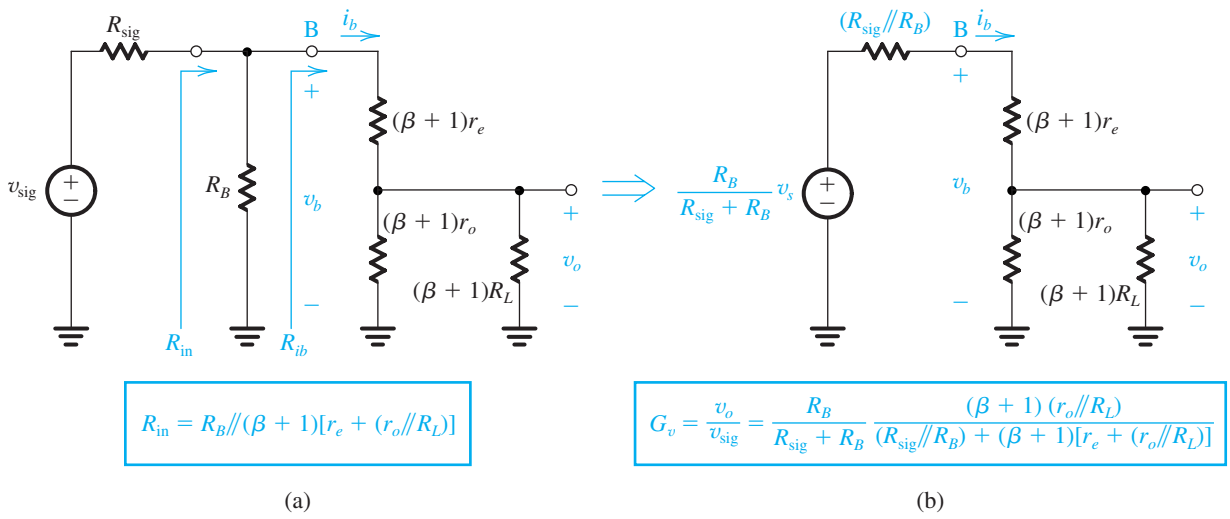


FIGURE 5.64 **(a)** An equivalent circuit of the emitter follower obtained from the circuit in Fig. 5.63(c) by reflecting all resistances in the emitter to the base side. **(b)** The circuit in (a) after application of the Thévenin theorem to the input circuit composed of V_{sig}, R_{sig}, and R_B.

from which we see that the emitter follower acts to raise the resistance level of R_L (or $R_L \parallel r_o$ to be exact) by the factor $(\beta + 1)$ and presents to the source the increased resistance. The total input resistance of the follower is

$$R_{in} = R_B \parallel R_{ib}$$

from which we see that to realize the full effect of the increased R_{ib}, we have to choose as large a value for the bias resistance R_B as is practical (i.e., from a bias design point of view). Also, whenever possible, we should dispense with R_B altogether and connect the signal source directly to the base (in which case we also dispense with C_{C1}).

To find the overall voltage gain G_v, we first apply the Thévenin theorem at the input side of the circuit in Fig. 5.64(a) to simplify it to the form shown in Fig. 5.64(b). From the latter circuit we see that v_o can be found by utilizing the voltage divider rule; thus,

$$G_v = \frac{R_B}{R_{sig} + R_B} \frac{(\beta + 1)(r_o \parallel R_L)}{(R_{sig} \parallel R_B) + (\beta + 1)[r_e + (r_o \parallel R_L)]} \tag{5.144}$$

We observe that the voltage gain is less than unity; however, for $R_B \gg R_{sig}$ and $(\beta + 1)[r_e + (r_o \parallel R_L)] \gg (R_{sig} \parallel R_B)$, it becomes very close to unity. Thus the voltage at the emitter (v_o) follows very closely the voltage at the input, which gives the circuit the name **emitter follower.**

Rather than reflecting the emitter resistance network into the base side, we can do the converse: Reflect the base resistance network into the emitter side. To keep the voltages unchanged, we divide all the base-side resistances by $(\beta + 1)$. This is the dual of the resistance reflection rule. Doing this for the circuit in Fig. 5.63(c) results in the alternate emitter-follower equivalent circuit, shown in Fig. 5.65(a). Here also we can simplify the circuit by applying the Thévenin theorem at the input side, resulting in the circuit in Fig. 5.65(b).

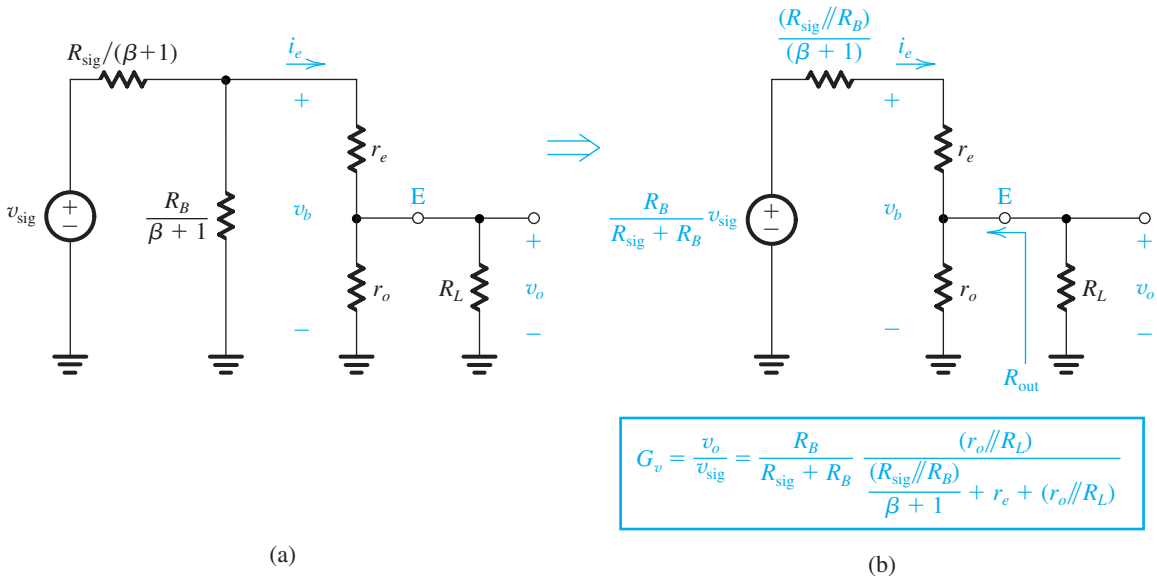


FIGURE 5.65 **(a)** An alternate equivalent circuit of the emitter follower obtained by reflecting all base-circuit resistances to the emitter side. **(b)** The circuit in (a) after application of the Thévenin theorem to the input circuit composed of V_{sig}, $R_{sig}/(\beta+1)$, and $R_B/(\beta+1)$.

Inspection of the latter reveals that the output voltage and hence v_o/v_{sig} can be found by a simple application of the voltage-divider rule, with the result that

$$G_v = \frac{R_B}{R_{sig}+R_B}\frac{(r_o \parallel R_L)}{\frac{R_{sig}\parallel R_B}{\beta+1}+r_e+(r_o \parallel R_L)} \tag{5.145}$$

which, as expected, is identical to the expression in Eq. (5.144) except that both the numerator and denominator of the second factor on the right-hand side have been divided by $(\beta+1)$. To gain further insight regarding the operation of the emitter follower, let's simplify this expression for the usual case of $R_B \gg R_{sig}$ and $r_o \gg R_L$. The result is

$$\frac{v_o}{v_{sig}} \cong \frac{R_L}{\frac{R_{sig}}{\beta+1}+r_e+R_L} \tag{5.146}$$

which clearly indicates that the gain approaches unity when $R_{sig}/(\beta+1)$ becomes much smaller than R_L or alternatively when $(\beta+1)R_L$ becomes much larger than R_{sig}. This is the **buffering action** of the emitter follower, which derives from the fact that the circuit has a short-circuit current that is approximately equal to $(\beta+1)$.

It is also useful to represent the output of the emitter follower by its Thévenin equivalent circuit. The open-circuit output voltage will be $G_{vo}v_{sig}$ where G_{vo} can be obtained from Eq. (5.145) by setting $R_L=\infty$,

$$G_{vo} = \frac{R_B}{R_{sig}+R_B}\frac{r_o}{\frac{R_{sig}\parallel R_B}{\beta+1}+r_e+r_o} \tag{5.147}$$

Note that r_o usually is large and the second factor becomes almost unity. The first factor approaches unity for $R_B \gg R_{sig}$. The Thévenin resistance is the output resistance R_{out}. It can be determined by inspection of the circuit in Fig. 5.65(b): Reduce v_{sig} to zero, "grab hold" of the emitter terminal, and look back into the circuit. The result is

$$R_{out} = r_o \parallel \left(r_e + \frac{R_{sig} \parallel R_B}{\beta + 1} \right) \tag{5.148}$$

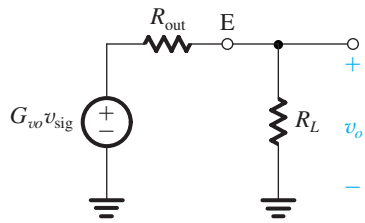
Usually r_o is much larger than the parallel component between the parentheses and can be neglected, leaving

$$R_{out} \cong r_e + \frac{R_{sig} \parallel R_B}{\beta + 1} \tag{5.149}$$

Thus the output resistance of the emitter follower is low, again a result of its impedance transformation or buffering action, which leads to the division of $(R_{sig} \parallel R_B)$ by $(\beta + 1)$. The Thévenin equivalent circuit of the emitter follower is shown together with the formulas for G_{vo} and R_{out} in Fig. 5.66. This circuit can be used to find v_o and hence G_v for any value of R_L.

In summary, the emitter follower exhibits a high input resistance, a low output resistance, a voltage gain that is smaller than but close to unity, and a relatively large current gain. It is therefore ideally suited for applications in which a high-resistance source is to be connected to a low-resistance load—namely, as the last stage or output stage in a multistage amplifier, where its purpose would be not to supply additional voltage gain but rather to give the cascade amplifier a low output resistance. We shall study the design of amplifier output stages in Chapter 7.

Before leaving the emitter follower, the question of the maximum allowed signal swing deserves comment. Since only a small fraction of the input signal appears between the base and the emitter, the emitter follower exhibits linear operation for a large range of input-signal amplitude. There is, however, an absolute upper limit imposed on the value of the output-signal amplitude by transistor cutoff. To see how this comes about, consider the circuit of Fig. 5.63(a) when the input signal is a sine wave. As the input goes negative,



$$G_{vo} = \frac{R_B}{R_{sig} + R_B} \frac{r_o}{\frac{(R_{sig} /\!/ R_B)}{(\beta + 1)} + r_e + r_o}$$

$$R_{out} = r_o /\!/ \left(r_e + \frac{R_{sig} /\!/ R_B}{\beta + 1} \right)$$

FIGURE 5.66 Thévenin equivalent circuit of the output of the emitter follower of Fig. 5.63(a). This circuit can be used to find v_o and hence the overall voltage gain v_o / v_s for any desired R_L.

the output v_o will also go negative, and the current in R_L will be flowing from ground into the emitter terminal. The transistor will cut off when this current becomes equal to the bias current I. Thus the peak value of v_o can be found from

$$\frac{\hat{V}_o}{R_L} = I$$

or

$$\hat{V}_o = IR_L$$

The corresponding value of v_{sig} will be

$$\hat{V}_s = \frac{IR_L}{G_v}$$

Increasing the amplitude of v_s above this value results in the transistor becoming cut off and the negative peaks of the output-signal waveform being clipped off.

EXERCISE

5.47 The emitter follower in Fig. 5.63(a) is used to connect a source with $R_{sig} = 10$ kΩ to a load $R_L = 1$ kΩ. The transistor is biased at $I = 5$ mA, utilizes a resistance $R_B = 40$ kΩ, and has $\beta = 100$ and $V_A = 100$ V. Find R_{ib}, R_{in}, G_v, G_{vo}, and R_{out}. What is the largest peak amplitude of an output sinusoid that can be used without the transistor cutting off? If in order to limit nonlinear distortion the base–emitter signal voltage is limited to 10 mV peak, what is the corresponding amplitude at the output? What will the overall voltage gain become if R_L is changed to 2 kΩ? To 500 Ω?

Ans. 96.7 kΩ; 28.3 kΩ; 0.735 V/V; 0.8 V/V; 84 Ω; 5 V; 1.9 V; 0.768 V/V; 0.685 V/V

5.7.7 Summary and Comparisons

For easy reference and to enable comparisons, we present in Table 5.6 the formulas for determining the characteristic parameters of discrete single-stage BJT amplifiers. In addition to the remarks already made throughout this section about the characteristics and areas of applicability of the various configurations, we make the following concluding points:

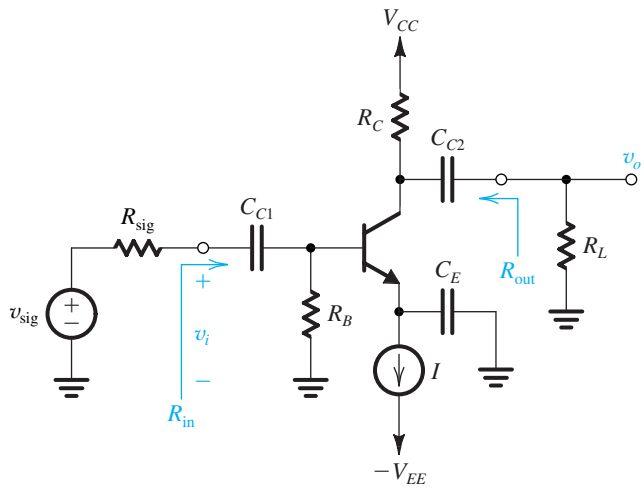
1. The CE configuration is the best suited for realizing the bulk of the gain required in an amplifier. Depending on the magnitude of the gain required, either a single stage or a cascade of two or three stages can be used.
2. Including a resistor R_e in the emitter lead of the CE stage provides a number of performance improvements at the expense of gain reduction.
3. The low input resistance of the CB amplifier makes it useful only in specific applications. As we shall see in Chapter 8, it has a much superior high-frequency response than the CE amplifier. This will make it useful as a high-frequency amplifier, especially when combined with the CE circuit. We shall see one such combination in Chapter 6.

4. The emitter follower finds application as a voltage buffer for connecting a high-resistance source to a low-resistance load and as the output stage in a multistage amplifier.

Finally, we should point out that the Exercises in this section (except for that relating to the emitter follower) used the same component values to allow numerical comparisons.

TABLE 5.6 Characteristics of Single-Stage Discrete BJT Amplifiers

Common Emitter



$$R_{\text{in}} = R_B \parallel r_\pi = R_B \parallel (\beta+1)r_e$$

$$A_v = -g_m(r_o \parallel R_C \parallel R_L)$$

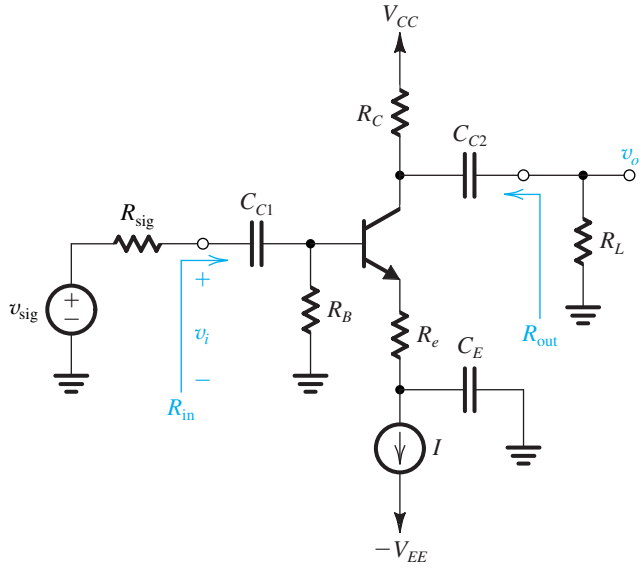
$$R_{\text{out}} = r_o \parallel R_C$$

$$G_v = -\frac{(R_B \parallel r_\pi)}{(R_B \parallel r_\pi) + R_{\text{sig}}} g_m(r_o \parallel R_C \parallel R_L)$$

$$\cong -\frac{\beta(r_o \parallel R_C \parallel R_L)}{r_\pi + R_{\text{sig}}}$$

$$A_{is} = -g_m R_{\text{in}} \cong -\beta$$

Common Emitter with Emitter Resistance



Neglecting r_o:

$$R_{\text{in}} = R_B \parallel (\beta+1)(r_e + R_e)$$

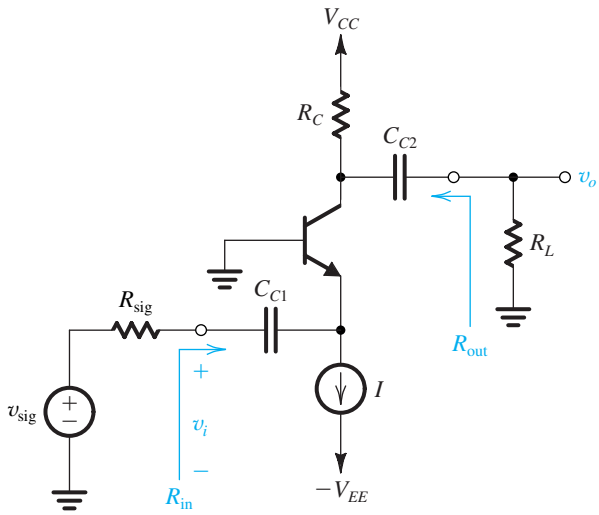
$$A_v = -\frac{\alpha(R_C \parallel R_L)}{r_e + R_e} \cong \frac{-g_m(R_C \parallel R_L)}{1 + g_m R_e}$$

$$R_{\text{out}} = R_C$$

$$G_v \cong -\frac{\beta(R_C \parallel R_L)}{R_{\text{sig}} + (\beta+1)(r_e + R_e)}$$

$$\frac{v_\pi}{v_i} \cong \frac{1}{1 + g_m R_e}$$

Common Base



Neglecting r_o:

$$R_{in} = r_e$$

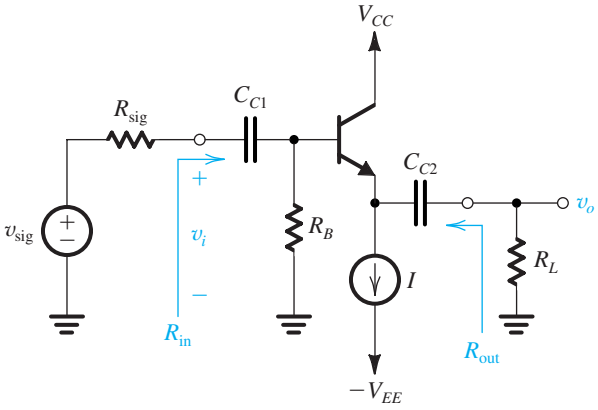
$$A_v = g_m(R_C \parallel R_L)$$

$$R_{out} = R_C$$

$$G_v = \frac{\alpha(R_C \parallel R_L)}{R_{sig} + r_e}$$

$$A_{is} \cong \alpha$$

Common Collector or Emitter Follower



$$R_{in} = R_B \parallel (\beta + 1)[r_e + (r_o \parallel R_L)]$$

$$A_v = \frac{(r_o \parallel R_L)}{(r_o \parallel R_L) + r_e}$$

$$R_{out} = r_o \parallel \left[r_e + \frac{R_{sig} \parallel R_B}{\beta + 1}\right]$$

$$G_v = \frac{R_B}{R_B + R_{sig}} \frac{(r_o \parallel R_L)}{\frac{R_{sig} \parallel R_B}{\beta + 1} + r_e + (r_o \parallel R_L)}$$

$$A_{is} \cong \beta + 1$$

5.8 THE BJT INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

Thus far we have assumed transistor action to be instantaneous, and as a result the transistor models we have developed do not include any elements (i.e., capacitors or inductors) that would cause time or frequency dependence. Actual transistors, however, exhibit charge-storage phenomena that limit the speed and frequency of their operation. We have already encountered such effects in our study of the *pn* junction in Chapter 3 and learned that they can be modeled as capacitances. In the following we study the charge-storage effects that take place in the BJT and take them into account by adding capacitances to the hybrid-π

model. The resulting augmented BJT model will be able to predict the observed dependence of amplifier gain on frequency and the time delays that transistor switches and logic gates exhibit.

5.8.1 The Base-Charging or Diffusion Capacitance C_{de}

When the transistor is operating in the active or saturation modes, minority-carrier charge is stored in the base region. In fact, we have already derived an expression for this charge, Q_n, in the case of an *npn* transistor operating in the active mode (Eq. 5.7). Using the result in Eq. (5.7) together with Eqs. (5.3) and (5.4), we can express Q_n in terms of the collector current i_C as

$$Q_n = \frac{W^2}{2D_n} i_C = \tau_F i_C \tag{5.150}$$

where τ_F is a device constant,

$$\tau_F = \frac{W^2}{2D_n} \tag{5.151}$$

with the dimension of time. It is known as the **forward base-transit time** and represents the average time a charge carrier (electron) spends in crossing the base. Typically, τ_F is in the range of 10 ps to 100 ps. For operation in the reverse active mode, a corresponding constant τ_R applies and is many orders of magnitude larger than τ_F.

Equation (5.151) applies for large signals and, since i_C is exponentially related to v_{BE}, Q_n will similarly depend on v_{BE}. Thus this charge-storage mechanism represents a nonlinear capacitive effect. However, for small signals we can define the **small-signal diffusion capacitance C_{de},**

$$C_{de} \equiv \frac{dQ_n}{dv_{BE}} = \tau_F \frac{di_C}{dv_{BE}} \tag{5.152}$$

resulting in

$$C_{de} = \tau_F g_m = \tau_F \frac{I_C}{V_T} \tag{5.153}$$

5.8.2 The Base–Emitter Junction Capacitance C_{je}

Using the development in Chapter 3, and in particular Eq. (3.X), the base–emitter junction or depletion-layer capacitance C_{je} can be expressed as

$$C_{je} = \frac{C_{je0}}{\left(1 - \dfrac{V_{BE}}{V_{0e}}\right)^m} \tag{5.154}$$

where C_{je0} is the value of C_{je} at zero voltage, V_{0e} is the EBJ built-in voltage (typically, 0.9 V), and m is the grading coefficient of the EBJ junction (typically, 0.5). It turns out, however, that because the EBJ is forward biased in the active mode, Eq. (5.154) does not provide an accurate prediction of C_{je}. Alternatively, one typically uses an approximate value for C_{je},

$$C_{je} \cong 2C_{je0} \tag{5.155}$$

5.8.3 The Collector–Base Junction Capacitance C_μ

In active-mode operation, the CBJ is reverse biased, and its junction or **depletion capacitance,** usually denoted C_μ, can be found from

$$C_\mu = \frac{C_{\mu 0}}{\left(1 + \dfrac{V_{CB}}{V_{0c}}\right)^m} \tag{5.156}$$

where $C_{\mu 0}$ is the value of C_μ at zero voltage, V_{0c} is the CBJ built-in voltage (typically, 0.75 V), and m is its grading coefficient (typically, 0.2–0.5).

5.8.4 The High-Frequency Hybrid-π Model

Figure 5.67 shows the hybrid-π model of the BJT, including capacitive effects. Specifically, there are two capacitances: the emitter–base capacitance $C_\pi = C_{de} + C_{je}$ and the collector–base capacitance C_μ. Typically, C_π is in the range of a few picofarads to a few tens of picofarads, and C_μ is in the range of a fraction of a picofarad to a few picofarads. Note that we have also added a resistor r_x to model the resistance of the silicon material of the base region between the base terminal B and a fictitious internal, or intrinsic, base terminal B′ that is right under the emitter region (refer to Fig. 5.6). Typically, r_x is a few tens of ohms, and its value depends on the current level in a rather complicated manner. Since (usually) $r_x \ll r_\pi$, its effect is negligible at low frequencies. Its presence is felt, however, at high frequencies, as will become apparent later.

The values of the hybrid-π equivalent circuit parameters can be determined at a given bias point using the formulas presented in this chapter. They can also be found from the terminal measurements specified on the BJT data sheets as described in Appendix X. For computer simulation, SPICE uses the parameters of the given IC technology to evaluate the BJT model parameters (Section 5.11).

Before proceeding, a note on notation is in order. Since we are now dealing with voltages and currents that are functions of frequency, we have reverted to using symbols that are uppercase letters with lowercase subscripts (e.g., V_π, I_c). This conforms to the notation system used throughout this book.

5.8.5 The Cutoff Frequency

The transistor data sheets do not usually specify the value of C_π. Rather, the behavior of β or h_{fe} versus frequency is normally given. In order to determine C_π and C_μ we shall derive an expression for h_{fe}, the CE short-circuit current gain, as a function of frequency in terms of

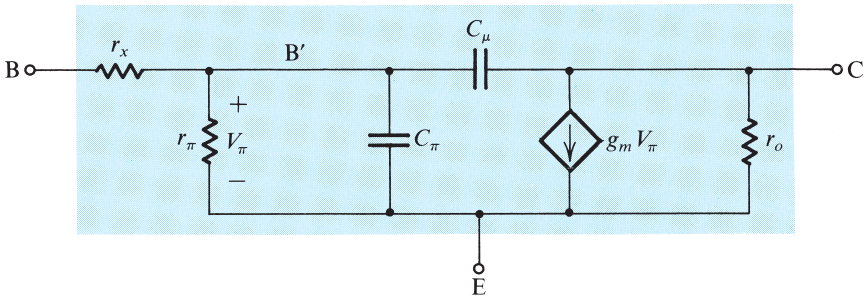


FIGURE 5.67 The high-frequency hybrid-π model.

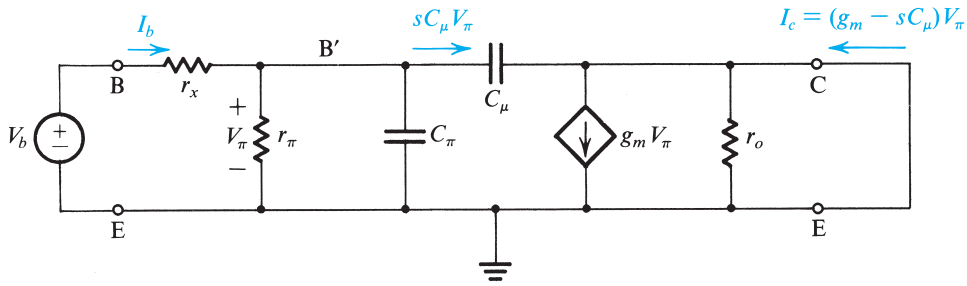


FIGURE 5.68 Circuit for deriving an expression for $h_{fe}(s) \equiv I_c / I_b$.

the hybrid-π components. For this purpose consider the circuit shown in Fig. 5.68, in which the collector is shorted to the emitter. A node equation at C provides the short-circuit collector current I_c as

$$I_c = (g_m - sC_\mu)V_\pi \tag{5.157}$$

A relationship between V_π and I_b can be established by multiplying I_b by the impedance seen between B′ and E:

$$V_\pi = I_b(r_\pi // C_\pi // C_\mu) = \frac{I_b}{1/r_\pi + sC_\pi + sC_\mu} \tag{5.158}$$

Thus h_{fe} can be obtained by combining Eqs. (5.157) and (5.158):

$$h_{fe} \equiv \frac{I_c}{I_b} = \frac{g_m - sC_\mu}{1/r_\pi + s(C_\pi + C_\mu)}$$

At the frequencies for which this model is valid, $g_m \gg \omega C_\mu$; thus we can neglect the sC_μ term in the numerator and write

$$h_{fe} \simeq \frac{g_m r_\pi}{1 + s(C_\pi + C_\mu)r_\pi}$$

Thus,

$$h_{fe} = \frac{\beta_0}{1 + s(C_\pi + C_\mu)r_\pi} \tag{5.159}$$

where β_0 is the low-frequency value of β. Thus h_{fe} has a single-pole (or STC) response[10] with a 3-dB frequency at $\omega = \omega_\beta$, where

$$\omega_\beta = \frac{1}{(C_\pi + C_\mu)r_\pi} \tag{5.160}$$

Figure 5.69 shows a Bode plot for $|h_{fe}|$. From the –6-dB/octave slope it follows that the frequency at which $|h_{fe}|$ drops to unity, which is called the **unity-gain bandwidth** ω_T, is given by

$$\omega_T = \beta_0 \omega_\beta \tag{5.161}$$

[10] The frequency response of single-time-constant (STC) networks was reviewed in Section 1.6. Also, a more detailed discussion of this important topic can be found in Appendix X.

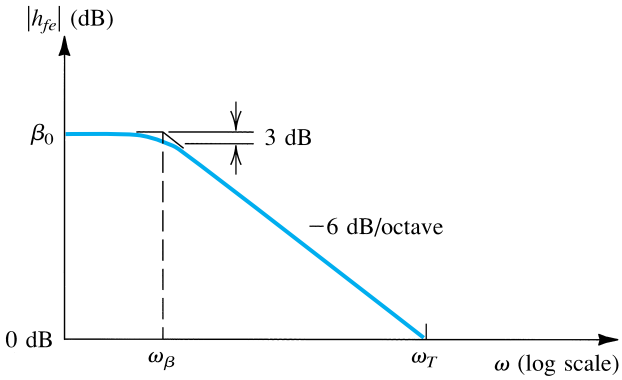


FIGURE 5.69 Bode plot for $|h_{fe}|$.

Thus,

$$\omega_T = \frac{g_m}{C_\pi + C_\mu} \tag{5.162}$$

and

$$f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} \tag{5.163}$$

The unity-gain bandwidth f_T is usually specified on the data sheets of the transistor. In some cases f_T is given as a function of I_C and V_{CE}. To see how f_T changes with I_C, recall that g_m is directly proportional to I_C, but only part of C_π (the diffusion capacitance C_{de}) is directly proportional to I_C. It follows that f_T decreases at low currents, as shown in Fig. 5.70. However, the decrease in f_T at high currents, also shown in Fig. 5.70, cannot be explained by this argument; rather it is due to the same phenomenon that causes β_0 to decrease at high currents. In the region where f_T is almost constant, C_π is dominated by the diffusion part.

Typically, f_T is in the range of 100 MHz to tens of GHz. The value of f_T can be used in Eq. (5.163) to determine $C_\pi + C_\mu$. The capacitance C_μ is usually determined separately by measuring the capacitance between base and collector at the desired reverse-bias voltage V_{CB}.

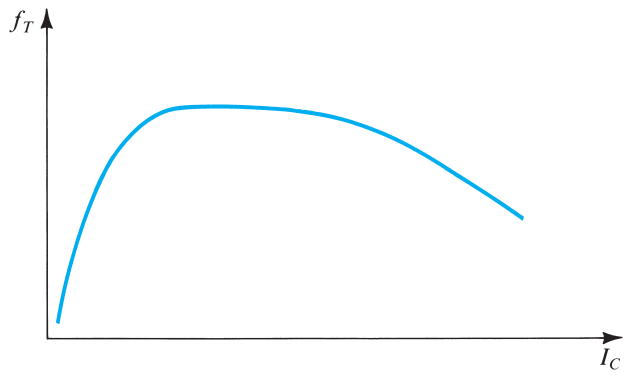


FIGURE 5.70 Variation of f_T with I_C.

Before leaving this section, we should mention that the hybrid-π model of Fig. 5.68 characterizes transistor operation fairly accurately up to a frequency of about $0.2f_T$. At higher frequencies one has to add other parasitic elements to the model as well as refine the model to account for the fact that the transistor is in fact a distributed-parameter network that we are trying to model with a lumped-component circuit. One such refinement consists of splitting r_x into a number of parts and replacing C_μ by a number of capacitors, each connected between the collector and one of the taps of r_x. This topic is beyond the scope of this book.

An important observation to make from the high-frequency model of Fig. 5.68 is that at frequencies above 5 to $10f_\beta$, one may ignore the resistance r_π. It can be seen then that r_x becomes the only resistive part of the input impedance at high frequencies. Thus r_x plays an important role in determining the frequency response of transistor circuits at high frequencies. It follows that an accurate determination of r_x should be made from a high-frequency measurement.

EXERCISES

5.48 Find C_{de}, C_{je}, C_π, C_μ, and f_T for a BJT operating at a dc collector current $I_C = 1$ mA and a CBJ reverse bias of 2 V. The device has $\tau_F = 20$ ps, $C_{je0} = 20$ fF, $C_{\mu 0} = 20$ fF, $V_{0e} = 0.9$ V, $V_{0c} = 0.5$ V, and $m_{CBJ} = 0.33$.

Ans. 0.8 pF; 40 fF; 0.84 pF; 12 fF; 7.47 GHz

5.49 For a BJT operated at $I_C = 1$ mA, determine f_T and C_π if $C_\mu = 2$ pF and $|h_{fe}| = 10$ at 50 MHz.

Ans. 500 MHz; 10.7 pF

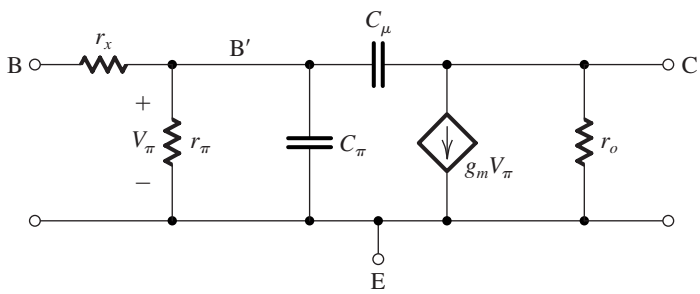
5.50 If C_π of the BJT in Exercise 5.49 includes a relatively constant depletion-layer capacitance of 2 pF, find f_T of the BJT when operated at $I_C = 0.1$ mA.

Ans. 130.7 MHz

5.8.6 Summary

For convenient reference, Table 5.7 provides a summary of the relationships used to compose the values of the parameters of the BJT high-frequency model.

TABLE 5.7 The BJT High-Frequency Model



$$g_m = I_C/V_T \qquad r_o = |V_A|/I_C \qquad r_\pi = \beta_0/g_m$$

$$C_\pi + C_\mu = \frac{g_m}{2\pi f_T} \qquad C_\pi = C_{de} + C_{je} \qquad C_{de} = \tau_F g_m \qquad C_{je} \cong 2C_{je0}$$

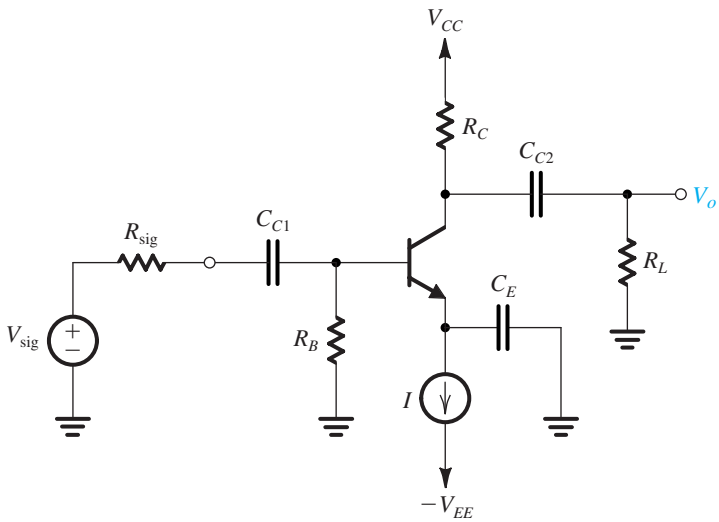
$$C_\mu = C_{jc0}\Big/\left(1 + \frac{V_{CB}}{V_{0c}}\right)^m, \quad m = 0.3\text{–}0.5$$

5.9 FREQUENCY RESPONSE OF THE COMMON-EMITTER AMPLIFIER

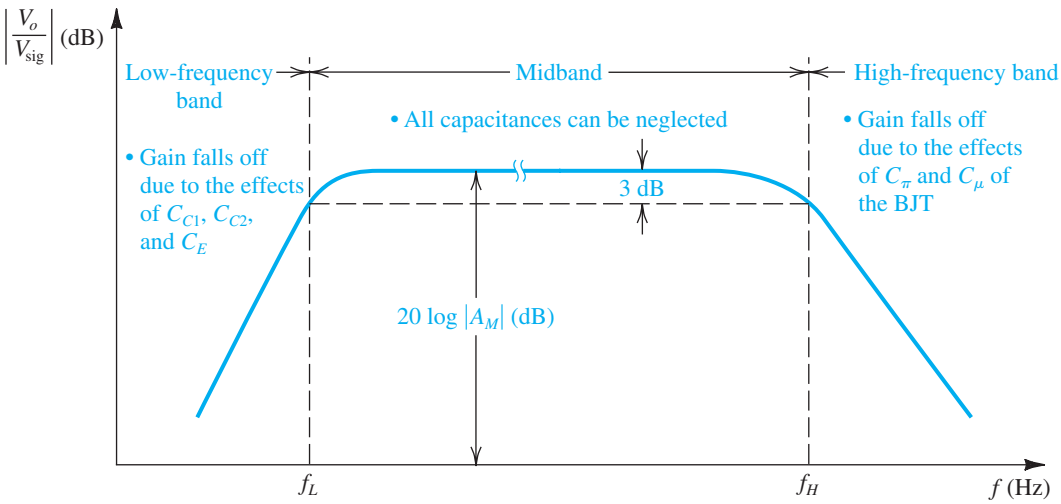
In this section we study the dependence of the gain of the BJT common-emitter amplifier of Fig. 5.71(a) on the frequency of the input signal.

5.9.1 The Three Frequency Bands

When the common-emitter amplifier circuit of Fig. 5.71(a) was studied in Section 5.7.3, it was assumed that the coupling capacitors C_{C1} and C_{C2} and the bypass capacitor C_E were



(a)



(b)

FIGURE 5.71 **(a)** Capacitively coupled common-emitter amplifier. **(b)** Sketch of the magnitude of the gain of the CE amplifier versus frequency. The graph delineates the three frequency bands relevant to frequency response determination.

acting as perfect short circuits at all signal frequencies of interest. We also neglected the internal capacitances of the BJT. That is, C_π and C_μ of the BJT high-frequency model (Fig. 5.67) were assumed to be sufficiently small to act as open circuits at all signal frequencies of interest. As a result of ignoring all capacitive effects, the gain expressions derived in Section 5.7.3 were independent of frequency. In reality, however, this situation only applies over a limited, though usually wide, band of frequencies. This is illustrated in Fig. 5.71(b), which shows a sketch of the magnitude of the overall voltage gain, $|G_v|$, of the common-emitter amplifier versus frequency. We observe that the gain is almost constant over a wide frequency band, called the **midband.** The value of the midband gain A_M corresponds to the overall voltage gain G_v that we derived in Section 5.7.3, namely,

$$A_M = \frac{V_o}{V_{\text{sig}}} = -\frac{(R_B \parallel r_\pi)}{(R_B \parallel r_\pi) + R_{\text{sig}}} g_m (r_o \parallel R_C \parallel R_L) \tag{5.164}$$

Figure 5.71(b) shows that the gain falls off at signal frequencies below and above the midband. The gain falloff in the **low-frequency band** is due to the fact that even though C_{C1}, C_{C2}, and C_E are large capacitors (typically, in the μF range), as the signal frequency is reduced their impedances increase and they no longer behave as short circuits. On the other hand, the gain falls off in the **high-frequency band** as a result of C_{gs} and C_{gd}, which though very small (in the fraction of a pF to the pF range), their impedances at sufficiently high frequencies decrease; thus they can no longer be considered as open circuits. Our objective in this section is to study the mechanisms by which these two sets of capacitances affect the amplifier gain in the low-frequency and the high-frequency bands. In this way we will be able to determine the frequencies f_L and f_H, which define the extent of the midband, as shown in Fig. 5.71(b).

The midband is obviously the useful frequency band of the amplifier. Usually, f_L and f_H are the frequencies at which the gain drops by 3 dB below its value at midband; that is, at f_L and f_H, $|\text{gain}| = |A_M|/(\sqrt{2})$. The amplifier **bandwidth** or 3-dB bandwidth is defined as the difference between the lower (f_L) and upper or higher (f_H) 3-dB frequencies:

$$BW \equiv f_H - f_L \tag{5.165}$$

Since usually $f_L \ll f_H$,

$$BW \cong f_H$$

A figure-of-merit for the amplifier is its gain–bandwidth product, defined as

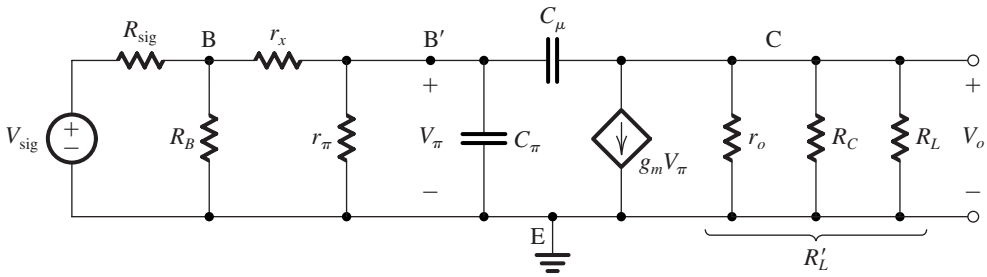
$$GB = |A_M| BW \tag{5.166}$$

It will be shown at a later stage that in amplifier design, it is usually possible to trade-off gain for bandwidth. One way of accomplishing this, for instance, is by including an emitter-degeneration resistance R_e, as we have done in Section 5.7.4.

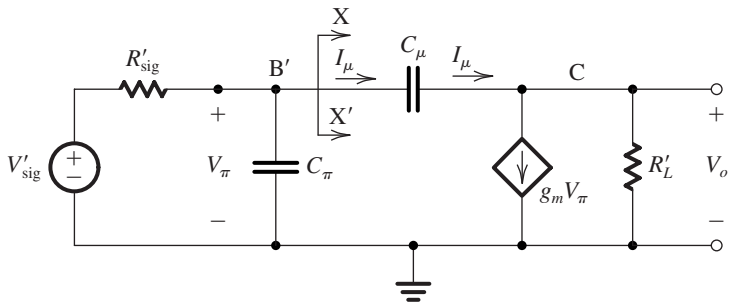
5.9.2 The High-Frequency Response

To determine the gain, or the transfer function, of the amplifier of Fig. 5.71(a) at high frequencies, and in particular the upper 3-dB frequency f_H, we replace the BJT with its high-frequency model of Fig. 5.67. At these frequencies C_{C1}, C_{C2}, and C_E will be behaving as perfect short circuits. The result is the high-frequency amplifier equivalent circuit shown in Fig. 5.72(a).

The equivalent circuit of Fig. 5.72(a) can be simplified by utilizing Thévenin theorem at the input side and by combining the three parallel resistances at the output side. Specifically, the reader should be able to show that applying Thévenin theorem *twice* simplifies the resistive network at the input side to a signal generator V'_{sig} and a resistance R'_{sig},



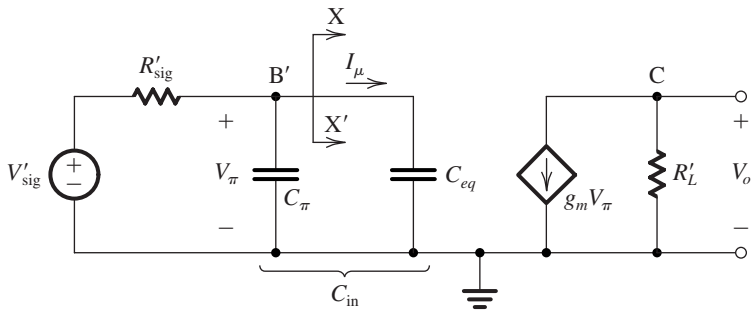
(a)



$$V'_{\text{sig}} = V_{\text{sig}} \frac{R_B}{R_B + R_{\text{sig}}} \frac{r_\pi}{r_\pi + r_x + (R_{\text{sig}} /\!/ R_B)} \qquad R'_L = r_o /\!/ R_C /\!/ R_L$$

$$R'_{\text{sig}} = r_\pi /\!/ [r_x + (R_B /\!/ R_{\text{sig}})]$$

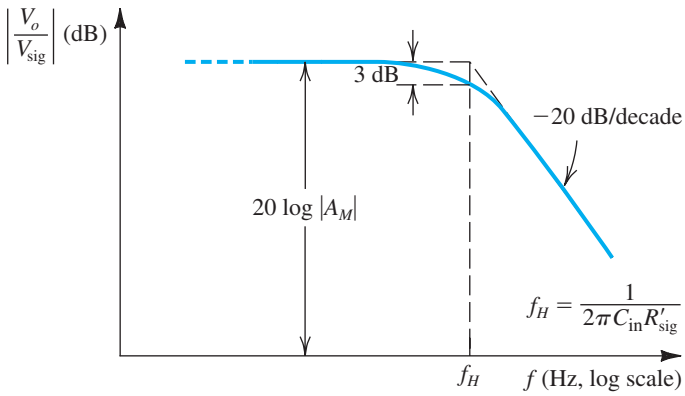
(b)



$$C_{\text{in}} = C_\pi + C_{eq} = C_\pi + C_\mu(1 + g_m R'_L) \qquad V_o = -g_m R'_L V_\pi$$

(c)

FIGURE 5.72 Determining the high-frequency response of the CE amplifier: **(a)** equivalent circuit; **(b)** the circuit of (a) simplified at both the input side and the output side; **(c)** equivalent circuit with C_μ replaced at the input side with the equivalent capacitance C_{eq};



(d)

FIGURE 5.72 *(Continued)* **(d)** sketch of the frequency-response plot, which is that of a low-pass STC circuit.

where

$$V'_{sig} = V_{sig} \frac{R_B}{R_B + R_{sig}} \frac{r_\pi}{r_\pi + r_x + (R_{sig} \parallel R_B)} \tag{5.167}$$

$$R'_{sig} = r_\pi \parallel [r_x + (R_B \parallel R_{sig})] \tag{5.168}$$

Observe that R'_{sig} is the resistance seen looking back into the resistive network between nodes B′ and E.

The circuit in Fig. 5.72(b) can be simplified further if we can find a way to deal with the bridging capacitance C_μ that connects the output node to the "input" node, B′. Toward that end consider first the output node. It can be seen that the load current is $(g_m V_\pi - I_\mu)$, where $g_m V_\pi$ is the output current of the transistor and I_μ is the current supplied through the very small capacitance C_μ. In the vicinity of f_H, which is close to the edge of the midband, it is reasonable to assume that I_μ is still much smaller than $g_m V_\pi$, with the result that V_o can be given approximately by

$$V_o \cong -g_m V_\pi R'_L = -g_m R'_L V_\pi \tag{5.169}$$

Since $V_o = V_{ce}$, Eq. (5.169) indicates that the gain from B′ to C is $-g_m R'_L$, the same value as in the midband. The current I_μ can now be found from

$$\begin{aligned} I_\mu &= sC_\mu(V_\pi - V_o) \\ &= sC_\mu[V_\pi - (-g_m R'_L V_\pi)] \\ &= sC_\mu(1 + g_m R'_L)V_\pi \end{aligned}$$

Now, in Fig. 5.72(b), the left-hand-side of the circuit, at XX′, knows of the existence of C_μ only through the current I_μ. Therefore we can replace C_μ by an equivalent capacitance C_{eq} between B′ and ground as long as C_{eq} draws a current equal to I_μ. That is,

$$sC_{eq}V_\pi = I_\mu = sC_\mu(1 + g_m R'_L)V_\pi$$

which results in

$$C_{eq} = C_{\mu}(1 + g_m R'_L) \tag{5.170}$$

Using C_{eq} enables us to simplify the equivalent circuit at the input side to that shown in Fig. 5.72(c), which we recognize as a single-time-constant (STC) network of the low-pass type (see Section 1.6 and Appendix X). Therefore we can express V_{π} in terms of V'_{gs} as

$$V_{\pi} = V'_{\text{sig}} \frac{1}{1 + s/\omega_0} \tag{5.171}$$

where ω_0 is the corner frequency of the STC network composed of C_{in} and R'_{sig},

$$\omega_0 = 1/C_{\text{in}} R'_{\text{sig}} \tag{5.172}$$

where C_{in} is the total input capacitance at B′,

$$C_{\text{in}} = C_{\pi} + C_{eq} = C_{\pi} + C_{\mu}(1 + g_m R'_L) \tag{5.173}$$

and R'_{sig} is the effective source resistance, given by Eq. (5.168). Combining Eqs. (5.169), (5.171), and (5.167) give the voltage gain in the high-frequency band as

$$\frac{V_o}{V_{\text{sig}}} = -\left[\frac{R_B}{R_B + R_{\text{sig}}} \frac{r_{\pi} \cdot g_m R'_L}{r_{\pi} + r_x + (R_{\text{sig}} \parallel R_B)}\right]\left(\frac{1}{1 + \dfrac{s}{\omega_0}}\right) \tag{5.174}$$

The quantity between the square brackets of Eq. (5.174) is the midband gain, and except for the fact that here r_x is taken into account, this expression is the same as that in Eq. (5.164). Thus,

$$\frac{V_o}{V_{\text{sig}}} = \frac{A_M}{1 + \dfrac{s}{\omega_0}} \tag{5.175}$$

from which we deduce that the upper 3-dB frequency f_H must be

$$f_H = \frac{\omega_0}{2\pi} = \frac{1}{2\pi C_{\text{in}} R'_{\text{sig}}} \tag{5.176}$$

We thus see that the high-frequency response will be that of a low-pass STC network with a 3-dB frequency f_H determined by the time constant $C_{\text{in}} R'_{\text{sig}}$. Fig. 5.72(d) shows a sketch of the magnitude of the high-frequency gain.

Before leaving this section we wish to make a number of observations:

1. The upper 3-dB frequency is determined by the interaction of R'_{sig} and C_{in}. If $R_B \gg R_{\text{sig}}$ and $r_x \ll R_{\text{sig}}$, then $R'_{\text{sig}} \cong R_{\text{sig}} \parallel r_{\pi}$. Thus the extent to which R_{sig} determines f_H depends on its value relative to r_{π}: If $R_{\text{sig}} \gg r_{\pi}$, then $R'_{\text{sig}} \cong r_{\pi}$; on the other hand, if R_{sig} is on the order of or smaller than r_{π}, then it has much greater influence on the value of f_H.
2. The input capacitance C_{in} is usually dominated by C_{eq}, which in turn is made large by the multiplication effect that C_{μ} undergoes. Thus, although C_{μ} is usually very small, its effect on the amplifier frequency response can be significant as a result of its

multiplication by the factor $(1 + g_m R'_L)$, which is approximately equal to the midband gain of the amplifier.

3. The multiplication effect that C_μ undergoes comes about because it is connected between two nodes (B′ and C) whose voltages are related by a large negative gain $(-g_m R'_L)$. This effect is known as the **Miller effect,** and $(1 + g_m R'_L)$ is known as the **Miller multiplier.** It is the Miller effect that causes the CE amplifier to have a large input capacitance C_{in} and hence a low f_H.
4. To extend the high-frequency response of a BJT amplifier, we have to find configurations in which the Miller effect is absent or at least reduced. We shall return to this subject at great length in Chapter 8.
5. The above analysis, resulting in an STC or a single-pole response, is a simplified one. Specifically, it is based on neglecting I_μ relative to $g_m V_\pi$, an assumption that applies well at frequencies not too much higher than f_H. A more exact analysis of the circuit in Fig. 5.72(a) will be considered in Chapter 8. The results above, however, are more than sufficient for our current needs.

EXAMPLE 5.18

It is required to find the midband gain and the upper 3-dB frequency of the common-emitter amplifier of Fig. 5.71(a) for the following case: $V_{CC} = V_{EE} = 10$ V, $I = 1$ mA, $R_B = 100$ kΩ, $R_C = 8$ kΩ, $R_{\text{sig}} = 5$ kΩ, $R_L = 5$ kΩ, $\beta_0 = 100$, $V_A = 100$ V, $C_\mu = 1$ pF, $f_T = 800$ MHz, and $r_x = 50$ Ω.

Solution

The transistor is biased at $I_C \cong 1$ mA. Thus the values of its hybrid-π model parameters are

$$g_m = \frac{I_C}{V_T} = \frac{1 \text{ mA}}{25 \text{ mV}} = 40 \text{ mA/V}$$

$$r_\pi = \frac{\beta_0}{g_m} = \frac{100}{40 \text{ mA/V}} = 2.5 \text{ kΩ}$$

$$r_o = \frac{V_A}{I_C} = \frac{100 \text{ V}}{1 \text{ mA}} = 100 \text{ kΩ}$$

$$C_\pi + C_\mu = \frac{g_m}{\omega_T} = \frac{40 \times 10^{-3}}{2\pi \times 800 \times 10^6} = 8 \text{ pF}$$

$$C_\mu = 1 \text{ pF}$$

$$C_\pi = 7 \text{ pF}$$

$$r_x = 50 \text{ Ω}$$

The midband voltage gain is

$$A_M = -\frac{R_B}{R_B + R_{\text{sig}}} \frac{r_\pi}{r_\pi + r_x + (R_B \parallel R_{\text{sig}})} g_m R'_L$$

where

$$R'_L = r_o \parallel R_C \parallel R_L$$

$$= (100 \parallel 8 \parallel 5) \text{ kΩ} = 3 \text{ kΩ}$$

Thus,

$$g_m R'_L = 40 \times 3 = 120 \text{ V/V}$$

and

$$A_M = -\frac{100}{100+5} \times \frac{2.5}{2.5+0.05+(100 \parallel 5)} \times 120$$
$$= -39 \text{ V/V}$$

and

$$20 \log |A_M| = 32 \text{ dB}$$

To determine f_H we first find C_{in},

$$C_{\text{in}} = C_\pi + C_\mu (1 + g_m R'_L)$$
$$= 7 + 1(1 + 120) = 128 \text{ pF}$$

and the effective source resistance R'_{sig},

$$R'_{\text{sig}} = r_\pi \parallel [r_x + (R_B \parallel R_{\text{sig}})]$$
$$= 2.5 \parallel [0.05 + (100 \parallel 5)]$$
$$= 1.65 \text{ k}\Omega$$

Thus,

$$f_H = \frac{1}{2\pi C_{\text{in}} R'_{\text{sig}}} = \frac{1}{2\pi \times 128 \times 10^{-12} \times 1.65 \times 10^3} = 754 \text{ kHz}$$

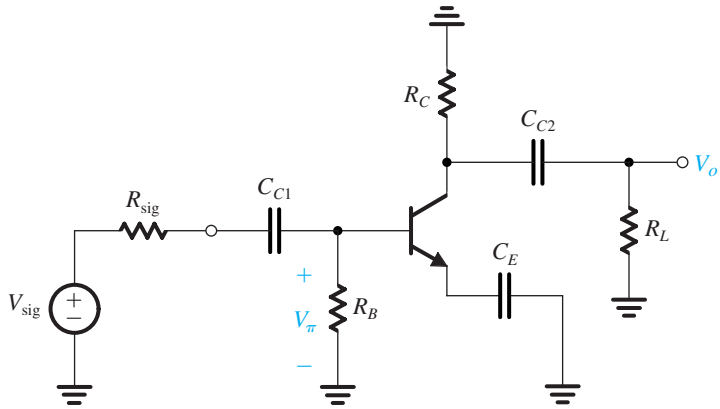
EXERCISE

5.51 For the amplifier in Example 5.18, find the value of R_L that reduces the midband gain to half the value found. What value of f_H results? Note the trade-off between gain and bandwidth.

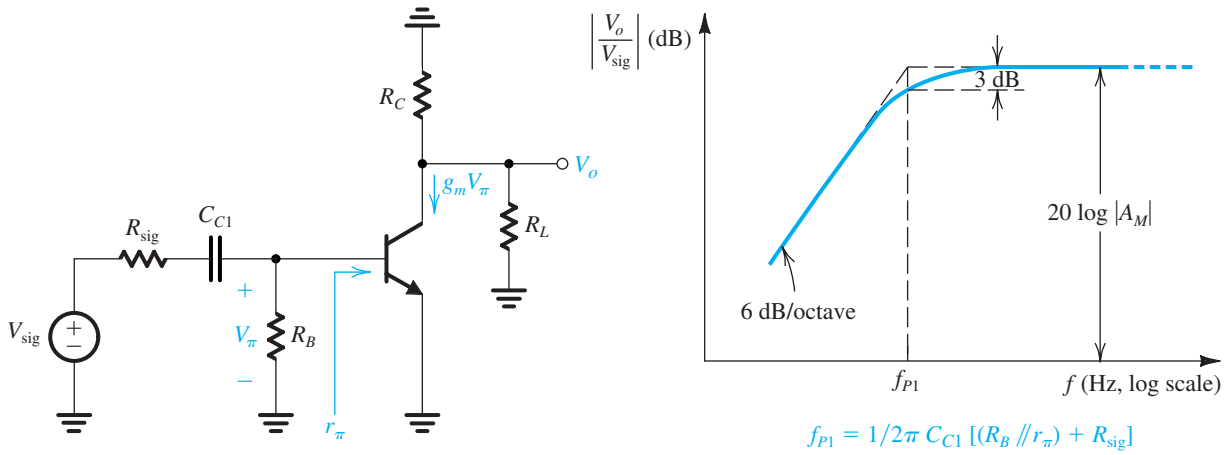
Ans. 1.9 kΩ; 1.42 MHz

5.9.3 The Low-Frequency Response

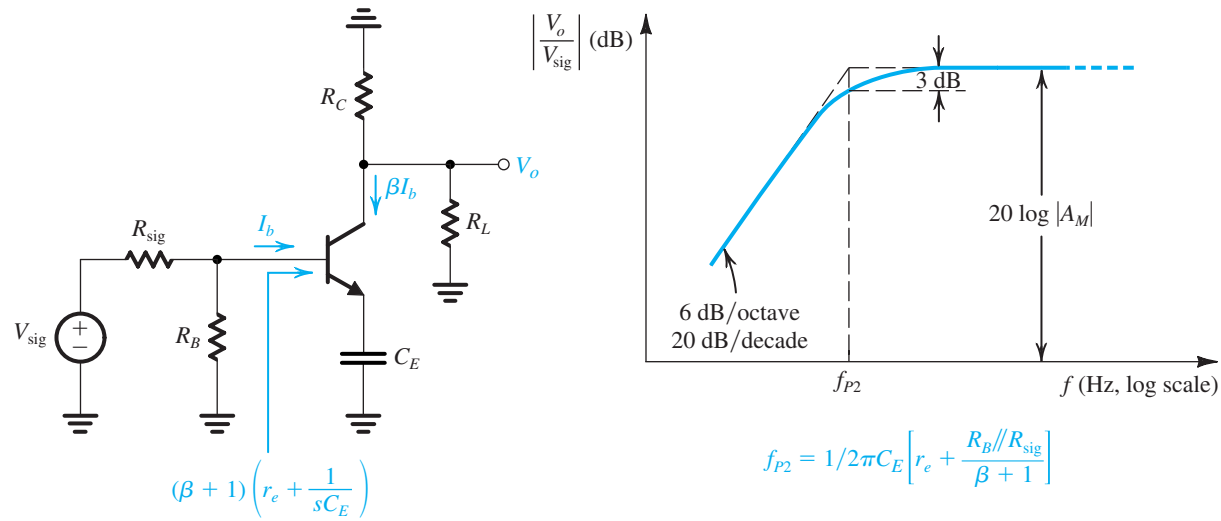
To determine the low-frequency gain or transfer function of the common-emitter amplifier circuit, we show in Fig. 5.73(a) the circuit with the dc sources eliminated (current source I open circuited and voltage source V_{CC} short circuited). We shall perform the small-signal analysis directly on this circuit. We will, of course, ignore C_π and C_μ since at such low frequencies their impedances will be very high and thus can be considered as open circuits. Also, to keep the analysis simple and thus focus attention on the mechanisms that limit the amplifier gain at low frequencies, we will neglect r_o. The reader can verify through SPICE simulation that the effect of r_o on the low-frequency amplifier gain is small. Finally, we shall also neglect r_x, which is usually much smaller than r_π, with which it appears in series.



(a)

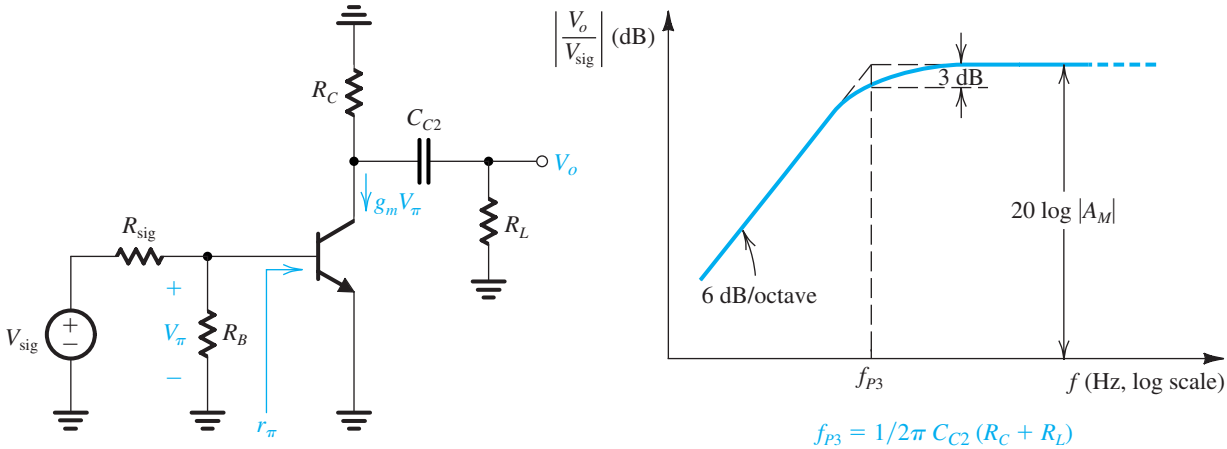


(b)

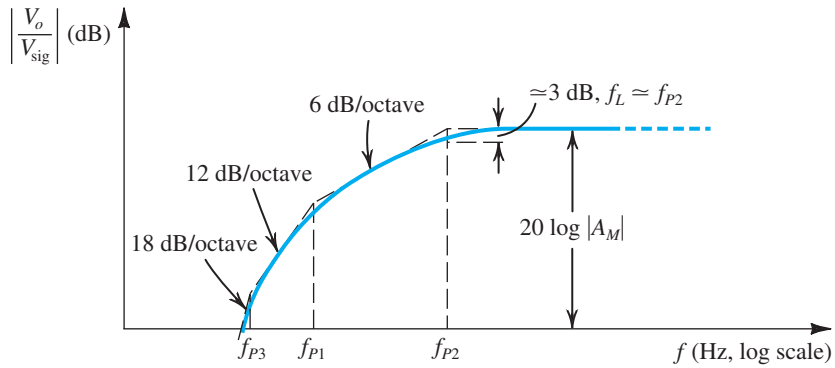


(c)

FIGURE 5.73 Analysis of the low-frequency response of the CE amplifier: **(a)** amplifier circuits with dc sources removed; **(b)** the effect of C_{C1} is determined with C_E and C_{C2} assumed to be acting as perfect short circuits; **(c)** the effect of C_E is determined with C_{C1} and C_{C2} assumed to be acting as perfect short circuits;



(d)



(e)

FIGURE 5.73 *(Continued)* **(d)** the effect of C_{C2} is determined with C_{C1} and C_E assumed to be acting as perfect short circuits; **(e)** sketch of the low-frequency gain under the assumptions that C_{C1}, C_E, and C_{C2} do not interact and that their break (or pole) frequencies are widely separated.

Our first cut at the analysis of the circuit in Fig. 5.72(a) is to consider the effect of the three capacitors C_{C1}, C_E, and C_{C2} *one at a time*. That is, when finding the effect of C_{C1}, we shall assume that C_E and C_{C2} are acting as perfect short circuits, and when considering C_E, we assume that C_{C1} and C_{C2} are perfect short circuits, and so on. This is obviously a major simplifying assumption—and one that might not be justified. However, it should serve as a first cut at the analysis enabling us to gain insight into the effect of these capacitances.

Figure 5.72(b) shows the circuit with C_E and C_{C2} replaced with short circuits. The voltage V_π at the base of the transistor can be written as

$$V_\pi = V_{sig} \frac{R_B \parallel r_\pi}{(R_B \parallel r_\pi) + R_{sig} + \dfrac{1}{sC_{C1}}}$$

and the output voltage is obtained as

$$V_o = -g_m V_\pi (R_C \parallel R_L)$$

These two equations can be combined to obtain the voltage gain V_o/V_{sig} including the effect of C_{C1} as

$$\frac{V_o}{V_{\text{sig}}} = -\frac{(R_B \parallel r_\pi)}{(R_B \parallel r_\pi) + R_{\text{sig}}} g_m (R_C \parallel R_L) \left[\frac{s}{s + \dfrac{1}{C_{C1}[(R_B \parallel r_\pi) + R_{\text{sig}}]}} \right] \tag{5.177}$$

from which we observe that the effect of C_{C1} is to introduce the frequency-dependent factor between the square brackets on the right-hand side of Eq. (5.177). We recognize this factor as the transfer fraction of a single-time-constant (STC) network of the high-pass type (see Section 1.6 and Appendix X) with a corner or break frequency ω_{P1},

$$\omega_{P1} = \frac{1}{C_{C1}[(R_B \parallel r_\pi) + R_{\text{sig}}]} \tag{5.178}$$

Note that $[(R_B \parallel r_\pi) + R_{\text{sig}}]$ is the *resistance seen between the terminals of* C_{C1} *when* V_{sig} *is set to zero*. The STC high-pass factor introduced by C_{C1} will cause the amplifier gain to roll off at low frequencies at the rate of 6 dB/octave (20 dB/decade) with a 3-dB frequency at $f_{P1} = \omega_{P1}/2\pi$, as indicated in Fig. 5.73(b).

Next, we consider the effect of C_E. For this purpose we assume that C_{C1} and C_{C2} are acting as perfect short circuits and thus obtain the circuit in Fig. 5.73(c). Reflecting r_e and C_E into the base circuit and utilizing the Thévenin theorem enables us to obtain the base current as

$$I_b = V_{\text{sig}} \frac{R_B}{R_B + R_{\text{sig}}} \frac{1}{(R_B \parallel R_{\text{sig}}) + (\beta + 1)\left(r_e + \dfrac{1}{sC_E}\right)}$$

The collector current can then be found as βI_b and the output voltage as

$$\begin{aligned} V_o &= -\beta I_b (R_C \parallel R_L) \\ &= -\frac{R_B}{R_B + R_{\text{sig}}} \frac{\beta (R_C \parallel R_L)}{(R_B \parallel R_{\text{sig}}) + (\beta + 1)\left(r_e + \dfrac{1}{sC_E}\right)} V_{\text{sig}} \end{aligned}$$

Thus the voltage gain including the effect of C_E can be expressed as

$$\frac{V_o}{V_{\text{sig}}} = -\frac{R_B}{R_B + R_{\text{sig}}} \frac{\beta (R_C \parallel R_L)}{(R_B \parallel R_{\text{sig}}) + (\beta + 1) r_e} \frac{s}{s + \left[1/C_E\left(r_e + \dfrac{R_B \parallel R_{\text{sig}}}{\beta + 1}\right)\right]} \tag{5.179}$$

We observe that C_E introduces the STC high-pass factor on the extreme right-hand side. Thus C_E causes the gain to fall off at low frequency at the rate of 6 dB/octave with a 3-dB frequency equal to the corner or break frequency of the high-pass STC factor; that is,

$$\omega_{P2} = \frac{1}{C_E\left[r_e + \dfrac{R_B \parallel R_{\text{sig}}}{\beta + 1}\right]} \tag{5.180}$$

Observe that $[r_e + ((R_B \parallel R_{\text{sig}})/(\beta + 1))]$ *is the resistance seen between the two terminals of* C_E *when* V_{sig} *is set to zero*. The effect of C_E on the amplifier frequency response is illustrated by the sketch in Fig. 5.73(c).

Finally, we consider the effect of C_{C2}. The circuit with C_{C1} and C_E assumed to be acting as perfect short circuits is shown in Fig. 5.73(d), for which we can write

$$V_\pi = V_{\text{sig}} \frac{R_B \parallel r_\pi}{(R_B \parallel r_\pi) + R_{\text{sig}}}$$

and

$$V_o = -g_m V_\pi \frac{R_C}{R_C + \dfrac{1}{sC_{C2}} + R_L} R_L$$

These two equations can be combined to obtain the low-frequency gain including the effect of C_{C2} as

$$\frac{V_o}{V_{\text{sig}}} = -\frac{R_B \parallel r_\pi}{(R_B \parallel r_\pi) + R_{\text{sig}}} g_m (R_C \parallel R_L) \left[\frac{s}{s + \dfrac{1}{C_{C2}(R_C + R_L)}} \right] \tag{5.181}$$

We observe that C_{C2} introduces the frequency-dependent factor between the square brackets, which we recognize as the transfer function of a high-pass STC network with a break frequency ω_{P3},

$$\omega_{P3} = \frac{1}{C_{C2}(R_C + R_L)} \tag{5.182}$$

Here we note that as expected, $(R_C + R_L)$ *is the resistance seen between the terminals of* C_{C2} *when* V_{sig} *is set to zero*. Thus capacitor C_{C2} causes the low-frequency gain of the amplifier to decrease at the rate of 6 dB/octave with a 3-dB frequency at $f_{P3} = \omega_{P3}/2\pi$, as illustrated by the sketch in Fig. 5.73(d).

Now that we have determined the effects of C_{C1} and of C_{C2} acting alone, the question becomes what will happen when all three are present at the same time. This question has two parts: First, what happens when all three capacitors are present but do not interact? The answer is that the amplifier low-frequency gain can be expressed as

$$\frac{V_o}{V_{\text{sig}}} = -A_M \left(\frac{s}{s + \omega_{P1}} \right) \left(\frac{s}{s + \omega_{P2}} \right) \left(\frac{s}{s + \omega_{P3}} \right) \tag{5.183}$$

from which we see that it acquires three break frequencies at f_{P1}, f_{P2}, and f_{P3}, all in the low-frequency band. If the three frequencies are widely separated, their effects will be distinct, as indicated by the sketch in Fig. 5.73(e). The important point to note here is that the 3-dB frequency f_L *is determined by the highest of the three break frequencies*. This is usually the break frequency caused by the bypass capacitor C_E, simply because the resistance that it sees is usually quite small. Thus, even if one uses a large value for C_E, f_{P2} is usually the highest of the three break frequencies.

If f_{P1}, f_{P2}, and f_{P3} are close together, none of the three dominates, and to determine f_L, we have to evaluate $|V_o/V_{\text{sig}}|$ in Eq. (5.183) and calculate the frequency at which it drops to $|A_M|/\sqrt{2}$. The work involved in doing this, however, is usually too great and is rarely justified in practice, particularly because in any case, Eq. (5.183) is an approximation based on the assumption that the three capacitors do not interact. This leads to the second part of the question: What happens when all three capacitors are present and interact? We do know that C_{C1} and C_E usually interact and that their combined effect is two poles at frequencies that will differ from ω_{P1} and ω_{P2}. Of course, one can derive the overall transfer function taking this interaction into account and find more precisely the low-frequency response. This, however, will be too complicated to yield additional insight. As an alternative, for hand

calculations we can obtain a reasonably good estimate for f_L using the following formula (which we will not derive here)[11]:

$$f_L \cong \frac{1}{2\pi}\left[\frac{1}{C_{C1}R_{C1}} + \frac{1}{C_E R_E} + \frac{1}{C_{C2}R_{C2}}\right] \tag{5.184}$$

or equivalently,

$$f_L = f_{P1} + f_{P2} + f_{P3} \tag{5.185}$$

where R_{C1}, R_E, and R_{C2} are the resistances seen by C_{C1}, C_E, and C_{C2}, respectively, when V_{sig} is set to zero. Equations (5.184) and (5.185) provide insight regarding the relative contributions of the three capacitors to f_L. Finally, we note that a far more precise determination of the low-frequency gain and the 3-dB frequency f_L can be obtained using SPICE (Section 5.11).

Selecting Values for C_{C1}, C_E, and C_{C2} We now address the design issue of selecting appropriate values for C_{C1}, C_E, and C_{C2}. The design objective is to place the lower 3-dB frequency f_L at a specified location while minimizing the capacitor values. Since as mentioned above C_E usually sees the lowest of the three resistances, the total capacitance is minimized by selecting C_E so that its contribution to f_L is dominant. That is, by reference to Eq. (5.184), we may select C_E such that $1/(C_E R_E)$ is, say, 80% of $\omega_L = 2\pi f_L$, leaving each of the other capacitors to contribute 10% to the value of ω_L. Example 5.19 should help to illustrate this process.

EXAMPLE 5.19

We wish to select appropriate values for C_{C1}, C_{C2}, and C_E for the common-emitter amplifier whose high-frequency response was analyzed in Example 5.18. The amplifier has $R_B = 100$ kΩ, $R_C = 8$ kΩ, $R_L = 5$ kΩ, $R_{\text{sig}} = 5$ kΩ, $\beta_0 = 100$, $g_m = 40$ mA/V, and $r_\pi = 2.5$ kΩ. It is required to have $f_L = 100$ Hz.

Solution

We first determine the resistances seen by the three capacitors C_{C1}, C_E, and C_{C2} as follows:

$$\begin{aligned} R_{C1} &= (R_B \parallel r_\pi) + R_{\text{sig}} \\ &= (100 \parallel 2.5) + 5 = 7.44 \text{ kΩ} \\ R_E &= r_e + \frac{R_B \parallel R_{\text{sig}}}{\beta + 1} \\ &= 0.025 + \frac{100 \parallel 5}{101} = 0.072 \text{ kΩ} = 72 \text{ Ω} \\ R_{C2} &= R_C + R_L = 8 + 5 = 13 \text{ kΩ} \end{aligned}$$

Now, selecting C_E so that it contributes 80% of the value of ω_L gives

$$\begin{aligned} \frac{1}{C_E \times 72} &= 0.8 \times 2\pi \times 100 \\ C_E &= 27.6 \ \mu\text{F} \end{aligned}$$

[11] The interested reader can refer to Chapter 7 of the fourth edition of this book.

Next, if C_{C1} is to contribute 10% of f_L,

$$\frac{1}{C_{C1} \times 7.44 \times 10^3} = 0.1 \times 2\pi \times 100$$

$$C_{C1} = 2.1\ \mu\text{F}$$

Similarly, if C_{C2} is to contribute 10% of f_L, its value should be selected as follows:

$$\frac{1}{C_{C2} \times 13 \times 10^3} = 0.1 \times 2\pi \times 100$$

$$C_{C2} = 1.2\ \mu\text{F}$$

In practice, we would select the nearest standard values for the three capacitors while ensuring that $f_L \geq 100$ Hz.

EXERCISE

5.52 A common-emitter amplifier has $C_{C1} = C_E = C_{C2} = 1\ \mu$F, $R_B = 100$ kΩ, $R_{\text{sig}} = 5$ kΩ, $g_m = 40$ mA/V, $r_\pi = 2.5$ kΩ, $R_C = 8$ kΩ, and $R_L = 5$ kΩ. Assuming that the three capacitors do not interact, find f_{P1}, f_{P2}, and f_{P3} and hence estimate f_L.

Ans. 21.4 Hz; 2.21 kHz; 12.2 Hz; since $f_{P2} \gg f_{P1}$ and f_{P3}, $f_L \cong f_{P2} = 2.21$ kHz; using Eq. (5.185), a somewhat better estimate for f_L is 2.24 kHz

5.9.4 A Final Remark

The frequency response of the other amplifier configurations will be studied in Chapter 8.

5.10 THE BASIC BJT DIGITAL LOGIC INVERTER

The most fundamental component of a digital system is the logic inverter. In Section 1.7, the inverter was studied at a conceptual level, and the realization of the inverter using voltage-controlled switches was presented. Having studied the BJT, we can now consider its application in the realization of a simple logic inverter. Such a circuit is shown in Fig. 5.74. The reader will note that we have already studied this circuit in some detail. In fact, we used it in

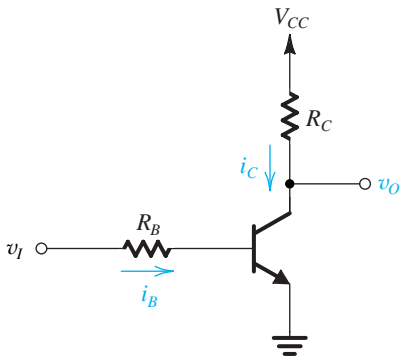


FIGURE 5.74 Basic BJT digital logic inverter.

Section 5.3.4 to illustrate the operation of the BJT as a switch. The operation of the circuit as a logic inverter makes use of the cutoff and saturation modes. In very simple terms, if the input voltage v_I is "high," at a value close to the power-supply voltage V_{CC}, representing a logic 1 in a positive-logic system, the transistor will be conducting and, with appropriate choice of values for R_B and R_C, saturated. Thus the output voltage will be $V_{CE\,\text{sat}} \cong 0.2$ V, representing a "low" or logic 0. Conversely, if the input voltage is "low," at a value close to ground (e.g., $V_{CE\text{sat}}$), then the transistor will be cut off, i_C will be zero, and $v_O = V_{CC}$, which is "high" or logic 1.

The choice of cutoff and saturation as the two modes of operation of the BJT in this inverter circuit is motivated by the following two factors:

1. The power dissipation in the circuit is relatively low in both cutoff and saturation: In cutoff all currents are zero (except for very small leakage currents), and in saturation the voltage across the transistor is very small ($V_{CE\text{sat}}$).
2. The output voltage levels (V_{CC} and $V_{CE\text{sat}}$) are well defined. In contrast, if the transistor is operated in the active region, $v_O = V_{CC} - i_C R_C = V_{CC} - \beta i_B R_C$, which is highly dependent on the rather ill-controlled transistor parameter β.

5.10.1 The Voltage Transfer Characteristic

As mentioned in Section 1.7, the most useful characterization of an inverter circuit is in terms of its voltage transfer characteristic, v_O versus v_I. A sketch of the voltage transfer characteristic (VTC) of the inverter circuit of Fig. 5.74 is presented in Fig. 5.75. The transfer characteristic is approximated by three straight-line segments corresponding to the operation of the BJT in the cutoff, active, and saturation regions, as indicated. The actual transfer characteristic will obviously be a smooth curve but will closely follow the straight-line asymptotes indicated. We shall now compute the coordinates of the breakpoints of the transfer

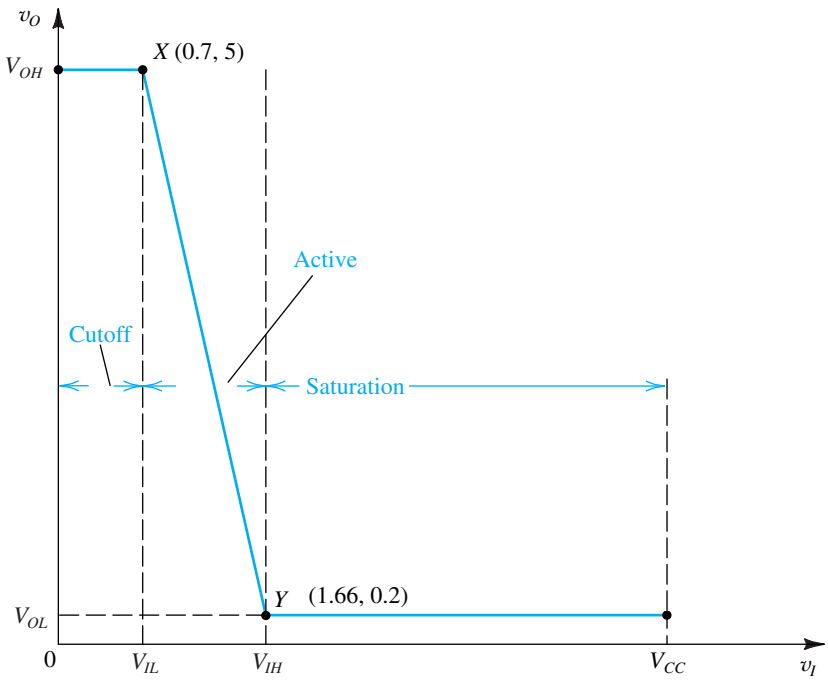


FIGURE 5.75 Sketch of the voltage transfer characteristic of the inverter circuit of Fig. 5.74 for the case $R_B = 10$ kΩ, $R_C = 1$ kΩ, $\beta = 50$, and $V_{CC} = 5$ V. For the calculation of the coordinates of X and Y, refer to the text.

characteristic of Fig. 5.75 for a representative case—$R_B = 10\ \text{k}\Omega$, $R_C = 1\ \text{k}\Omega$, $\beta = 50$, and $V_{CC} = 5$ V—as follows:

1. At $v_I = V_{OL} = V_{CE\text{sat}} = 0.2$ V, $v_O = V_{OH} = V_{CC} = 5$ V.
2. At $v_I = V_{IL}$, the transistor begins to turn on; thus,
$$V_{IL} \cong 0.7\ \text{V}$$
3. For $V_{IL} < v_I < V_{IH}$, the transistor is in the active region. It operates as an amplifier whose small-signal gain is
$$A_v \equiv \frac{v_o}{v_i} = -\beta\frac{R_C}{R_B + r_\pi}$$
The gain depends on the value of r_π, which in turn is determined by the collector current and hence by the value of v_I. As the current through the transistor increases, r_π decreases and we can neglect r_π relative to R_B, thus simplifying the gain expression to
$$A_v \cong -\beta\frac{R_C}{R_B} = -50 \times \frac{1}{10} = -5\ \text{V/V}$$
4. At $v_I = V_{IH}$, the transistor enters the saturation region. Thus V_{IH} is the value of v_I that results in the transistor being at the edge of saturation,
$$I_B = \frac{(V_{CC} - V_{CE\text{sat}})/R_C}{\beta}$$
For the values we are using, we obtain $I_B = 0.096$ mA, which can be used to find V_{IH},
$$V_{IH} = I_B R_B + V_{BE} = 1.66\ \text{V}$$
5. For $v_I = V_{OH} = 5$ V, the transistor will be deep into saturation with $v_O = V_{CE\text{sat}} \cong 0.2$ V, and
$$\beta_{\text{forced}} = \frac{(V_{CC} - V_{CE\text{sat}})/R_C}{(V_{OH} - V_{BE})/R_B}$$
$$= \frac{4.8}{0.43} = 1.1$$
6. The noise margins can now be computed using the formulas from Section 1.7,
$$NM_H = V_{OH} - V_{IH} = 5 - 1.66 = 3.34\ \text{V}$$
$$NM_L = V_{IL} - V_{OL} = 0.7 - 0.2 = 0.5\ \text{V}$$
Obviously, the two noise margins are vastly different, making this inverter circuit less than ideal.
7. The gain in the transition region can be computed from the coordinates of the breakpoints X and Y,
$$\text{Voltage gain} = -\frac{5 - 0.2}{1.66 - 0.7} = -5\ \text{V/V}$$
which is equal to the approximate value found above (the fact that it is exactly the same value is a coincidence).

5.10.2 Saturated Versus Nonsaturated BJT Digital Circuits

The inverter circuit just discussed belongs to the saturated variety of BJT digital circuits. A historically significant family of saturated BJT logic circuits is **transistor-transistor logic**

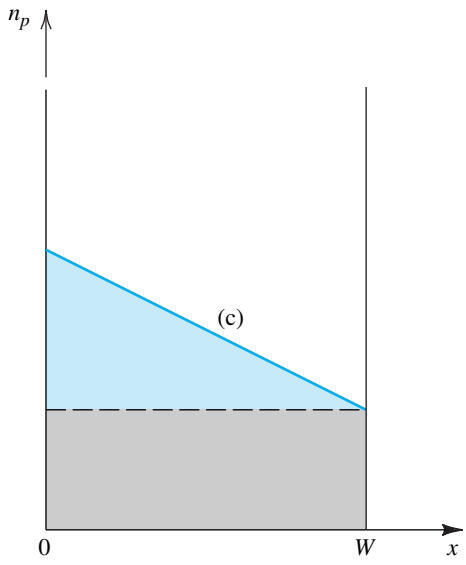


FIGURE 5.76 The minority-carrier charge stored in the base of a saturated transistor can be divided into two components: That in blue produces the gradient that gives rise to the diffusion current across the base, and that in gray results in driving the transistor deeper into saturation.

(TTL). Although some versions of TTL remains in use, saturated bipolar digital circuits generally are no longer the technology of choice in digital system design. This is because their speed of operation is severely limited by the relatively long time delay required to turn off a saturated transistor, as we will now explain briefly.

In our study of BJT saturation in Section 5.1.5, we made use of the minority-carrier distribution in the base region (see Fig. 5.10). Such a distribution is shown in Fig. 5.76, where the minority carrier charge stored in the base has been divided into two components: The component represented by the blue triangle produces the gradient that gives rise to the diffusion current across the base; the other component, represented by the gray rectangle, causes the transistor to be driven deeper into saturation. The deeper the transistor is driven into saturation (i.e., the greater the base overdrive factor is), the greater the amount of the "gray" component of the stored charge will be. It is this "extra" stored base charge that represents a serious problem when it comes to turning off the transistor: Before the collector current can begin to decrease, all of the extra stored charge must first be removed. This adds a relatively large component to the turn-off time of a saturated transistor.

From the above we conclude that to achieve high operating speeds, the BJT should not be allowed to saturate. This is the case in **current-mode logic** and its particular form, emitter-coupled logic (ECL), which will be studied briefly in Chapter 12. There we will show that ECL is currently the highest-speed logic-circuit family available. It is based on the current-switching arrangement that was discussed conceptually in Section 1.7 (Fig. 1.33).

EXERCISE

5.53 Consider the inverter of Fig. 5.74 when v_I is low. Let the output be connected to the input terminals of N identical inverters. Convince yourself that the output level V_{OH} can be determined using the equivalent circuit shown in Fig. E5.53. Hence show that

$$V_{OH} = V_{CC} - R_C \frac{V_{CC} - V_{BE}}{R_C + R_B/N}$$

For $N = 5$, calculate V_{OH} using the component values of the example circuit discussed earlier (i.e., $R_B = 10\ \text{k}\Omega$, $R_C = 1\ \text{k}\Omega$, $V_{CC} = 5\ \text{V}$).

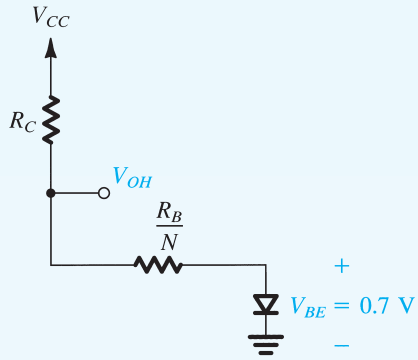


FIGURE E5.53

Ans. 3.6 V

5.11 THE SPICE BJT MODEL AND SIMULATION EXAMPLES

SUMMARY

- Depending on the bias conditions on its two junctions, the BJT can operate in one of four possible modes: cutoff (both junctions reverse biased), active (the EBJ forward biased and the CBJ reverse biased), saturation (both junctions forward biased), and reverse-active (the EBJ reverse biased and the CBJ forward biased).
- For amplifier applications, the BJT is operated in the active mode. Switching applications make use of the cutoff and saturation modes. The reverse-active mode of operation is of conceptual interest only.
- A BJT operating in the active mode provides a collector current $i_C = I_S e^{|v_{BE}|/V_T}$. The base current $i_B = (i_C/\beta)$, and the emitter current $i_E = i_C + i_B$. Also, $i_C = \alpha i_E$, and thus $\beta = \alpha/(1-\alpha)$ and $\alpha = \beta/(\beta+1)$. See Table 5.2.
- To ensure operation in the active mode, the collector voltage of an *npn* transistor must be kept higher than approximately 0.4 V below the base voltage. For a *pnp* transistor the collector voltage must be lower than approximately 0.4 V above the base voltage. Otherwise, the CBJ becomes forward biased, and the transistor enters the saturation region.
- A convenient and intuitively appealing model for the large-signal operation of the BJT is the Ebers-Moll model shown in Fig. 5.8. A fundamental relationship between its parameters is $\alpha_F I_{SE} = \alpha_R I_{SC} = I_S$. While α_F is close to unity, α_R is very small (0.01–0.2), and β_R is correspondingly small. Use of the EM model enables expressing the terminal currents in terms of the voltages v_{BE} and v_{BC}. The resulting relationships are given in Eqs. (5.26) to (5.29).
- In a saturated transistor, $|V_{CE\text{sat}}| \simeq 0.2$ V and $I_{C\text{sat}} = (V_{CC} - V_{CE\text{sat}})/R_C$. The ratio of $I_{C\text{sat}}$ to the base current is the forced β, which is lower than β. The collector-to-emitter resistance, $R_{CE\text{sat}}$, is small (few tens of ohms).
- At a constant collector current, the magnitude of the base–emitter voltage decreases by about 2 mV for every 1°C rise in temperature.
- With the emitter open-circuited ($i_E = 0$), the CBJ breaks down at a reverse voltage BV_{CBO} that is typically >50 V. For $i_E > 0$, the breakdown voltage is less than BV_{CBO}. In the common-emitter configuration the breakdown voltage specified is BV_{CEO}, which is about half BV_{CBO}. The emitter–base junction breaks down at a reverse bias of 6 V to 8 V. This breakdown usually has an adverse effect on β.
- A summary of the current-voltage characteristics and large-signal models of the BJTs in both the active and saturation modes of operation is presented in Table 5.3.
- The dc analysis of transistor circuits is greatly simplified by assuming that $|V_{BE}| \simeq 0.7$ V.
- To operate as a linear amplifier, the BJT is biased in the active region and the signal v_{be} is kept small ($v_{be} \ll V_T$).
- For small signals, the BJT functions as a linear voltage-controlled current source with a transconductance $g_m = (I_C/V_T)$. The input resistance between base and emitter, looking into the base, is $r_\pi = \beta/g_m$. Simplified low-frequency equivalent-circuit models for the BJT are shown in Figs. 5.51 and 5.52. These models can be augmented by including the output resistance $r_o = |V_A|/I_C$ between the collector and the emitter. Table 5.4 provides a summary of the equations for determining the model parameters.
- Bias design seeks to establish a dc collector current that is as independent of the value of β as possible.
- In the common-emitter configuration, the emitter is at signal ground, the input signal is applied to the base, and the output is taken at the collector. A high voltage gain and a reasonably high input resistance are obtained, but the high-frequency response is limited.
- The input resistance of the common-emitter amplifier can be increased by including an unbypassed resistance in the emitter lead. This emitter-degeneration resistance provides other performance improvements at the expense of reduced voltage gain.
- In the common-base configuration, the base is at signal ground, the input signal is applied to the emitter, and the output is taken at the collector. A high voltage gain (from emitter to collector) and an excellent high-frequency response are obtained, but the input resistance is very low. The CB amplifier is useful as a current buffer.
- In the emitter follower the collector is at signal ground, the input signal is applied to the base, and the output taken at the emitter. Although the voltage gain is less than unity, the input resistance is very high and the output resistance is very low. The circuit is useful as a voltage buffer.
- The basic BJT logic inverter utilizes the cutoff and saturation modes of transistor operation. A saturated transistor has a large amount of minority-carrier charge stored in its base region and is thus slow to turn off.
- Table 5.5 shows the parameters utilized to characterize amplifiers.
- For a summary of the characteristics of discrete single-stage BJT amplifiers, refer to Table 5.6.
- The high-frequency model of the BJT together with the formulas for determining its parameter values are shown in Table 5.7.

- Analysis of the high-frequency gain of the CE amplifier in Section 5.9 shows that it rolls off at a slope of –6 dB/octave with the 3-dB frequency $f_H = 1/2\pi C_{in} R'_{sig}$. Here R'_{sig} is a modified value of R_{sig}, approximately equal to $R_{sig} \| r_\pi$, and $C_{in} = C_\pi + (1 + g_m R'_L) C_\mu$. The multiplication of C_μ by $(1 + g_m R'_L)$ is known as the Miller effect, and it is the most significant factor in limiting the high-frequency response of the CE amplifier.
- For the analysis of the effect of C_{C1}, C_{C2}, and C_E on the low-frequency gain of the CE amplifier, refer to Section 5.9.3 and in particular to Fig. 5.73.

PROBLEMS

SECTION 5.1: DEVICE STRUCTURE AND PHYSICAL OPERATION

5.1 The terminal voltages of various *npn* transistors are measured during operation in their respective circuits with the following results:

Case	E	B	C	Mode
1	0	0.7	0.7	
2	0	0.8	0.1	
3	–0.7	0	0.7	
4	–0.7	0	–0.6	
5	0.7	0.7	0	
6	–2.7	–2.0	0	
7	0	0	5.0	
8	–0.10	5.0		

In this table, where the entries are in volts, 0 indicates the reference terminal to which the black (negative) probe of the voltmeter is connected. For each case, identify the mode of operation of the transistor.

5.2 An *npn* transistor has an emitter area of 10 μm × 10 μm. The doping concentrations are as follows: in the emitter $N_D = 10^{19}/\text{cm}^3$, in the base $N_A = 10^{17}/\text{cm}^3$, and in the collector $N_D = 10^{15}/\text{cm}^3$. The transistor is operating at $T = 300$ K, where $n_i = 1.5 \times 10^{10}/\text{cm}^3$. For electrons diffusing in the base, $L_n = 19$ μm and $D_n = 21.3$ cm^2/s. For holes diffusing in the emitter, $L_p = 0.6$ μm and $D_p = 1.7$ cm^2/s. Calculate I_S and β assuming that the base-width W is:

(a) 1 μm
(b) 2 μm
(c) 5 μm

For case (b), if $I_C = 1$ mA, find I_B, I_E, V_{BE}, and the minority-carrier charge stored in the base. (*Hint:* $\tau_b = L_n^2/D_n$. Recall that the electron charge $q = 1.6 \times 10^{-19}$ Coulomb.)

5.3 Two transistors, fabricated with the same technology but having different junction areas, when operated at a base-emitter voltage of 0.72 V, have collector currents of 0.2 mA and 12 mA. Find I_S for each device. What are the relative junction areas?

5.4 In a particular BJT, the base current is 7.5 μA, and the collector current is 400 μA. Find β and α for this device.

5.5 Find the values of β that correspond to α values of 0.5, 0.8, 0.9, 0.95, 0.99, 0.995, and 0.999.

5.6 Find the values of α that correspond to β values of 1, 2, 10, 20, 100, 200, 1000, and 2000.

5.7 Measurement of V_{BE} and two terminal currents taken on a number of *npn* transistors are tabulated below. For each, calculate the missing current value as well as α, β, and I_S as indicated by the table.

Transistor	a	b	c	d	e
V_{BE} (mV)	690	690	580	780	820
I_C (mA)	1.000	1.000		10.10	
I_B (μA)	50		7	120	1050
I_E (mA)		1.070	0.137		75.00
α					
β					
I_S					

5.8 Consider an *npn* transistor whose base–emitter drop is 0.76 V at a collector current of 10 mA. What current will it conduct at $v_{BE} = 0.70$ V? What is its base–emitter voltage for $i_C = 10$ μA?

5.9 Show that for a transistor with α close to unity, if α changes by a small per-unit amount $(\Delta\alpha/\alpha)$ the corresponding per-unit change in β is given approximately by

$$\frac{\Delta\beta}{\beta} \simeq \beta\left(\frac{\Delta\alpha}{\alpha}\right)$$

5.10 An *npn* transistor of a type whose β is specified to range from 60 to 300 is connected in a circuit with emitter grounded, collector at +9 V, and a current of 50 μA injected into the base. Calculate the range of collector and emitter currents that can result. What is the maximum power dissipated in the transistor? (*Note:* Perhaps you can see why this is a bad way to establish the collector operating current in a BJT.)

5.11 A particular BJT when conducting a collector current of 10 mA is known to have $v_{BE} = 0.70$ V and $i_B = 100$ μA. Use these data to create specific transistor models of the form shown in Figs. 5.5(a) and (b).

5.12 Using the *npn* transistor model of Fig. 5.5(b), consider the case of a transistor for which the base is connected to ground, the collector is connected to a 10-V dc source through a 2-kΩ resistor, and a 3-mA current source is connected to the emitter with the polarity so that current is drawn out of the emitter terminal. If $\beta = 100$ and $I_S = 10^{-15}$ A, find the voltages at the emitter and the collector and calculate the base current.

5.13 Consider an *npn* transistor for which $\beta_F = 100$, $\alpha_R = 0.1$, and $I_S = 10^{-15}$ A.

(a) If the transistor is operated in the forward active mode with $I_B = 10\ \mu$A and $V_{CB} = 1$ V, find V_{BE}, I_C, and I_E.
(b) Now, operate the transistor in the reverse active mode with a forward-bias voltage V_{BC} equal to the value of V_{BE} found in (a) and with $V_{EB} = 1$ V. Find I_C, I_B, and I_E.

5.14 A transistor characterized by the Ebers-Moll model shown in Fig. 5.8 is operated with both emitter and collector grounded and a base current of 1 mA. If the collector junction is 10 times larger than the emitter junction and $\alpha_F \cong 1$, find i_C and i_E.

***5.15** (a) Use the Ebers-Moll expressions in Eqs. (5.26) and (5.27) to show that the i_C–v_{CB} relationship sketched in Fig. 5.9 can be described by

$$i_C = \alpha_F I_E - I_S\left(\frac{1}{\alpha_R} - \alpha_F\right)e^{v_{BC}/V_T}$$

(b) Calculate and sketch i_C–v_{CB} curves for a transistor for which $I_S = 10^{-15}$ A, $\alpha_F \cong 1$, and $\alpha_R = 0.1$. Sketch graphs for $I_E = 0.1$ mA, 0.5 mA, and 1 mA. For each, give the values of v_{BC}, v_{BE}, and v_{CE} for which $i_C = 0.5\alpha_F I_E$ and $i_C = 0$.

5.16 Consider the *pnp* large-signal model of Fig. 5.12(b) applied to a transistor having $I_S = 10^{-13}$ A and $\beta = 40$. If the emitter is connected to ground, the base is connected to a current source that pulls out of the base terminal a current of 20 μA, and the collector is connected to a negative supply of −10 V via a 10-kΩ resistor, find the collector voltage, the emitter current, and the base voltage.

5.17 A *pnp* transistor has $v_{EB} = 0.8$ V at a collector current of 1 A. What do you expect v_{EB} to become at $i_C = 10$ mA? At $i_C = 5$ A?

5.18 A *pnp* transistor modeled with the circuit in Fig. 5.12 is connected with its base at ground, collector at –1.5 V, and a 10-mA current injected into its emitter. If it is said to have $\beta = 10$, what are its base and collector currents? In which direction do they flow? If $I_S = 10^{-16}$ A, what voltage results at the emitter? What does the collector current become if a transistor with $\beta = 1000$ is substituted? (*Note:* The fact that the collector current changes by less than 10% for a large change of β illustrates that this is a good way to establish a specific collector current.)

5.19 A *pnp* power transistor operates with an emitter-to-collector voltage of 5 V, an emitter current of 10 A, and $V_{EB} = 0.85$ V. For $\beta = 15$, what base current is required? What is I_S for this transistor? Compare the emitter–base junction area of this transistor with that of a small-signal transistor that conducts $i_C = 1$ mA with $v_{EB} = 0.70$ V. How much larger is it?

SECTION 5.2: CURRENT-VOLTAGE CHARACTERISTICS

5.20 For the circuits in Fig. P5.20, assume that the transistors have very large β. Some measurements have been made

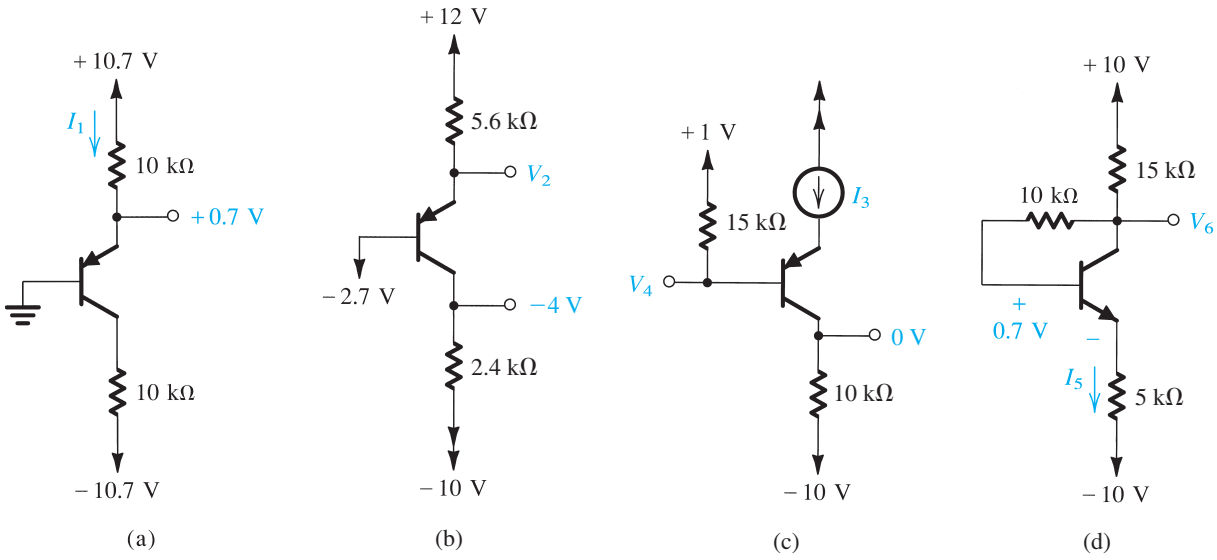


FIGURE P5.20

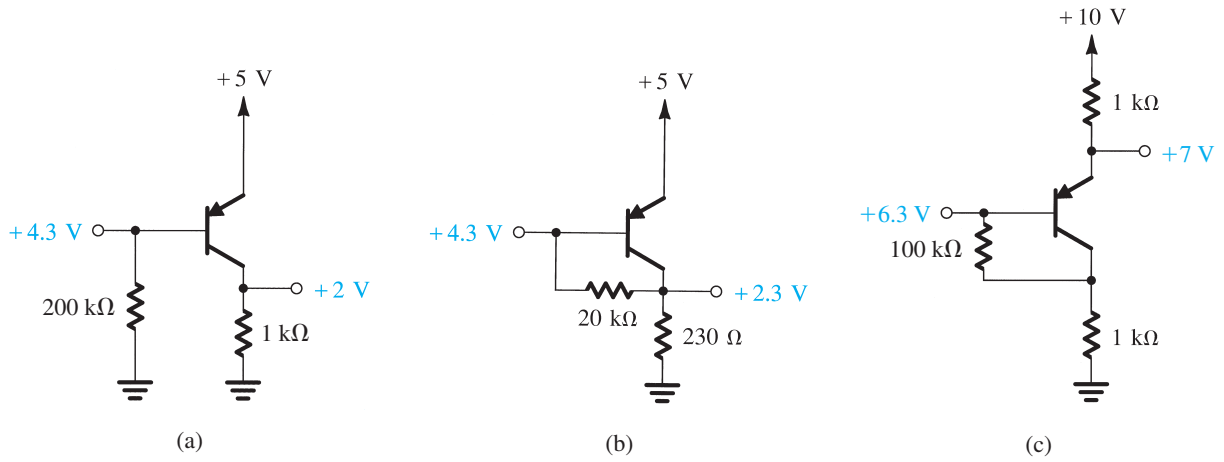


FIGURE P5.21

on these circuits, the results are indicated in the figure. Find the values of the other labeled voltages and currents.

5.21 Measurements on the circuits of Fig. P5.21 produce labeled voltages as indicated. Find the value of β for each transistor.

D5.22 Examination of the table of standard values for resistors with 5% tolerance in Appendix X reveals that the closest values to those found in the design of Example 5.1 are 5.1 kΩ and 6.8 kΩ. For these values use approximate calculations (e.g., $V_{BE} \simeq 0.7$ V and $\alpha \simeq 1$) to determine the values of collector current and collector voltage that are likely to result.

D5.23 Redesign the circuit in Example 5.1 to provide $V_C = +3$ V and $I_C = 5$ mA.

5.24 For each of the circuits shown in Fig. P5.24, find the emitter, base, and collector voltages and currents. Use $\beta = 30$, but assume $|V_{BE}| = 0.7$ V independent of current level.

5.25 Repeat Problem 5.24 using transistors for which $|V_{BE}| = 0.7$ V at $I_C = 1$ mA.

5.26 For the circuit shown in Fig. P5.26, measurement indicates that $V_B = -1.5$ V. Assuming $V_{BE} = 0.7$ V, calculate V_E, α, β, and V_C. If a transistor with $\beta = \infty$ is used, what values of V_B, V_E, and V_C result?

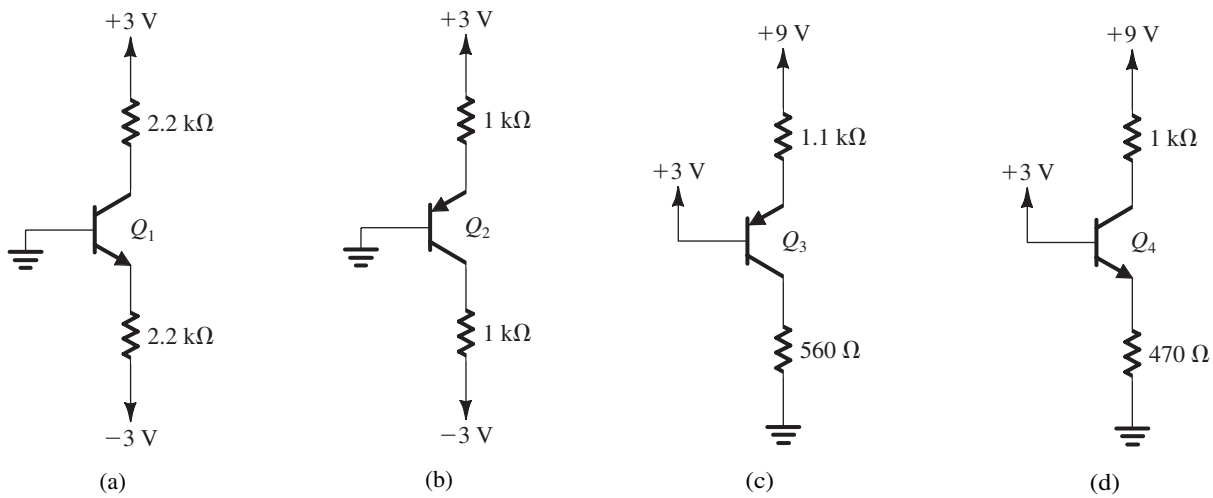


FIGURE P5.24

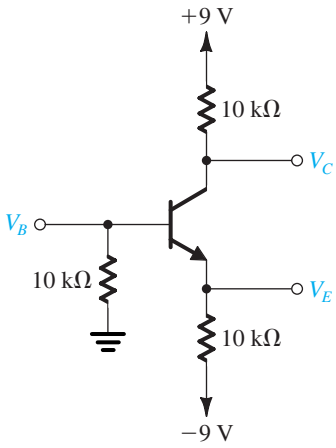


FIGURE P5.26

5.27 The current I_{CBO} of a small transistor is measured to be 20 nA at 25°C. If the temperature of the device is raised to 85°C, what do you expect I_{CBO} to become?

***5.28** Augment the model of the *npn* BJT shown in Fig. 5.20(a) by a current source representing I_{CBO}. In terms of this addition, what do the terminal currents i_B, i_C, and i_E become? If the base lead is open-circuited while the emitter is connected to ground and the collector is connected to a positive supply, find the emitter and collector currents.

5.29 An *npn* transistor is accidentally connected with collector and emitter leads interchanged. The resulting currents in the normal emitter and base leads are 0.5 mA and 1 mA, respectively. What are the values of α_R and β_R?

5.30 A BJT whose emitter current is fixed at 1 mA has a base–emitter voltage of 0.69 V at 25°C. What base–emitter voltage would you expect at 0°C? At 100°C?

5.31 A particular *pnp* transistor operating at an emitter current of 0.5 mA at 20°C has an emitter–base voltage of 692 mV.

(a) What does v_{EB} become if the junction temperature rises to 50°C?
(b) If the transistor has $n = 1$ and is operated at a fixed emitter–base voltage of 700 mV, what emitter current flows at 20°C? At 50°C?

5.32 Consider a transistor for which the base–emitter voltage drop is 0.7 V at 10 mA. What current flows for $V_{BE} = 0.5$ V?

5.33 In Problem 5.32, the stated voltages are measured at 25°C. What values correspond at –25°C? At 125°C?

5.34 Use the Ebers-Moll expressions in Eqs. (5.31) and (5.32) to derive Eq. (5.35). Note that the emitter current is set to a constant value I_E. Ignore the terms not involving exponentials.

5.35 Use Eq. (5.35) to plot the i_C–v_{CB} characteristics of an *npn* transistor having $\alpha_F \cong 1$, $\alpha_R = 0.1$, and $I_S = 10^{-15}$ A. Plot graphs for $I_E = 0.1$ mA, 0.5 mA, and 1 mA. Use an expanded scale for the negative values of v_{BC} in order to show the details of the saturation region. Neglect the Early effect.

***5.36** For the saturated transistor shown in Fig. P5.36, use the EM expressions to show that for $\alpha_F \cong 1$,

$$V_{CE\text{sat}} = V_T \ln\left(\frac{\frac{1}{\alpha_R} - \frac{I_{C\text{sat}}}{I_E}}{1 - \frac{I_{C\text{sat}}}{I_E}}\right)$$

For a BJT with $\alpha_R = 0.1$, evaluate $V_{CE\text{sat}}$ for $I_{C\text{sat}}/I_E = 0.9$, 0.5, 0.1, and 0.

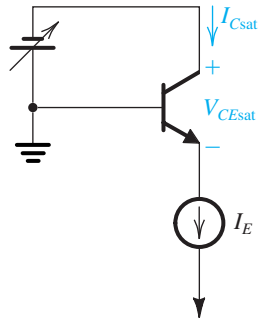


FIGURE P5.36

5.37 Use Eq. (5.36) to plot i_C versus v_{CE} for an *npn* transistor having $I_S = 10^{-15}$ A and $V_A = 100$ V. Provide curves for $v_{BE} = 0.65$, 0.70, 0.72, 0.73, and 0.74 volts. Show the characteristics for v_{CE} up to 15 V.

5.38 For a particular *npn* transistor operating at a v_{BE} of 670 mV and $I_C = 3$ mA, the i_C–v_{CE} characteristic has a slope of 3×10^{-5} ʊ. To what value of output resistance does this correspond? What is the value of the Early voltage for this transistor? For operation at 30 mA, what would the output resistance become?

5.39 For a BJT having an Early voltage of 200 V, what is its output resistance at 1 mA? At 100 μA?

5.40 Measurements of the i_C–v_{CE} characteristic of a small-signal transistor operating at $v_{BE} = 720$ mV show that $i_C = 1.8$ mA at $v_{CE} = 2$ V and that $i_C = 2.4$ mA at $v_{CE} = 14$ V. What is the corresponding value of i_C near saturation? At what value of v_{CE} is $i_C = 2.0$ mA? What is the value of the Early voltage for this transistor? What is the output resistance that corresponds to operation at $v_{BE} = 720$ mV?

5.41 Give the *pnp* equivalent circuit models that correspond to those shown in Fig. 5.20 for the *npn* case.

5.42 A BJT operating at $i_B = 8$ μA and $i_C = 1.2$ mA undergoes a reduction in base current of 0.8 μA. It is found that when v_{CE} is held constant, the corresponding reduction in collector current is 0.1 mA. What are the values of h_{FE} and h_{fe} that apply? If the base current is increased from 8 μA to 10 μA

and v_{CE} is increased from 8 V to 10 V, what collector current results? Assume $V_A = 100$ V.

5.43 For a transistor whose β characteristic is sketched in Fig. 5.22, estimate values of β at –55°C, 25°C, and 125°C for $I_C = 100$ μA and 10 mA. For each current, estimate the temperature coefficient for temperatures above and below room temperature (four values needed).

5.44 Figure P5.44 shows a diode-connected *npn* transistor. Since $v_{CB} = 0$ results in activemode operation, the BJT will internally operate in the active mode; that is, its base and collector currents will be related by β_F. Use the EM equations to show that the diode-connected transistor has the i–v characteristics,

$$i = \frac{I_S}{\alpha_F}(e^{v/V_T} - 1) \cong I_S e^{v/V_T}$$

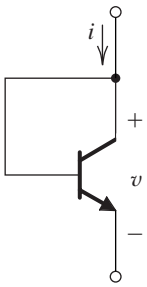


FIGURE P5.44

5.45 A BJT for which $\alpha_R = 0.2$ operates with a constant base current but with the collector open. What value of $V_{CE\text{sat}}$ would you measure?

5.46 Find the saturation voltage $V_{CE\text{sat}}$ and the saturation resistance $R_{CE\text{sat}}$ of an *npn* BJT operated at a constant base current of 0.1 mA and a forced β of 20. The transistor has $\beta_F = 50$ and $\beta_R = 0.2$.

***5.47** Use Eq. (5.47) to show that the saturation resistance $R_{CE\text{sat}} \equiv \partial v_{CE}/\partial i_C$ of a transistor operated with a constant base current I_B is given by

$$R_{CE\text{sat}} = \frac{V_T}{\beta_F I_B} \frac{1}{x(1-x)}$$

where

$$x = \frac{I_{C\text{sat}}}{\beta_F I_B} = \frac{\beta_{\text{forced}}}{\beta_F}$$

Find $R_{CE\text{sat}}$ for $\beta_{\text{forced}} = \beta_F/2$.

5.48 For a transistor for which $\beta_F = 70$ and $\beta_R = 0.7$, find an estimate of $R_{CE\text{sat}}$ and $V_{CE\text{off}}$ for $I_B = 2$ mA by evaluating $V_{CE\text{sat}}$ at $i_C = 3$ mA and at $i_C = 0.3$ mA (using Eq. 5.49). (*Note:* Because here we are modeling operation at a very low forced β, the value of $R_{CE\text{sat}}$ will be much larger than that given by Eq. 5.48).

5.49 A transistor has $\beta_F = 150$ and the collector junction is 10 times larger than the emitter junction. Evaluate $V_{CE\text{sat}}$ for $\beta_{\text{forced}}/\beta_F = 0.99$, 0.95, 0.9, 0.5, 0.1, 0.01, and 0.

5.50 A particular *npn* BJT with $v_{BE} = 720$ mV at $i_C = 600$ μA and, having $\beta = 150$, has a collector–base junction 20 times larger than the emitter–base junction.

(a) Find α_F, α_R, and β_R.
(b) For a collector current of 5 mA and nonsaturated operation, what is the base–emitter voltage and the base current?
(c) For the situation in (b) but with double the calculated base current, what is the value of forced β? What are the base–emitter and base–collector voltages? What are $V_{CE\text{sat}}$ and $R_{CE\text{sat}}$?

***5.51** A BJT with fixed base current has $V_{CE\text{sat}} = 60$ mV with the emitter grounded and the collector open-circuited. When the collector is grounded and the emitter is open-circuited, $V_{CE\text{sat}}$ becomes –1 mV. Estimate values for β_R and β_F for this transistor.

5.52 A BJT for which $I_B = 0.5$ mA has $V_{CE\text{sat}} = 140$ mV at $I_C = 10$ mA and $V_{CE\text{sat}} = 170$ mV at $I_C = 20$ mA. Estimate the values of its saturation resistance, $R_{CE\text{sat}}$, and its offset voltage, $V_{CE\text{off}}$. Also, determine the values of β_F and β_R.

5.53 A BJT for which BV_{CBO} is 30 V is connected as shown in Fig. P5.53. What voltages would you measure on the collector, base, and emitter?

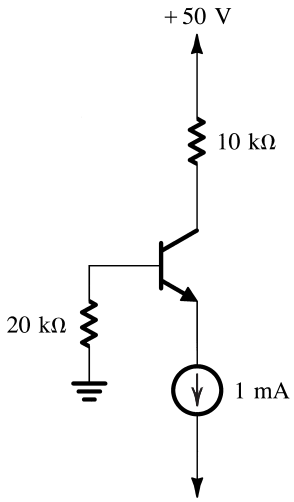


FIGURE P5.53

SECTION 5.3: THE BJT AS AN AMPLIFIER AND AS A SWITCH

5.54 A common-emitter amplifier circuit operated with $V_{CC} = +10$ V is biased at $V_{CE} = +1$ V. Find the voltage gain, the maximum allowed output negative swing without the transistor entering saturation, and the corresponding maximum input signal permitted.

5.55 For the common-emitter circuit in Fig. 5.26(a) with $V_{CC} = +10$ V and $R_C = 1$ kΩ, find V_{CE} and the voltage gain at the following dc collector bias currents: 1 mA, 2 mA, 5 mA, 8 mA, and 9 mA. For each, give the maximum possible positive- and

negative-output signal swing as determined by the need to keep the transistor in the active region. Present your results in a table.

D5.56 Consider the CE amplifier circuit of Fig. 5.26(a) when operated with a dc supply $V_{CC} = +5$ V. It is required to find the point at which the transistor should be biased; that is, find the value of V_{CE} so that the output sine-wave signal v_{ce} resulting from an input sine-wave signal v_{be} of 5-mV peak amplitude has the maximum possible magnitude. What is the peak amplitude of the output sine wave and the value of the gain obtained? Assume linear operation around the bias point. (*Hint:* To obtain the maximum possible output amplitude for a given input, you need to bias the transistor as close to the edge of saturation as possible without entering saturation at any time, that is, without v_{CE} decreasing below 0.3 V.)

5.57 The transistor in the circuit of Fig. P5.57 is biased at a dc collector current of 0.5 mA. What is the voltage gain? (*Hint:* Use the Thévenin theorem to convert the circuit to the form in Fig. 5.26a).

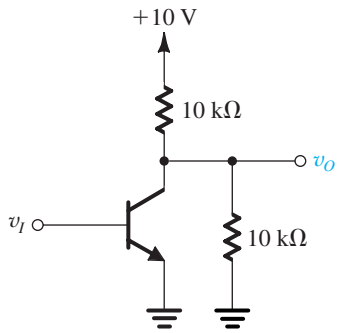


FIGURE P5.57

5.58 Sketch and label the voltage transfer characteristics of the *pnp* common-emitter amplifiers shown in Fig. P5.58.

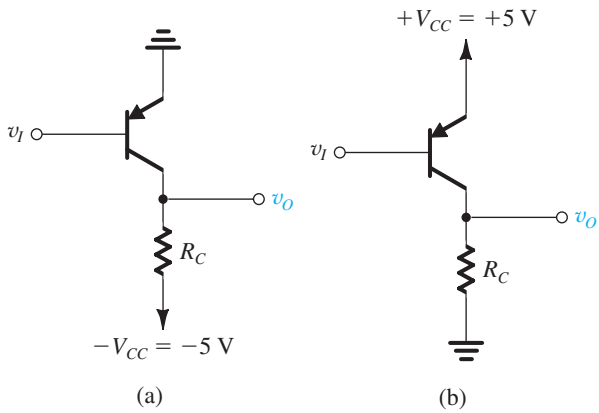


FIGURE P5.58

***5.59** In deriving the expression for small-signal voltage gain A_v in Eq. (5.56) we neglected the Early effect. Derive this expression including the Early effect, that is, by substituting

$$i_C = I_S e^{v_{BE}/V_T}\left(1 + \frac{v_{CE}}{V_A}\right)$$

in Eq. (5.50). Show that the gain expression changes to

$$A_v = \frac{-I_C R_C / V_T}{\left[1 + \dfrac{I_C R_C}{V_A + V_{CE}}\right]}$$

For the case $V_{CC} = 5$ V and $V_{CE} = 2.5$ V, what is the gain without and with the Early effect taken into account? Let $V_A = 100$ V.

5.60 When the common-emitter amplifier circuit of Fig. 5.26(a) is biased with a certain V_{BE}, the dc voltage at the collector was found to be +2 V. For $V_{CC} = +5$ V and $R_C = 1$ kΩ, find I_C and the small-signal voltage gain. For a change $\Delta v_{BE} = +5$ mV, calculate the resulting Δv_O. Calculate it two ways: by finding Δi_C using the transistor exponential characteristic and approximately using the small-signal voltage gain. Repeat for $\Delta v_{BE} = -5$ mV. Summarize your results in a table.

***5.61** Consider the common-emitter amplifier circuit of Fig. 5.26(a) when operated with a supply voltage $V_{CC} = +5$ V.

(a) What is the theoretical maximum voltage gain that this amplifier can provide?
(b) What value of V_{CE} must this amplifier be biased at to provide a voltage gain of –100 V/V?
(c) If the dc collector current I_C at the bias point is to be 0.5 mA, what value of R_C should be used?
(d) What is the value of V_{BE} required to provide the bias point mentioned above? Assume that the BJT has $I_S = 10^{-15}$ A.
(e) If a sine-wave signal v_{be} having a 5-mV peak amplitude is superimposed on V_{BE}, find the corresponding output voltage signal v_{ce} that will be superimposed on V_{CE} assuming linear operation around the bias point.
(f) Characterize the signal current i_c that will be superimposed on the dc bias current I_C?
(g) What is the value of the dc base current I_B at the bias point. Assume $\beta = 100$. Characterize the signal current i_b that will be superimposed on the base current I_B.
(h) Dividing the amplitude of v_{be} by the amplitude of i_b, evaluate the incremental (or small-signal) input resistance of the amplifier.
(i) Sketch and clearly label correlated graphs for v_{BE}, v_{CE}, i_C, and i_B. Note that each graph consists of a dc or average value and a superimposed sine wave. Be careful of the phase relationships of the sine waves.

5.62 The essence of transistor operation is that a change in v_{BE}, Δv_{BE}, produces a change in i_C, Δi_C. By keeping Δv_{BE} small, Δi_C is approximately linearly related to Δv_{BE}, $\Delta i_C \equiv g_m \Delta v_{BE}$, where g_m is known as the transistor transconductance. By passing Δi_C in R_C, an output voltage signal Δv_O is obtained. Use the expression for the small-signal voltage gain in Eq. (5.56) to derive an expression for g_m. Find the value of g_m for a transistor biased at $I_C = 1$ mA.

5.63 Consider the characteristic curves shown in Fig. 5.29 with the following additional calibration data: Label, from the lowest colored line, $i_B = 1$ μA, 10 μA, 20 μA, 30 μA, and 40 μA. Assume the lines to be horizontal, and let $\beta = 100$. For $V_{CC} = 5$ V and $R_C = 1$ kΩ, what peak-to-peak collector voltage swing will result for i_B varying over the range 10 μA to 40 μA? If at the bias point (not the one shown in the figure) $V_{CE} = \frac{1}{2}V_{CC}$, find the value of I_C and I_B. If at this current $V_{BE} = 0.7$ V and if $R_B = 100$ kΩ, find the required value of V_{BB}.

***5.64** Sketch the i_C–v_{CE} characteristics of an *npn* transistor having $\beta = 100$ and $V_A = 100$ V. Sketch characteristic curves for $i_B = 20$ μA, 50 μA, 80 μA, and 100 μA. For the purpose of this sketch, assume that $i_C = \beta i_B$ at $v_{CE} = 0$. Also, sketch the load line obtained for $V_{CC} = 10$ V and $R_C = 1$ kΩ. If the dc bias current into the base is 50 μA, write the equation for the corresponding i_C–v_{CE} curve. Also, write the equation for the load line, and solve the two equations to obtain V_{CE} and I_C. If the input signal causes a sinusoidal signal of 30-μA peak amplitude to be superimposed on I_B, find the corresponding signal components of i_C and v_{CE}.

D5.65 For the circuit in Fig. P5.65 select a value for R_B so that the transistor saturates with an overdrive factor of 10. The BJT is specified to have a minimum β of 20 and $V_{CEsat} = 0.2$ V. What is the value of forced β achieved?

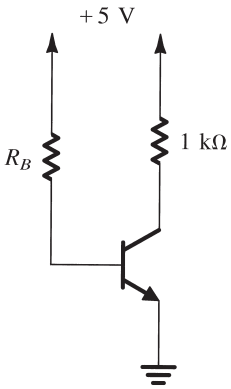


FIGURE P5.65

D5.66 For the circuit in Fig. P5.66 select a value for R_E so that the transistor saturates with a forced β of 10. Assume $V_{EB} = 0.7$ V and $V_{ECsat} = 0.2$ V.

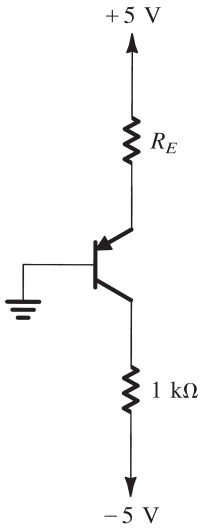


FIGURE P5.66

5.67 For each of the saturated circuits in Fig. P5.67, find i_B, i_C, and i_E. Use $|V_{BE}| = 0.7$ V and $|V_{CEsat}| = 0.2$ V.

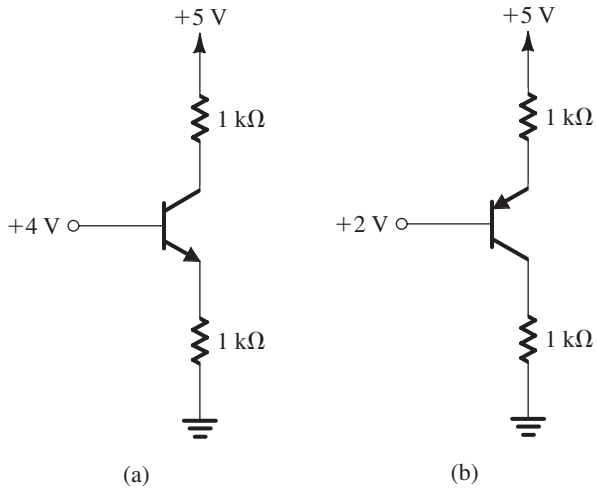


FIGURE P5.67

***5.68** Consider the operation of the circuit shown in Fig. P5.68 as v_B rises slowly from zero. For this transistor, assume $\beta = 50$, v_{BE} at which the transistor conducts is 0.5 V, v_{BE} when fully conducting is 0.7 V, saturation begins at $v_{BC} = 0.4$ V, and the transistor is deeply in saturation at $v_{BC} = 0.6$ V. Sketch and label v_E and v_C versus v_B. For what range of v_B is i_C essentially zero? What are the values of v_E, i_E, i_C, and v_C for $v_B = 1$ V and 3 V. For what value of v_B does saturation begin? What is i_B at this point? For $v_B = 4$ V and 6 V, what are the values of v_E, v_C, i_E, i_C, and i_B. Augment your sketch by adding a plot of i_B.

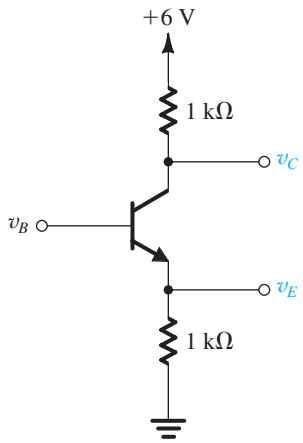


FIGURE P5.68

SECTION 5.4: BJT CIRCUITS AT DC

5.69 The transistor in the circuit of Fig. P5.69 has a very high β. Find V_E and V_C for V_B (a) +2 V, (b) +1 V, and (c) 0 V. Assume $V_{BE} \simeq 0.7$ V.

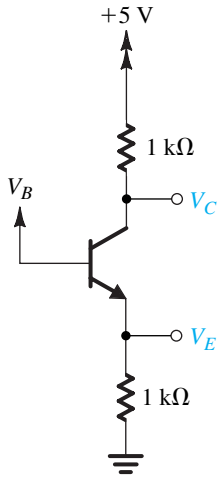


FIGURE P5.69

5.70 The transistor in the circuit of Fig. P5.69 has a very high β. Find the highest value of V_B for which the transistor still operates in the active mode. Also, find the value of V_B for which the transistor operates in saturation with a forced β of 1.

5.71 Consider the operation of the circuit shown in Fig. P5.71 for V_B at –1 V, 0 V, and +1 V. Assume that V_{BE} is 0.7 V for usual currents and that β is very high. What values of V_E and V_C result? At what value of V_B does the emitter current reduce to one-tenth of its value for $v_B = 0$ V. For what value of V_B is the transistor just at the edge of conduction? What values of V_E and V_C correspond? For what value of V_B does the transistor reach saturation (when the base-to-collector junction reaches 0.5 V of forward bias)? What values of V_C and V_E correspond? Find the value of V_B for which the transistor operates in saturation with a forced β of 2.

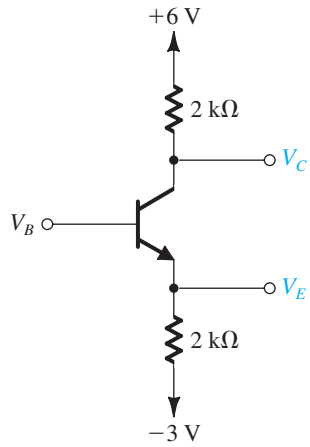


FIGURE P5.71

5.72 For the transistor shown in Fig. P5.72, assume $\alpha \cong 1$ and $v_{BE} = 0.5$ V at the edge of conduction. What are the values of V_E and V_C for $V_B = 0$ V? For what value of V_B does the transistor cut off? Saturate? In each case, what values of V_E and V_C result?

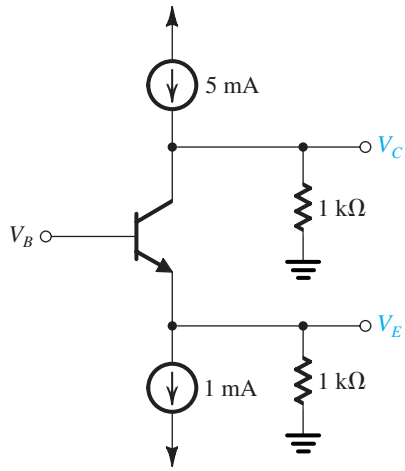


FIGURE P5.72

D5.73 Consider the circuit in Fig. P5.69 with the base voltage V_B obtained using a voltage divider across the 5-V supply. Assuming the transistor β to be very large (i.e., ignoring the base current), design the voltage divider to obtain V_B = 2 V. Design for a 0.2-mA current in the voltage divider. Now, if the BJT $\beta = 100$, analyze the circuit to determine the collector current and the collector voltage.

5.74 A single measurement indicates the emitter voltage of the transistor in the circuit of Fig. P5.74 to be 1.0 V. Under the assumption that $|V_{BE}| = 0.7$ V, what are V_B, I_B, I_E, I_C, V_C, β, and α? (*Note:* Isn't it surprising what a little measurement can lead to?)

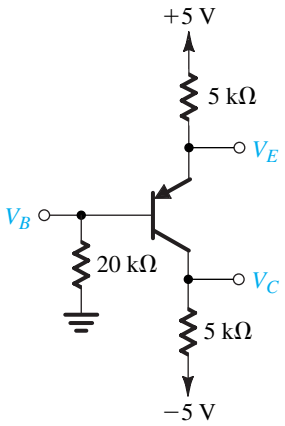


FIGURE P5.74

D5.75 Design a circuit using a *pnp* transistor for which $\alpha \cong 1$ and $V_{EB} \cong 0.7$ V using two resistors connected appropriately to ±9 V so that $I_E = 2$ mA and $V_{BC} = 4.5$ V. What exact values of R_E and R_C would be needed? Now, consult a table of standard 5% resistor values (e.g., that provided in Appendix X) to select suitable practical values. What are the values of I_E and V_{BC} that result?

5.76 In the circuit shown in Fig. P5.76, the transistor has $\beta = 30$. Find the values of V_B, V_E, and V_C. If R_B is raised to 270 kΩ, what voltages result? With $R_B = 270$ kΩ, what value of β would return the voltages to the values first calculated?

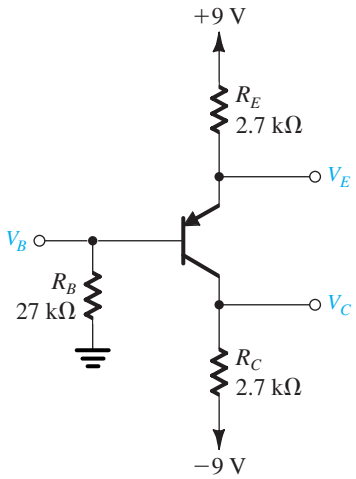


FIGURE P5.76

5.77 In the circuit shown in Fig. P5.76, the transistor has $\beta = 30$. Find the values of V_B, V_E, and V_C, and verify that the transistor is operating in the active mode. What the largest value that R_C can have while the transistor remains in the active mode?

5.78 For the circuit in Fig. P5.78, find V_B, V_E, and V_C for $R_B = 100$ kΩ, 10 kΩ, and 1 kΩ. Let $\beta = 100$.

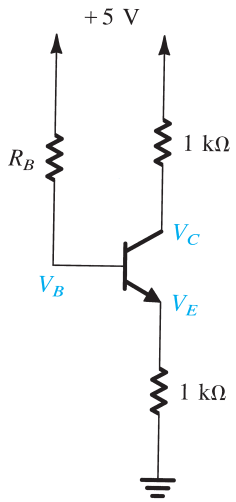


FIGURE P5.78

5.79 For the circuits in Fig. P5.79, find values for the labeled node voltages and branch currents. Assume β to be very high and $|V_{BE}| = 0.7$ V.

***5.80** Repeat the analysis of the circuits in Problem 5.79 using $\beta = 100$. Find all the labeled node voltages and branch currents. Assume $|V_{BE}| = 0.7$ V.

****D5.81** It is required to design the circuit in Fig. P5.81 so that a current of 1 mA is established in the emitter and a voltage of +5 V appears at the collector. The transistor type used has a nominal β of 100. However, the β value can be as low as 50 and as high as 150. Your design should ensure that the specified emitter current is obtained when $\beta = 100$ and that at the extreme values of β the emitter current does not change by more than 10% of its nominal value. Also, design for as large a value for R_B as possible. Give the values of R_B, R_E, and R_C to the nearest kilohm. What is the expected range of collector current and collector voltage corresponding to the full range of β values?

D5.82 The *pnp* transistor in the circuit of Fig. P5.82 has $\beta = 50$. Find the value for R_C to obtain $V_C = +5$ V. What happens if the transistor is replaced with another having $\beta = 100$?

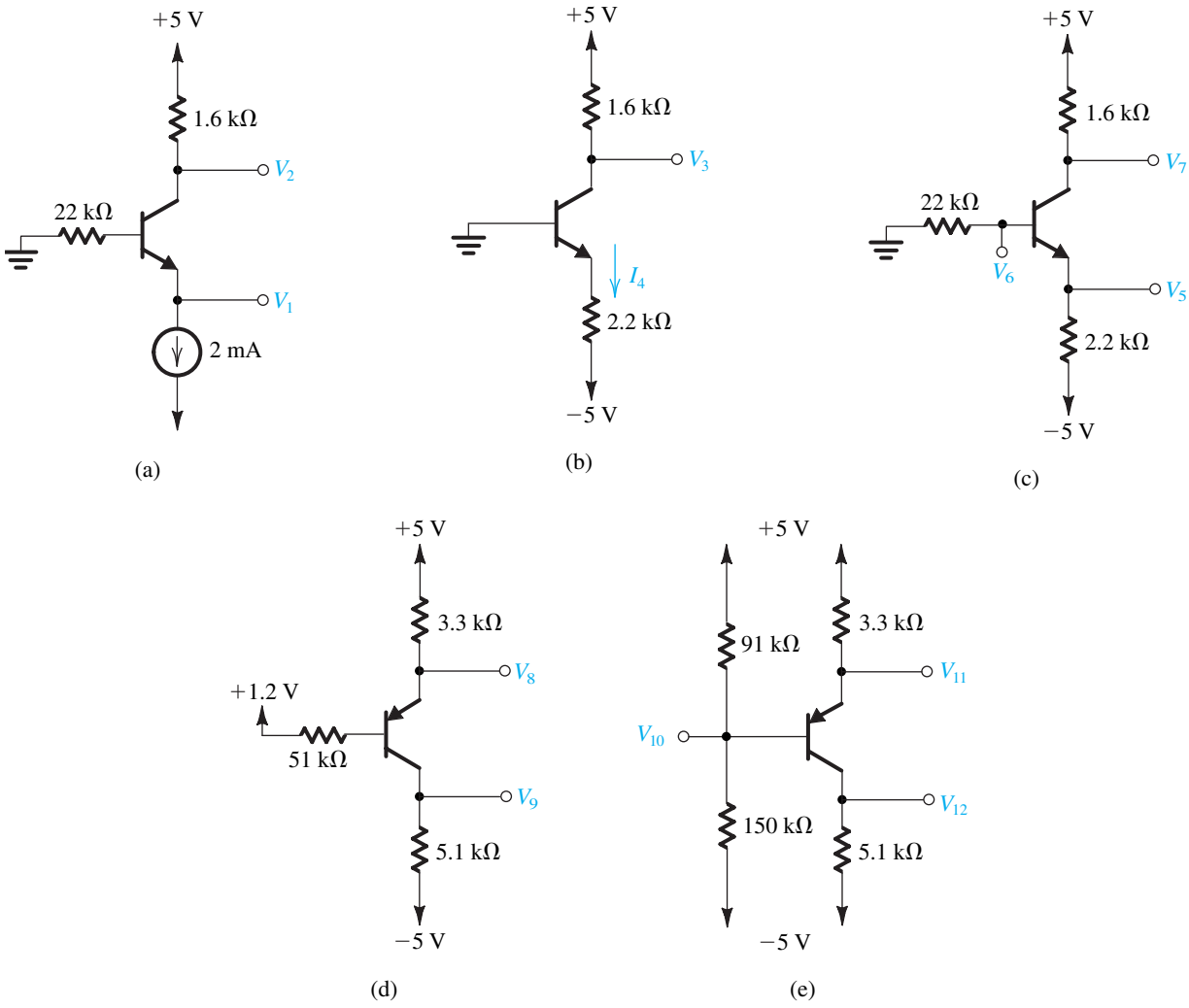


FIGURE P5.79

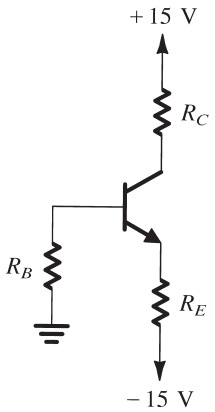


FIGURE P5.81

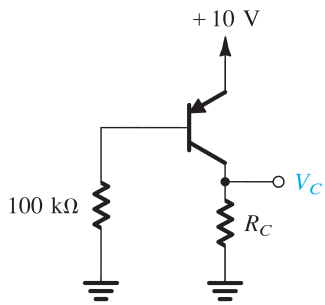


FIGURE P5.82

**5.83 Consider the circuit shown in Fig. P5.83. It resembles that in Fig. 5.41 but includes other features. First, note diodes D_1 and D_2 are included to make design (and analysis) easier and to provide temperature compensation for the emitter–base voltages of Q_1 and Q_2. Second, note resistor R, whose propose is provide negative feedback (more on this later in the book!). Using $|V_{BE}|$ and $V_D = 0.7$ V independent of current and $\beta = \infty$, find the voltages V_{B1}, V_{E1}, V_{C1}, V_{B2}, V_{E2}, and V_{C2}, initially with R open-circuited and then with R connected. Repeat for $\beta = 100$, initially with R open-circuited then connected.

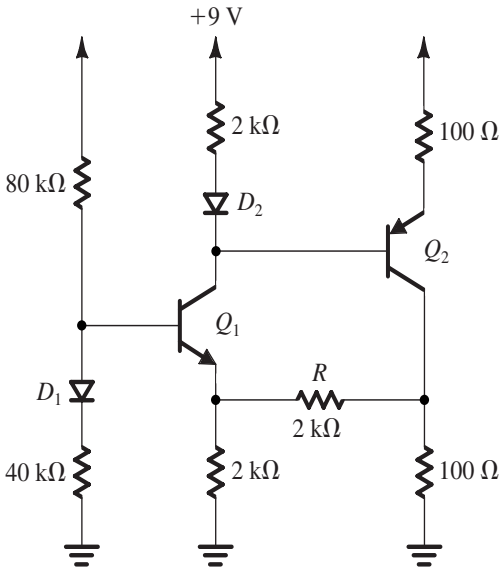


FIGURE P5.83

*5.84 For the circuit shown in Fig. P5.84, find the labeled node voltages for:

(a) $\beta = \infty$
(b) $\beta = 100$

**D5.85 Using $\beta = \infty$, design the circuit shown in Fig. P5.85 so that the bias currents in Q_1, Q_2, and Q_3 are 2 mA, 2 mA, and 4 mA, respectively, and $V_3 = 0$, $V_5 = -4$ V, and $V_7 = 2$ V. For each resistor, select the nearest standard value utilizing the table of standard values for 5% resistors in Appendix H. Now, for $\beta = 100$, find the values of V_3, V_4, V_5, V_6, and V_7.

5.86 For the circuit in Fig. P5.86, find V_B and V_E for $v_I = 0$ V, +3 V, −5 V, and −10 V. The BJTs have $\beta = 100$.

**5.87 Find the approximate values for the collector voltages in the circuits of Fig. P5.87. Also, calculate forced β for each of the transistors. (*Hint:* Assume all transistors are operating in saturation, and verify the assumption.)

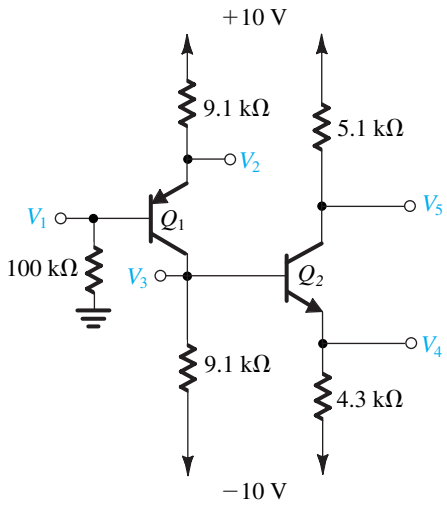


FIGURE P5.84

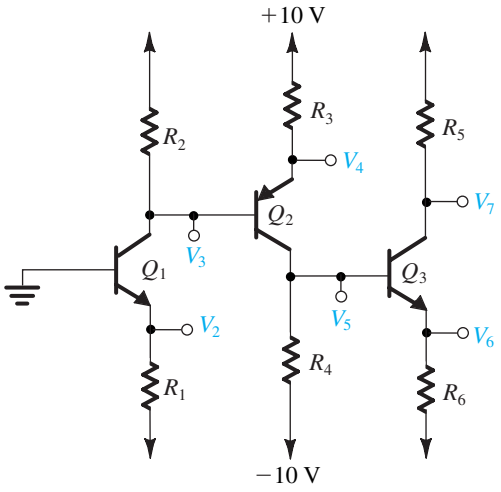


FIGURE P5.85

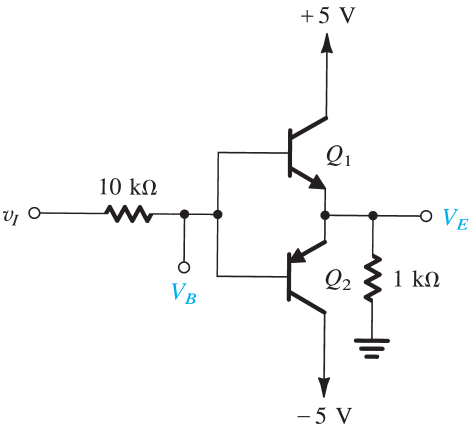


FIGURE P5.86

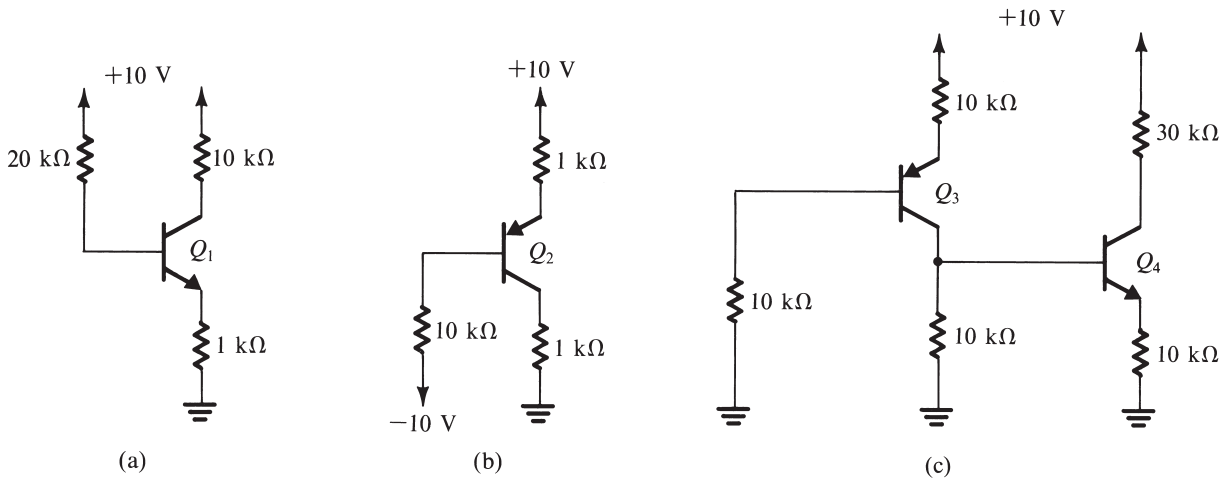


FIGURE P5.87

SECTION 5.5: BIASING IN BJT AMPLIFIER CIRCUITS

D5.88 For the circuit in Fig. 5.43(a), neglect the base current I_B in comparison with the current in the voltage divider. It is required to bias the transistor at $I_C = 1$ mA, which requires selecting R_{B1} and R_{B2} so that $V_{BE} = 0.690$ V. If $V_{CC} = 5$ V, what must the ratio R_{B1}/R_{B2} be? Now, if R_{B1} and R_{B2} are 1% resistors, that is, each can be in the range of 0.99 to 1.01 of its nominal value, what is the range obtained for V_{BE}? What is the corresponding range of I_C? If $R_C = 3$ kΩ, what is the range obtained for V_{CE}? Comment on the efficacy of this biasing arrangement.

D5.89 It is required to bias the transistor in the circuit of Fig. 5.43(b) at $I_C = 1$ mA. The transistor β is specified to be nominally 100, but it can fall in the range of 50 to 150. For $V_{CC} = +5$ V and $R_C = 3$ kΩ, find the required value of R_B to achieve $I_C = 1$ mA for the "nominal" transistor. What is the expected range for I_C and V_{CE}? Comment on the efficacy of this bias design.

D5.90 Consider the single-supply bias network shown in Fig. 5.44(a). Provide a design using a 9-V supply in which the supply voltage is equally split between R_C, V_{CE}, and R_E with a collector current of 3 mA. The transistor β is specified to have a minimum value of 90. Use a voltage-divider current of $I_E/10$, or slightly higher. Since a reasonable design should operate for the best transistors for which β is very high, do your initial design with $\beta = \infty$. Then choose suitable 5% resistors (see Appendix X), making the choice in a way that will result in a V_{BB} that is slightly higher than the ideal value. Specify the values you have chosen for R_E, R_C, R_1, and R_2. Now, find V_B, V_E, V_C, and I_C for your final design using $\beta = 90$.

D5.91 Repeat Problem 5.90, but use a voltage-divider current which is $I_E/2$. Check your design at $\beta = 90$. If you have the data available, find how low β can be while the value of I_C does not fall below that obtained with the design of Problem 5.90 for $\beta = 90$.

****D5.92** It is required to design the bias circuit of Fig. 5.44 for a BJT whose nominal $\beta = 100$.

(a) Find the largest ratio (R_B/R_E) that will guarantee I_E remain within ±5% of its nominal value for β as low as 50 and as high as 150.
(b) If the resistance ratio found in (a) is used, find an expression for the voltage $V_{BB} \equiv V_{CC} R_2/(R_1 + R_2)$ that will result in a voltage drop of $V_{CC}/3$ across R_E.
(c) For $V_{CC} = 10$ V, find the required values of R_1, R_2, and R_E to obtain $I_E = 2$ mA and to satisfy the requirement for stability of I_E in (a).
(d) Find R_C so that $V_{CE} = 3$ V for β equal to its nominal value.

Check your design by evaluating the resulting range of I_E.

***D5.93** Consider the two-supply bias arrangement shown in Fig. 5.45 using ±3-V supplies. It is required to design the circuit so that $I_C = 3$ mA and V_C is placed midway between V_{CC} and V_E.

(a) For $\beta = \infty$, what values of R_E and R_C are required?
(b) If the BJT is specified to have a minimum β of 90, find the largest value for R_B consistent with the need to limit the voltage drop across it to one-tenth the voltage drop across R_E.
(c) What standard 5%-resistor values (see Appendix X) would you use for R_B, R_E, and R_C? In making the selection, use somewhat lower values in order to compensate for the low-β effects.
(d) For the values you selected in (c), find I_C, V_B, V_E, and V_C for $\beta = \infty$ and for $\beta = 90$.

D5.94 Utilizing ±5-V power supplies, it is required to design a version of the circuit in Fig. 5.45 in which the signal will be coupled to the emitter and thus R_B can be set to zero. Find values for R_E and R_C so that a dc emitter current of 1 mA is obtained and so that the gain is maximized while allowing ±1 V of signal swing at the collector. If temperature increases from the nominal value of 25°C to 125°C, estimate the percentage change in collector bias current. In addition to the −2 mV/°C change in V_{BE}, assume that the transistor β changes over this temperature range from 50 to 150.

D5.95 Using a 5-V power supply, design a version of the circuit of Fig. 5.46 to provide a dc emitter current of 0.5 mA and to allow a ±1-V signal swing at the collector. The BJT has a nominal $\beta = 100$. Use standard 5%-resistor values (see Appendix H). If the actual BJT used has $\beta = 50$, what emitter current is obtained? Also, what is the allowable signal swing at the collector? Repeat for $\beta = 150$.

D5.96 (a) Using a 3-V power supply, design the feedback bias circuit of Fig. 5.46 to provide $I_C = 3$ mA and $V_C = V_{CC}/2$ for $\beta = 90$.
(b) Select standard 5% resistor values, and reevaluate V_C and I_C for $\beta = 90$.
(c) Find V_C and I_C for $\beta = \infty$.
(d) To improve the situation that obtains when high-β transistors are used, we have to arrange for an additional current to flow through R_B. This can be achieved by connecting a resistor between base and emitter, as shown in Fig. P5.96. Design this circuit for $\beta = 90$. Use a current through R_{B2} equal to the base current. Now, what values of V_C and I_C result with $\beta = \infty$?

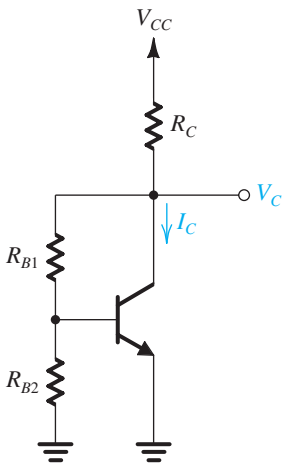


FIGURE P5.96

D5.97 A circuit that can provide a very large voltage gain for a high-resistance load is shown in Fig. P5.97. Find the values of I and R_B to bias the BJT at $I_C = 3$ mA and $V_C = 1.5$ V. Let $\beta = 90$.

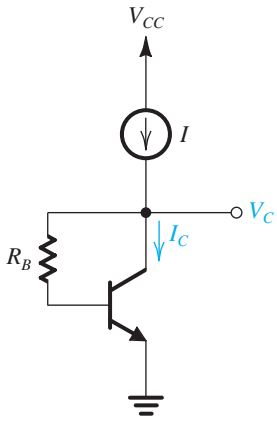


FIGURE P5.97

5.98 The circuit in Fig. P5.98 provides a constant current I_O as long as the circuit to which the collector is connected maintains the BJT in the active mode. Show that

$$I_O = \alpha \frac{V_{CC}[R_2/(R_1 + R_2)] - V_{BE}}{R_E + (R_1 // R_2)/(\beta + 1)}$$

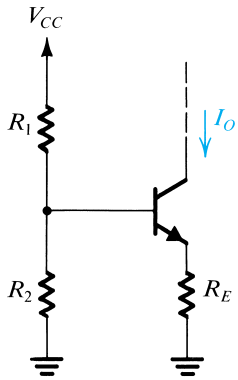


FIGURE P5.98

D5.99 The current-bias circuit shown in Fig. P5.99 provides bias current to Q_1 that is independent of R_B and nearly independent of the value of β_1 (as long as Q_2 operates in the active mode). Prepare a design meeting the following specifications: Use ±5-V supplies; $I_{C1} = 0.1$ mA, $V_{BE} = 2$ V for $\beta = \infty$; the voltage across R_E decreases by at most 5% for $\beta = 50$; $V_{CE1} = 1.5$ V for $\beta = \infty$ and 2.5 V for $\beta = 50$. Use standard 5%-resistor values (see Appendix H). What values for R_1, R_2, R_E, R_B, and R_C do you choose? What values of I_{C1} and V_{CE1} result for $\beta = 50$, 100, and 200?

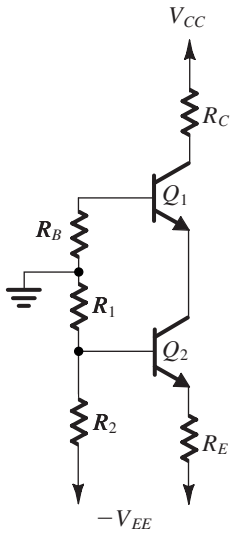


FIGURE P5.99

***D5.100** For the circuit in Fig. P5.100, assuming all transistors to be identical with β infinite, derive an expression for the output current I_O, and show that by selecting

$$R_1 = R_2$$

and keeping the current in each junction the same, the current I_O will be

$$I_O = \frac{\alpha V_{CC}}{2R_E}$$

which is independent of V_{BE}. What must the relationship of R_E to R_1 and R_2 be? For $V_{CC} = 10$ V and assuming $\alpha \simeq 1$ and $V_{BE} = 0.7$ V, design the circuit to obtain an output current of 0.5 mA. What is the lowest voltage that can be applied to the collector of Q_3?

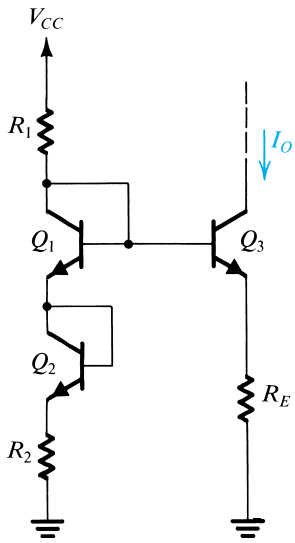


FIGURE P5.100

D5.101 For the circuit in Fig. P5.101 find the value of R that will result in $I_O \simeq 2$ mA. What is the largest voltage that can be applied to the collector? Assume $|V_{BE}| = 0.7$ V.

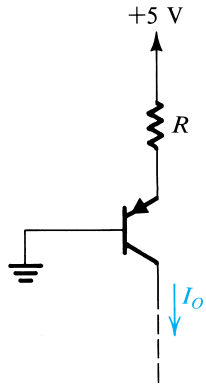


FIGURE P5.101

SECTION 5.6: SMALL-SIGNAL OPERATION AND MODELS

5.102 Consider a transistor biased to operate in the active mode at a dc collector current I_C. Calculate the collector signal current as a fraction of I_C (i.e., i_c/I_C) for input signals v_{be} of +1 mV, −1 mV, +2 mV, −2 mV, +5 mV, −5 mV, +8 mV, −8 mV, +10 mV, −10 mV, +12 mV, and −12 mV. In each case do the calculation two ways:

(a) using the exponential characteristic, and
(b) using the small-signal approximation.

Present your results in the form of a table that includes a column for the error introduced by the small-signal approximation. Comment on the range of validity of the small-signal approximation.

5.103 An *npn* BJT with grounded emitter is operated with $V_{BE} = 0.700$ V, at which the collector current is 1 mA. A 10-kΩ resistor connects the collector to a +15-V supply. What is the resulting collector voltage V_C? Now, if a signal applied to the base raises v_{BE} to 705 mV, find the resulting total collector current i_C and total collector voltage v_C using the exponential i_C–v_{BE} relationship. For this situation, what are v_{be} and v_c? Calculate the voltage gain v_c/v_{be}. Compare with the value obtained using the small-signal approximation, that is, $-g_m R_C$.

5.104 A transistor with $\beta = 120$ is biased to operate at a dc collector current of 1.2 mA. Find the values of g_m, r_π, and r_e. Repeat for a bias current of 120 μA.

5.105 A *pnp* BJT is biased to operate at $I_C = 2.0$ mA. What is the associated value of g_m? If $\beta = 50$, what is the value of

the small-signal resistance seen looking into the emitter (r_e)? Into the base (r_π)? If the collector is connected to a 5-kΩ load, with a signal of 5-mV peak applied between base and emitter, what output signal voltage results?

D5.106 A designer wishes to create a BJT amplifier with a g_m of 50 mA/V and a base input resistance of 2000 Ω or more. What emitter-bias current should he choose? What is the minimum β he can tolerate for the transistor used?

5.107 A transistor operating with nominal g_m of 60 mA/V has a β that ranges from 50 to 200. Also, the bias circuit, being less than ideal, allows a ±20% variation in I_C. What are the extreme values found of the resistance looking into the base?

5.108 In the circuit of Fig. 5.48, V_{BE} is adjusted so that $V_C = 2$ V. If $V_{CC} = 5$ V, $R_C = 3$ kΩ, and a signal $v_{be} = 0.005 \sin \omega t$ volts is applied, find expressions for the total instantaneous quantities $i_C(t)$, $v_C(t)$, and $i_B(t)$. The transistor has $\beta = 100$. What is the voltage gain?

***D5.109** We wish to design the amplifier circuit of Fig. 5.48 under the constraint that V_{CC} is fixed. Let the input signal $v_{be} = \hat{V}_{be} \sin \omega_t$, where $\hat{V}_{be}$ is the maximum value for acceptable linearity. Show for the design that results in the largest signal at the collector without the BJT leaving the active region, that

$$R_C I_C = (V_{CC} - 0.3 - \hat{V}_{be}) \Big/ \left(1 + \frac{\hat{V}_{be}}{V_T}\right)$$

and find an expression for the voltage gain obtained. For $V_{CC} = 5$ V and $\hat{V}_{be} = 5$ mV, find the dc voltage at the collector, the amplitude of the output voltage signal, and the voltage gain.

5.110 The following table summarizes some of the basic attributes of a number of BJTs of different types, operating as amplifier under various conditions. Provide the missing entries.

Transistor	a	b	c	d	e	f	g
α	1.000					0.90	
β		100		∞			
I_C (mA)	1.00		1.00				
I_E (mA)		1.00				5	
I_B (mA)			0.020				1.10
g_m (mA/V)							700
r_e (Ω)				25	100		
r_π (Ω)					10.1 kΩ		

(*Note:* Isn't it remarkable how much two parameters can reveal?)

5.111 A BJT is biased to operate in the active mode at a dc collector current of 1.0 mA. It has a β of 120. Give the four small-signal models (Figs. 5.51 and 5.52) of the BJT complete with the values of their parameters.

5.112 The transistor amplifier in Fig. P5.112 is biased with a current source I and has a very high β. Find the dc voltage at the collector, V_C. Also, find the value of g_m. Replace the transistor with its simplified hybrid-π model of Fig. 5.51(a) (note that the dc current source I should be replaced with an open circuit). Hence find the voltage gain v_c/v_i.

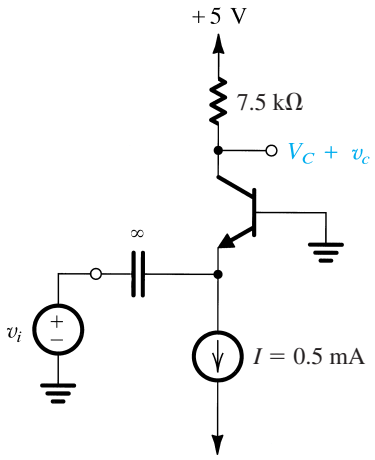


FIGURE P5.112

5.113 For the conceptual circuit shown in Fig. 5.50, $R_C = 2$ kΩ, $g_m = 50$ mA/V, and $\beta = 100$. If a peak-to-peak output voltage of 1 V is measured at the collector, what ac input voltage and current must be associated with the base?

5.114 A biased BJT operates as an amplifier between a signal source, with a source resistance of 10 kΩ, connected to the base and a 10-kΩ load connected as a collector resistance R_C. In the corresponding model, g_m is 40 mA/V and r_π is

2.5 kΩ. Draw the complete amplifier model using the hybrid-π BJT equivalent circuit. Calculate the overall voltage gain (v_c/v_s). What is the value of BJT β implied by the values of the model parameters? To what value must β be increased to double the overall voltage gain?

5.115 For the circuit shown in Fig. P5.115, draw a complete small-signal equivalent circuit utilizing an appropriate T model for the BJT ($\alpha = 0.99$). Your circuit should show the values of all components, including the model parameters. What is the input resistance R_{in}? Calculate the overall voltage gain (v_o/v_s).

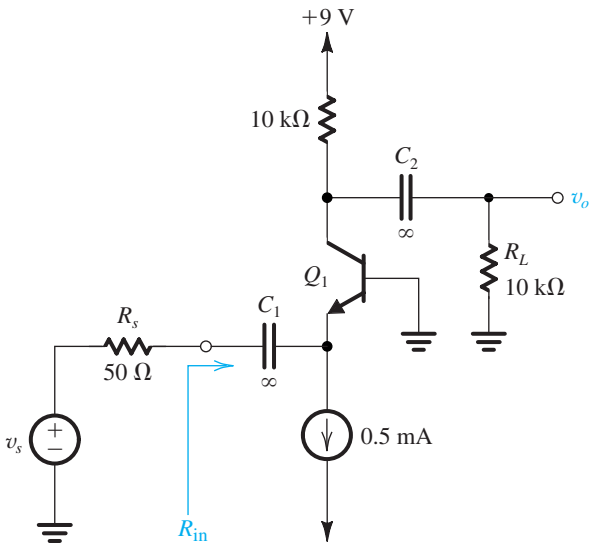


FIGURE P5.115

5.116 In the circuit shown in Fig. P5.116, the transistor has a β of 200. What is the dc voltage at the collector? Find the input resistances R_{i1} and R_{i2} and the overall voltage gain (v_o/v_s). For output signal of ±0.4 V, what values of v_s and v_b are required?

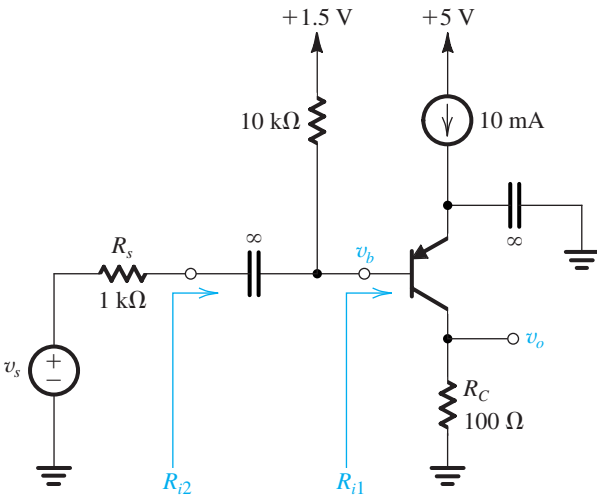


FIGURE P5.116

5.117 Consider the augmented hybrid-π model shown in Fig. 5.58. Disregarding how biasing is to be done, what is the largest possible voltage gain available for a signal source connected directly to the base and a very-high-resistance load? Calculate the value of the maximum possible gain for $V_A = 25$ V and $V_A = 250$ V.

5.118 Reconsider the amplifier shown in Fig. 5.53 and analyzed in Example 5.14 under the condition that β is not well controlled. For what value of β does the circuit begin to saturate? We can conclude that large β is dangerous in this circuit. Now, consider the effect of reduced β, say, to $\beta = 25$. What values of r_e, g_m, and r_π result? What is the overall voltage gain? (*Note:* You can see that this circuit, using base-current control of bias, is very β-sensitive and usually *not recommended*.)

5.119 Reconsider the circuit shown in Fig. 5.55 under the condition that the signal source has an internal resistance of 100 Ω. What does the overall voltage gain become? What is the largest input signal voltage that can be used without output-signal clipping?

D5.120 Redesign the circuit of Fig. 5.55 by raising the resistor values by a factor n to increase the resistance seen by the input v_i to 75 Ω. What value of voltage gain results? Grounded-base circuits of this kind are used in systems such as cable TV, in which, for highest-quality signaling, load resistances need to be "matched" to the equivalent resistances of the interconnecting cables.

5.121 Using the BJT equivalent circuit model of Fig. 5.52(a), sketch the equivalent circuit of a transistor amplifier for which a resistance R_e is connected between the emitter and ground, the collector is grounded, and an input signal source v_b is connected between the base and ground. (It is assumed that the transistor is properly biased to operate in the active region.) Show that:

(a) the voltage gain between base and emitter, that is, v_e/v_b, is given by

$$\frac{v_e}{v_b} = \frac{R_e}{R_e + r_e}$$

(b) the input resistance,

$$R_{in} \equiv \frac{v_b}{i_b} = (\beta + 1)(R_e + r_e)$$

Find the numerical values for (v_e/v_b) and R_{in} for the case R_e = 1 kΩ, $\beta = 100$, and the emitter bias current $I_E = 1$ mA.

5.122 When the collector of a transistor is connected to its base, the transistor still operates (internally) in the active region because the collector–base junction is still in effect reverse biased. Use the simplified hybrid-π model to find the

incremental (small-signal) resistance of the resulting two-terminal device (known as a diode-connected transistor.)

**D5.123 Design an amplifier using the configuration of Fig. 5.55(a). The power supplies available are ±10 V. The input signal source has a resistance of 100 Ω, and it is required that the amplifier input resistance match this value. (Note that $R_{in} = r_e \,//\, R_E \simeq r_e$.) The amplifier is to have the greatest possible voltage gain and the largest possible output signal but retain small-signal linear operation (i.e., the signal component across the base–emitter junction should be limited to no more than 10 mV). Find values for R_E and R_C. What is the value of voltage gain realized?

*5.124 The transistor in the circuit shown in Fig. P5.124 is biased to operate in the active mode. Assuming that β is very large, find the collector bias current I_C. Replace the transistor with the small-signal equivalent circuit model of Fig. 5.52(b) (remember to replace the dc power supply with a short circuit). Analyze the resulting amplifier equivalent circuit to show that

$$\frac{v_{o1}}{v_i} = \frac{R_E}{R_E + r_e}$$

$$\frac{v_{o2}}{v_i} = \frac{-\alpha R_C}{R_E + r_e}$$

Find the values of these voltage gains ($\alpha \simeq 1$). Now, if the terminal labeled v_{o1} is connected to ground, what does the voltage gain v_{o2}/v_i become?

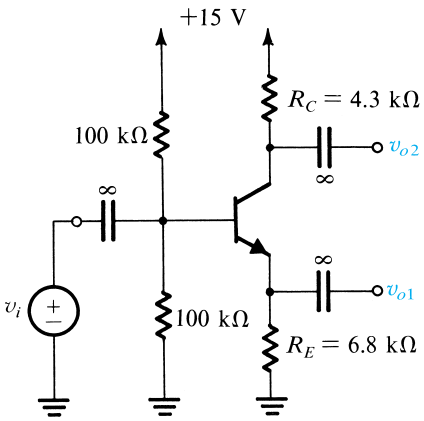


FIGURE P5.124

SECTION 5.7: SINGLE-STAGE BJT AMPLIFIERS

5.125 An amplifier is measured to have $R_i = 10$ kΩ, $A_{vo} = 100$ V/V, and $R_o = 100$ Ω. Also, when a load resistance R_L of 1 kΩ is connected between the output terminals, the input resistance is found to decrease to 8 kΩ. If the amplifier is fed with a signal source having an internal resistance of 2 kΩ, find G_m, A_v, G_{vo}, G_v, R_{out}, and A_i.

5.126 Figure P5.126 shows an alternative equivalent circuit for representing *any* linear two-port network including voltage amplifiers. This equivalent circuit is based on the *g*-parameter two-port representation (see Appendix X).

(a) Using the values of R_i, A_{vo}, and R_o given in Example 5.17 together with the measured value of R_{in} of 400 kΩ obtained when a load R_L of 10 kΩ is connected to the output, determine the value of the feedback factor f.
(b) Now, use the equivalent circuit of Fig. P5.126 to determine the value of R_{out} obtained when the amplifier is fed with a signal generator having $R_{sig} = 100$ kΩ. Check your result against that found in Example 5.17.

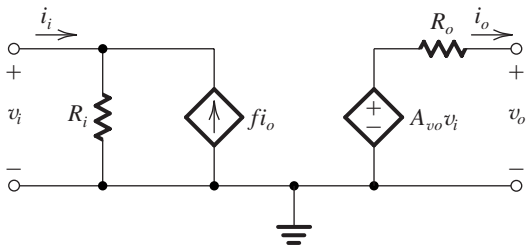


FIGURE P5.126

5.127 Refer to Table 5.5. By equating the expression for G_v obtained from Equivalent Circuit A to that obtained from Equivalent Circuit B with $G_{vo} = R_i/(R_i + R_{sig})A_{vo}$, show that

$$\frac{R_{in}}{R_i}\frac{R_{sig} + R_i}{R_{sig} + R_{in}} = \frac{R_L + R_o}{R_L + R_{out}}$$

Now, use this expression to:

(a) Show that for $R_L = \infty$, $R_{in} = R_i$.
(b) Show that for $R_{sig} = 0$, $R_{out} = R_o$.
(c) Find R_{out} when $R_{sig} = \infty$ (i.e., the amplifier input is open-circuited), and evaluate its value for the amplifier specified in Example 5.17.

5.128 A common-emitter amplifier of the type shown in Fig. 5.60(a) is biased to operate at $I_C = 0.2$ mA and has a collector resistance $R_C = 24$ kΩ. The transistor has $\beta = 100$ and a large V_A. The signal source is directly coupled to the base, and C_{C1} and R_B are eliminated. Find R_{in}, the voltage gain A_{vo}, and R_o. Use these results to determine the overall voltage gain when a 10-kΩ load resistor is connected to the collector and the source resistance $R_{sig} = 10$ kΩ.

5.129 Repeat Problem 5.128 with a 125-Ω resistance included in the signal path in the emitter. Furthermore, contrast the maximum amplitude of the input sine wave that can be applied with and without R_e assuming that to limit distortion the signal between base and emitter is not to exceed 5 mV.

5.130 For the common-emitter amplifier shown in Fig. P5.130, let $V_{CC} = 9$ V, $R_1 = 27$ kΩ, $R_2 = 15$ kΩ, $R_E = 1.2$ kΩ, and $R_C = 2.2$ kΩ. The transistor has $\beta = 100$ and $V_A = 100$ V.

Calculate the dc bias current I_E. If the amplifier operates between a source for which R_{sig} = 10 kΩ and a load of 2 kΩ, replace the transistor with its hybrid-π model, and find the values of R_{in}, the voltage gain v_o/v_{sig}, and the current gain i_o/i_i.

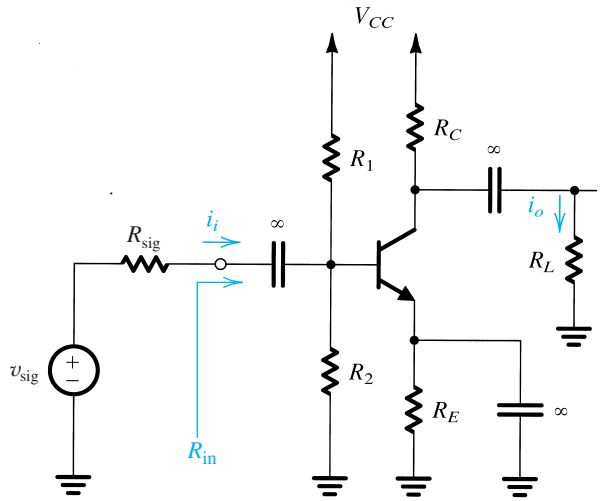


FIGURE P5.130

D5.131 Using the topology of Fig. P5.130, design an amplifier to operate between a 10-kΩ source and a 2-kΩ load with a gain v_o/v_{sig} of −8 V/V. The power supply available is 9 V. Use an emitter current of approximately 2 mA and a current of about one-tenth that in the voltage divider that feeds the base, with the dc voltage at the base about one-third of the supply. The transistor available has β = 100 and V_A = 100 V. Use standard 5% resistor (see Appendix H).

5.132 A designer, having examined the situation described in Problem 5.130 and estimating the available gain to be approximately −8 V/V, wishes to explore the possibility of improvement by reducing the loading of the source by the amplifier input. As an experiment, the designer varies the resistance levels by a factor of approximately 3: R_1 to 82 kΩ, R_2 to 47 kΩ, R_E to 3.6 kΩ, and R_C to 6.8 kΩ (standard values of 5%-tolerance resistors). With V_{CC} = 9 V, R_s = 10 kΩ, R_L = 2 kΩ, β = 100, and V_A = 100 V, what does the gain become? Comment.

D5.133 Consider the CE amplifier circuit of Fig. 5.60(a). It is required to design the circuit (i.e., find values for I, R_B, and R_C) to meet the following specifications:

(a) $R_i \cong 5$ kΩ.
(b) the dc voltage drop across R_B is approximately 0.5 V.
(c) the open-circuit voltage gain from base to collector is the maximum possible, consistent with the requirement that the collector voltage never falls by more than approximately 0.5 V below the base voltage with the signal between base and emitter being as high as 5 mV.

Assume that v_s is a sinusoidal source, the available supply V_{CC} = 5 V, and the transistor has β = 100 and a very large Early voltage. Use standard 5%-resistance values, and specify the value of I to one significant digit. What base-to-collector open-circuit voltage gain does your design provide? If R_s = R_L = 10 kΩ, what is the overall voltage gain?

D5.134 In the circuit of Fig. P5.134, v_s is a small sine-wave signal with zero average. The transistor β is 100.

(a) Find the value of R_E to establish a dc emitter current of about 0.5 mA.
(b) Find R_C to establish a dc collector voltage of about +5 V.
(c) For R_L = 10 kΩ and the transistor r_o = 200 kΩ, draw the small-signal equivalent circuit of the amplifier and determine its overall voltage gain.

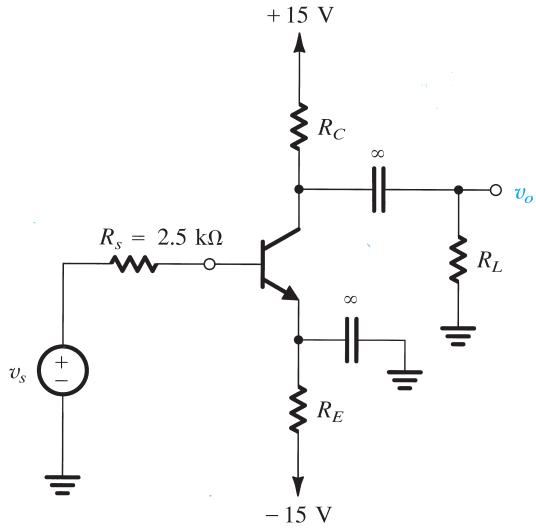


FIGURE P5.134

***5.135** The amplifier of Fig. P5.135 consists of two identical common-emitter amplifiers connected in cascade. Observe that the input resistance of the second stage, R_{in2}, constitutes the load resistance of the first stage.

(a) For V_{CC} = 15 V, R_1 = 100 kΩ, R_2 = 47 kΩ, R_E = 3.9 kΩ, R_C = 6.8 kΩ, and β = 100, determine the dc collector current and collector voltage of each transistor.
(b) Draw the small-signal equivalent circuit of the entire amplifier and give the values of all its components. Neglect r_{o1} and r_{o2}.
(c) Find R_{in1} and v_{b1}/v_s for R_s = 5 kΩ.
(d) Find R_{in2} and v_{b2}/v_{b1}.
(e) For R_L = 2 kΩ, find v_o/v_{b2}.
(f) Find the overall voltage gain v_o/v_s.

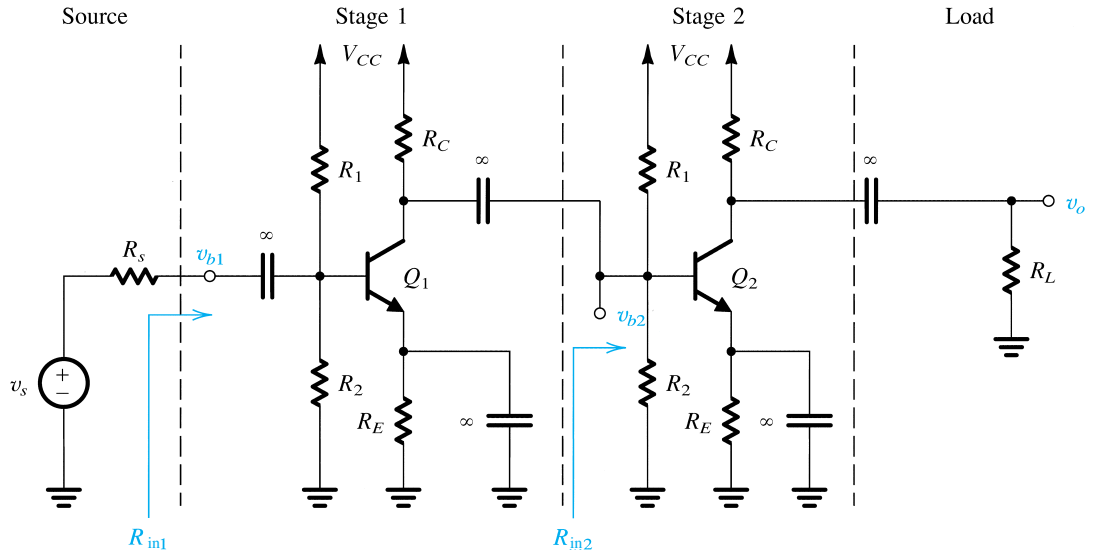


FIGURE P5.135

5.136 In the circuit of Fig. P5.136, v_s is a small sine-wave signal. Find R_{in} and the gain v_o/v_s. Assume $\beta = 100$. If the amplitude of the signal v_{be} is to be limited to 5 mV, what is the largest signal at the input? What is the corresponding signal at the output?

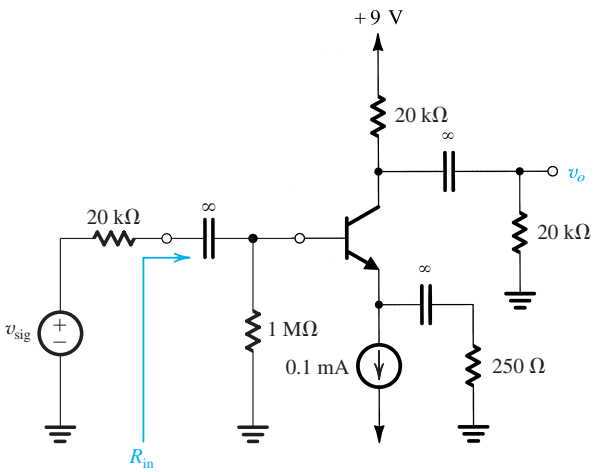


FIGURE P5.136

***5.137** The BJT in the circuit of Fig. P5.137 has $\beta = 100$.

(a) Find the dc collector current and the dc voltage at the collector.

(b) Replacing the transistor by its T model, draw the small-signal equivalent circuit of the amplifier. Analyze the resulting circuit to determine the voltage gain v_o/v_i.

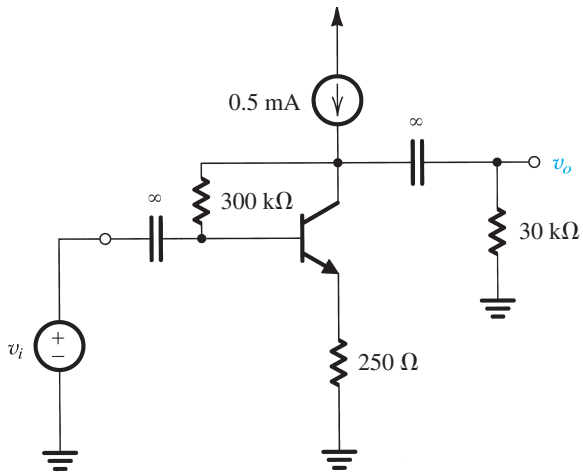


FIGURE P5.137

***5.138** Refer to the voltage-gain expression (in terms of the transistor β) given in Eq. (5.136) for the CE amplifier with a resistance R_e in the emitter. Let the BJT be biased at an emitter current of 0.5 mA. The source resistance R_s is 10 kΩ. The BJT β is specified to lie in the range of 50 to 150 with a nominal value of 100.

(a) What is the ratio of maximum to minimum voltage gain obtained without R_e?

(b) What value of R_e should be used to limit the ratio of maximum to minimum gain to 1.2?

(c) If the R_e found in (b) is used, by what factor is the gain reduced (compared to the case without R_e) for a BJT with a nominal β?

5.139 Consider the CB amplifier of Fig. 5.62 with $R_L = 10\ \text{k}\Omega$, $R_C = 10\ \text{k}\Omega$, $V_{CC} = 10$ V, and $R_s = 100\ \Omega$. To what value must I be set in order that the input resistance at E is equal to that of the source (i.e., 100 Ω)? What is the resulting voltage gain from the source to the load? Assume $\alpha \simeq 1$.

****D5.140** Consider the CB amplifier of Fig. 5.62(a) with the collector voltage signal coupled to a 1-kΩ load resistance through a large capacitor. Let the power supplies be ±5 V. The source has a resistance of 50 Ω. Design the circuit so that the amplifier input resistance is matched to that of the source and the output signal swing is as large as possible with relatively low distortion (v_{be} limited to 10 mV). Find I and R_C and calculate the overall voltage gain obtained and the output signal swing. Assume $\alpha \simeq 1$.

5.141 For the circuit in Fig. P5.141, find the input resistance R_i and the voltage gain v_o/v_s. Assume that the source provides a small signal v_s and that $\beta = 100$.

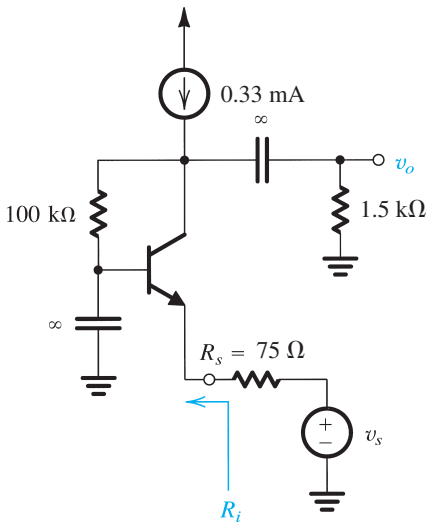


FIGURE P5.141

5.142 Consider the emitter follower of Fig. 5.63(a) for the case $I = 1$ mA, $\beta = 100$, $V_A = 100$ V, $R_B = 100\ \text{k}\Omega$, $R_s = 20\ \text{k}\Omega$, and $R_L = 1\ \text{k}\Omega$.

(a) Find R_{in}, v_b/v_s, and v_o/v_s.
(b) If v_s is a sine-wave signal, to what value should its amplitude be limited to in order that the transistor remains conducting at all times? For this amplitude, what is the corresponding amplitude across the base–emitter junction?
(c) If the signal amplitude across the base–emitter junction is to be limited to 10 mV, what is the corresponding amplitude of v_s and of v_o?
(d) Find the open-circuit voltage gain v_o/v_s and the output resistance. Use these values to determine the value of v_o/v_s obtained with $R_L = 500\ \Omega$.

5.143 For the emitter-follower circuit shown in Fig. P5.143, the BJT used is specified to have β values in the range of 40 to 200 (a distressing situation for the circuit designer). For the two extreme values of β ($\beta = 40$ and $\beta = 200$), find:

(a) I_E, V_E, and V_B.
(b) the input resistance R_i.
(c) the voltage gain v_o/v_s.

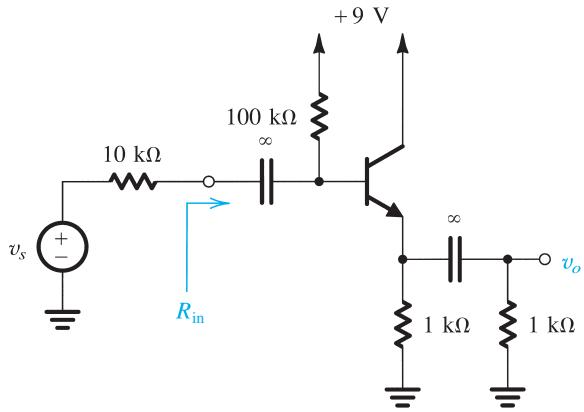


FIGURE P5.143

5.144 In the emitter follower in Fig. P5.144, the signal source is directly coupled to the transistor base. If the dc component of v_s is zero, find the dc emitter current. Assume $\beta = 100$. Neglecting r_o, find R_{in}, the voltage gain v_o/v_s, the current gain i_o/i_i, and the output resistance R_{out}.

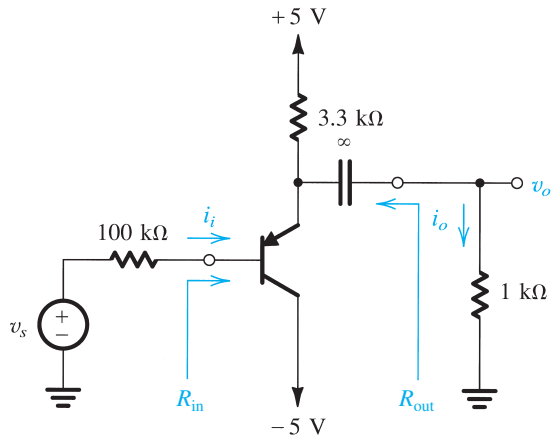


FIGURE P5.144

5.145 In the emitter follower of Fig. 5.63(a), the signal source is directly coupled to the base. Thus, C_{C1} and R_B are eliminated. The source has $R_s = 10\ \text{k}\Omega$ and a dc component of zero. The transistor has $\beta = 100$ and $V_A = 125$ V. The bias current $I = 2.5$ mA, and $V_{CC} = 3$ V. What is the output resistance

of the follower? Find the gain v_o/v_s with no load and with a load of 1 kΩ. With the 1-kΩ load connected, find the largest possible negative output signal. What is the largest possible positive output signal if operation is satisfactory up to the point that the base–collector junction is forward biased by 0.4 V?

5.146 The emitter follower of Fig. 5.63(a), when driven from a 10-kΩ source, was found to have an open-circuit voltage gain of 0.99 and an output resistance of 200 Ω. The output resistance increased to 300 Ω when the source resistance was increased to 20 kΩ. Find the overall voltage gain when the follower is driven by a 30-kΩ source and loaded by a 1-kΩ resistor. Assume r_o is very large.

****5.147** For the circuit in Fig. P5.147, called a **bootstrapped follower:**

(a) Find the dc emitter current and g_m, r_e, and r_π. Use $\beta = 100$.
(b) Replace the BJT with its T model (neglecting r_o), and analyze the circuit to determine the input resistance R_{in} and the voltage gain v_o/v_s.
(c) Repeat (b) for the case when capacitor C_B is open-circuited. Compare the results with those obtained in (b) to find the advantages of bootstrapping.

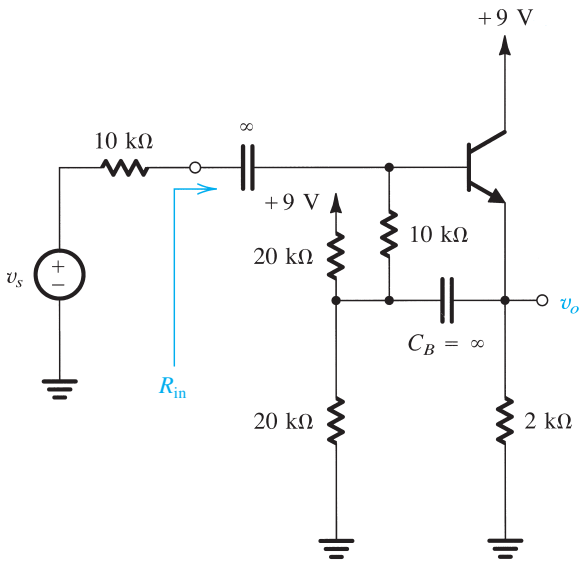


FIGURE P5.147

****5.148** For the follower circuit in Fig. P5.148 let transistor Q_1 have $\beta = 50$ and transistor Q_2 have $\beta = 100$, and neglect the effect of r_o. Use $V_{BE} = 0.7$ V.

(a) Find the dc emitter current of Q_1 and Q_2. Also, find the dc voltages V_{B1} and V_{B2}.
(b) If a load resistance $R_L = 1$ kΩ is connected to the output terminal, find the voltage gain from the base to the emitter of Q_2, v_o/v_{b2}, and find the input resistance R_{ib2} looking into the base of Q_2. (*Hint:* Consider Q_2 as an emitter follower fed by a voltage v_{b2} at its base.)
(c) Replacing Q_2 with its input resistance R_{ib2} found in (b), analyze the circuit of emitter follower Q_1 to determine its input resistance R_i, and the gain from its base to its emitter, v_{e1}/v_{b1}.
(d) If the circuit is fed with a source having a 100-kΩ resistance, find the transmission to the base of Q_1, v_{b1}/v_s.
(e) Find the overall voltage gain v_o/v_s.

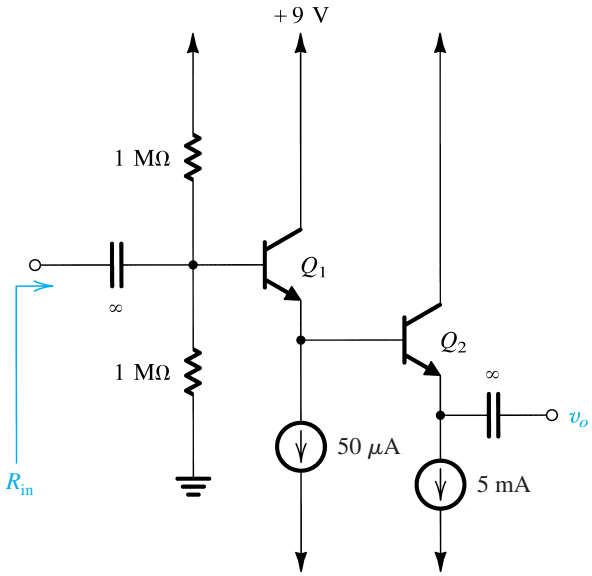


FIGURE P5.148

SECTION 5.8: THE BJT INTERNAL CAPACITANCES AND HIGH-FREQUENCY MODEL

5.149 An *npn* transistor is operated at $I_C = 0.5$ mA and $V_{CB} = 2$ V. It has $\beta_0 = 100$, $V_A = 50$ V, $\tau_F = 30$ ps, $C_{je0} = 20$ fF, $C_{\mu 0} = 30$ fF, $V_{0c} = 0.75$ V, $m_{CBJ} = 0.5$, and $r_x = 100$ Ω. Sketch the complete hybrid-π model, and specify the values of all its components. Also, find f_T.

5.150 Measurement of h_{fe} of an *npn* transistor at 500 MHz shows that $|h_{fe}| = 2.5$ at $I_C = 0.2$ mA and 11.6 at $I_C = 1.0$ mA. Furthermore, C_μ was measured and found to be 0.05 pF. Find f_T at each of the two collector currents used. What must τ_F and C_{je} be?

5.151 A particular BJT operating at $I_C = 2$ mA has $C_\mu = 1$ pF, $C_\pi = 10$ pF, and $\beta = 150$. What are f_T and f_β for this situation?

5.152 For the transistor described in Problem 5.151, C_π includes a relatively constant depletion-layer capacitance of 2 pF.

Transistor	I_E (mA)	r_e (Ω)	g_m (mA/V)	r_π (kΩ)	β_0	f_T (MHz)	C_μ (pF)	C_π (pF)	f_β (MHz)
(a)	1				100	400	2		
(b)		25					2	10.7	4
(c)				2.525		400		13.8	4
(d)	10				100	400	2		
(e)	0.1				100	100	2		
(f)	1				10	400	2		
(g)						800	1	9	80

If the device is operated at $I_C = 0.2$ mA, what does its f_T become?

5.153 A particular small-geometry BJT has f_T of 5 GHz and $C_\mu = 0.1$ pF when operated at $I_C = 0.5$ mA. What is C_π in this situation? Also, find g_m, and for $\beta = 150$, find r_π and f_β.

5.154 For a BJT whose unity-gain bandwidth is 1 GHz and $\beta_0 = 200$, at what frequency does the magnitude of h_{fe} become 20? What is f_β?

***5.155** For a sufficiently high frequency, measurement of the complex input impedance of a BJT having (ac) grounded emitter and collector yields a real part approximating r_x. For what frequency, defined in terms of ω_β, is such an estimate of r_x good to within 10% under the condition that $r_x \leq r_\pi/10$? Neglect C_μ.

***5.156** Complete the table entries above for transistors (a) through (g), under the conditions indicated. Neglect r_x.

SECTION 5.9: FREQUENCY RESPONSE OF THE COMMON-EMITTER AMPLIFIER

5.157 A designer wishes to investigate the effect of changing the bias current I on the midband gain and high-frequency response of the CE amplifier considered in Example 5.18. Let I be doubled to 2 mA, and assume that β_0 and f_T remain unchanged at 100 MHz and 800 MHz, respectively. To keep the node voltages nearly unchanged, the designer reduces R_B and R_C by a factor of 2 to 50 kΩ and 4 kΩ, respectively. Assume $r_x = 50$ Ω, and recall that $V_A = 100$ V and that C_μ remains constant at 1 pF. As before, the amplifier is fed with a source having $R_{sig} = 5$ kΩ and feeds a load $R_L = 5$ kΩ. Find the new values of A_M, f_H, and the gain–bandwidth product, $|A_M| f_H$. Comment on the results. Note that the price paid for whatever improvement in performance is achieved is an increase in power. By what factor does the power dissipation increase?

***5.158** The purpose of this problem is to investigate the high-frequency response of the CE amplifier when it is fed with a relatively large source resistance R_{sig}. Refer to the amplifier in Fig. 5.71(a) and to its high-frequency equivalent-circuit model and the analysis shown in Fig. 5.72. Let $R_B \gg R_{sig}$, $r_x \ll R_{sig}$, $R_{sig} \gg r_\pi$, $g_m R'_L \gg 1$, and $g_m R'_L C_\mu \gg C_\pi$.

Under these conditions, show that:

(a) the midband gain $A_M \cong -\beta(R'_L/R_{sig})$.
(b) the upper 3-dB frequency $f_H \cong 1/(2\pi C_\mu \beta R'_L)$.
(c) the gain–bandwidth product $A_M f_H \cong 1/(2\pi C_\mu R_{sig})$.

Evaluate this approximate value of the gain–bandwidth product for the case $R_{sig} = 25$ kΩ and $C_\mu = 1$ pF. Now, if the transistor is biased at $I_C = 1$ mA and has $\beta = 100$, find the midband gain and f_H for the two cases $R'_L = 25$ kΩ and $R'_L = 2.5$ kΩ. On the same coordinates, sketch Bode plots for the gain magnitude versus frequency for the two cases. What f_H is obtained when the gain is unity? What value of R'_L corresponds?

5.159 Consider the common-emitter amplifier of Fig. P5.159 under the following conditions: $R_{sig} = 5$ kΩ, $R_1 = 33$ kΩ, $R_2 = 22$ kΩ, $R_E = 3.9$ kΩ, $R_C = 4.7$ kΩ, $R_L = 5.6$ kΩ, $V_{CC} = 5$ V. The dc emitter current can be shown to be $I_E \cong 0.3$ mA, at which $\beta_0 = 120$, $r_o = 300$ kΩ, and $r_x = 50$ Ω. Find the input resistance R_{in} and the midband gain A_M. If the transistor is specified to have $f_T = 700$ MHz and $C_\mu = 1$ pF, find the upper 3-dB frequency f_H.

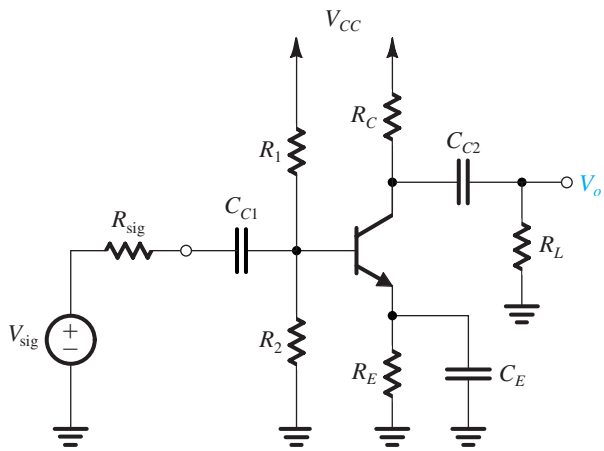


FIGURE P5.159

5.160 For a version of the CE amplifier circuit in Fig. P5.159, $R_{sig} = 10\ k\Omega$, $R_1 = 68\ k\Omega$, $R_2 = 27\ k\Omega$, $R_E = 2.2\ k\Omega$, $R_C = 4.7\ k\Omega$, and $R_L = 10\ k\Omega$. The collector current is 0.8 mA, $\beta = 200$, $f_T = 1$ GHz, and $C_\mu = 0.8$ pF. Neglecting the effect of r_x and r_o, find the midband voltage gain and the upper 3-dB frequency f_H.

5.161 The amplifier shown in Fig. P5.161 has $R_{sig} = R_L = 1\ k\Omega$, $R_C = 1\ k\Omega$, $R_B = 47\ k\Omega$, $\beta = 100$, $C_\mu = 0.8$ pF, and $f_T = 600$ MHz.

(a) Find the dc collector current of the transistor.
(b) Find g_m and r_π.
(c) Neglecting r_o, find the midband voltage gain from base to collector (neglect the effect of R_B).
(d) Use the gain obtained in (c) to obtain the component of R_{in} that arises as a result of R_B. Hence find R_{in}.
(e) Find the overall gain at midband.
(f) Find C_{in}.
(g) Find f_H.

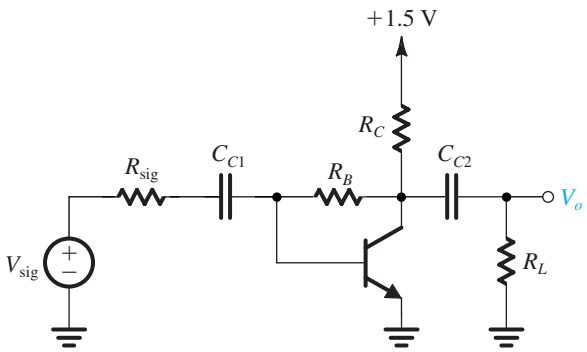


FIGURE P5.161

***5.162** Refer to Fig. P5.162. Utilizing the BJT high-frequency hybrid-π model with $r_x = 0$ and $r_o = \infty$, derive an expression for $Z_i(s)$ as a function of r_e and C_π. Find the frequency at which the impedance has a phase angle of 45° for the case in which the BJT has $f_T = 400$ MHz and the bias current is relatively high. What is the frequency when the bias current is reduced so that $C_\pi \simeq C_\mu$? Assume $\alpha = 1$.

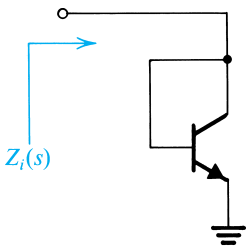


FIGURE P5.162

5.163 For the amplifier in Fig. P5.159, whose component values were specified in Problem 5.159, let $C_{C1} = C_{C2} = 1\ \mu$F, and $C_E = 10\ \mu$F. Find the break frequencies f_{P1}, f_{P2}, and f_{P3} resulting for C_{C1}, C_E, and C_{C2}, respectively. Note that R_E has to be taken into account in evaluating f_{P2}. Hence, estimate the value of the lower 3-dB frequency f_L.

D5.164 For the amplifier described in Problem 5.163, design the coupling and bypass capacitors for a lower 3-dB frequency of 100 Hz. Design so that the contribution of each of C_{C1} and C_{C2} to determining f_L is only 5%.

5.165 Consider the circuit of Fig. P5.159. For $R_{sig} = 10\ k\Omega$, $R_B \equiv R_1 // R_2 = 10\ k\Omega$, $r_x = 100\ \Omega$, $r_\pi = 1\ k\Omega$, $\beta_0 = 100$, and $R_E = 1\ k\Omega$, what is the ratio C_E/C_{C1} that makes their contributions to the determination of f_L equal?

***D5.166** For the common-emitter amplifier of Fig. P5.166, neglect r_x and r_o, and assume the current source to be ideal.

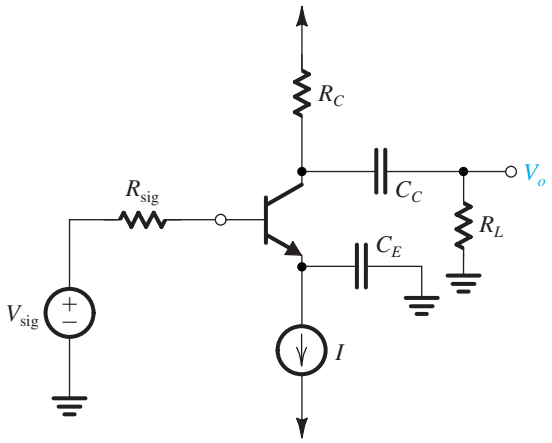


FIGURE P5.166

(a) Derive an expression for the midband gain.
(b) Derive expressions for the break frequencies caused by C_E and C_C.
(c) Give an expression for the amplifier voltage gain $A(s)$.
(d) For $R_s = R_C = R_L = 10\ k\Omega$, $\beta = 100$, and $I = 1$ mA, find the value of the midband gain.
(e) Select values for C_E and C_C to place the two break frequencies a decade apart and to obtain a lower 3-dB frequency of 100 Hz while minimizing the total capacitance.
(f) Sketch a Bode plot for the gain magnitude, and estimate the frequency at which the gain becomes unity.
(g) Find the phase shift at 100 Hz.

5.167 The BJT common-emitter amplifier of Fig. P5.167 includes an emitter degeneration resistance R_e.

(a) Assuming $\alpha \cong 1$, neglecting r_x and r_o, and assuming the current source to be ideal, derive an expression for the small-signal voltage gain $A(s) \equiv V_o/V_{sig}$. Hence find the midband gain A_M and the lower 3-dB frequency f_L.
(b) Show that including R_e reduces the magnitude of A_M by a certain factor. What is this factor?

(c) Show that including R_e reduces f_L by the same factor as in (b) and thus one can use R_e to trade-off gain for bandwidth.
(d) For $I = 1$ mA, $R_C = 10$ kΩ, and $C_E = 100$ μF, find $|A_M|$ and f_L with $R_e = 0$. Now find the value of R_e that lowers f_L by a factor of 5. What will the gain become?

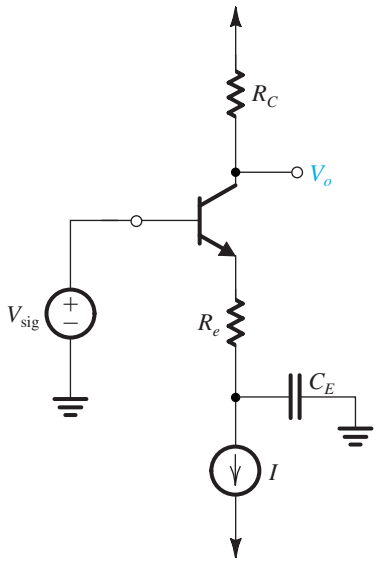


FIGURE P5.167

SECTION 5.10: THE BASIC BJT DIGITAL LOGIC INVERTER

5.168 Consider the inverter circuit in Fig. 5.74. In Exercise 5.53, the following expression is given for V_{OH} when the inverter is driving N identical inverters:

$$V_{OH} = V_{CC} - R_C \frac{V_{CC} - V_{BE}}{R_C + R_B/N}$$

For the same component values used in the analysis in the text (i.e., $V_{CC} = 5$ V, $R_C = 1$ kΩ, $R_B = 10$ kΩ, and $V_{BE} = 0.7$ V), find the maximum value of N that will still guarantee a high noise margin, NM_H, of at least 1 V. Assume $\beta = 50$ and $V_{CEsat} = 0.2$ V.

5.169 The purpose of this problem is to find the power dissipation of the inverter circuit of Fig. 5.74 in each of its two states. Assume that the component values are as given in the text (i.e., $V_{CC} = 5$ V, $R_C = 1$ kΩ, $R_B = 10$ kΩ, and $V_{BE} = 0.7$ V).

(a) With the input low at 0.2 V, the transistor is cut off. Let the inverter be driving 10 identical inverters. Find the total current supplied by the inverter and hence the power dissipated in R_C.
(b) With the input high and the transistor saturated, find the power dissipated in the inverter, neglecting the power dissipated in the base circuit.
(c) Use the results of (a) and (b) to find the average power dissipation in the inverter.

D5.170 Design a transistor inverter to operate from a 1.5-V supply. With the input connected to the 1.5-V supply through a resistor equal to R_C, the total power dissipated should be 1 mW, and forced β should be 10. Use $V_{BE} = 0.7$ V and $V_{CEsat} = 0.2$ V.

5.171 For the circuit in Fig. P5.171, consider the application of inputs of 5 V and 0.2 V to X and Y in any combination, and find the output voltage for each combination. Tabulate your results. How many input combinations are there? What happens when any input is high? What happens when both inputs are low? This is a logic gate that implements the NOR function: $Z = \overline{X + Y}$.

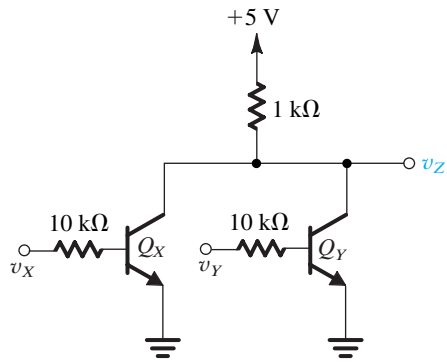


FIGURE P5.171

5.172 Consider the inverter of Fig. 5.74 with a load capacitor C connected between the output node and ground. We wish to find the contribution of C to the low-to-high delay time of the inverter, t_{PLH}. (For the formal definition of inverter delays, refer to Fig. 1.35.) Toward that end, assume that prior to $t = 0$, the transistor is on and saturated and $v_O = V_{OL} = V_{CEsat}$. Then, at $t = 0$, let the input fall to the low level, and assume that the transistor turns off instantaneously. Note that neglecting the turn-off time of a saturated transistor is an unrealistic assumption, but one that will help us concentrate on the effect of C. Now, with the transistor cut off, the capacitor will charge through R_C, and the output voltage will rise exponentially from $V_{OL} = V_{CEsat}$ to $V_{OH} = V_{CC}$. Find an expression for $v_O(t)$. Calculate the value of t_{PLH}, which in this case is the time for v_O to rise to $\frac{1}{2}(V_{OH} + V_{OL})$. Use $V_{CC} = 5$ V, $V_{CEsat} = 0.2$ V, $R_C = 1$ kΩ, and $C = 10$ pF. (*Hint:* The step response of RC circuits is reviewed in Section 1.7 and in greater detail in Appendix F.)

***5.173** Consider the inverter circuit of Fig. 5.74 with a load capacitor C connected between the output node and ground. We wish to find the contribution of C to the high-to-low delay time of the inverter, t_{PHL}. (For the formal definition of the inverter delays, refer to Fig. 1.35.) Toward that end,

assume that prior to $t = 0$, the transistor is off and $v_O = V_{OH} = V_{CC}$. Then, at $t = 0$, let the input rise to the high level, and assume that the transistor turns on instantaneously. Note that neglecting the delay time of the transistor is unrealistic but will help us concentrate on the effect of the load capacitance C. Now, because C cannot discharge instantaneously, the transistor cannot saturate immediately. Rather, it will operate in the active mode, and its collector will supply a constant current of $\beta(V_{CC} - V_{BE})/R_B$. Find the Thévenin equivalent circuit for discharging the capacitor, and show that the voltage will fall exponentially, starting at V_{CC} and heading toward a large negative voltage of $[V_{CC} - \beta(V_{CC} - V_{BE})R_C/R_B]$. Find an expression for $v_O(t)$. This exponential discharge will stop when v_O reaches $V_{OL} = V_{CEsat}$ and the transistor saturates. Calculate the value of t_{PHL}, which in this case is the time for v_O to fall to $\frac{1}{2}(V_{OH} + V_{OL})$. Use $V_{CC} = 5$ V, $V_{CEsat} = 0.2$ V, $V_{BE} = 0.7$ V, $R_B = 10$ kΩ, $R_C = 1$ kΩ, $\beta = 50$, and $C = 10$ pF. If you have solved Problem 5.172, compare the value of t_{PHL} to that of t_{PLH} found there, and find the inverter delay, t_P. (*Hint:* The step response of *RC* circuits is reviewed in Section 1.7 and in greater detail in Appendix F).