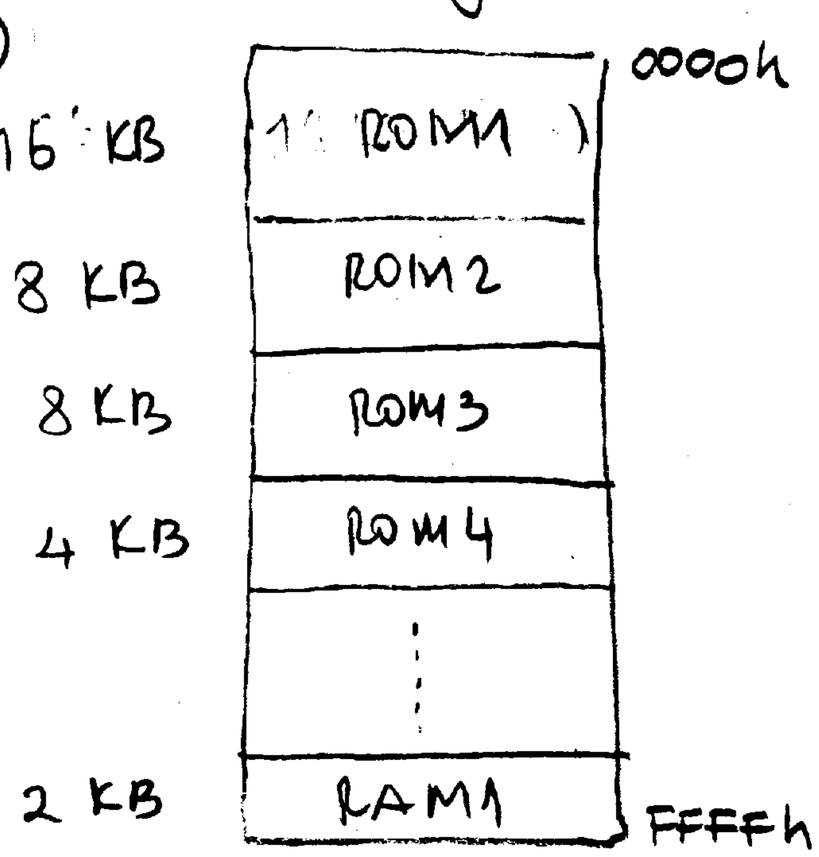
INTRODUCTION TO MICROCOMPUTERS FIRST EXAM

Dr. Salih FAPIL

October 24, 2008

#1)



An 8085 baised microprocessor system needs 36 KByte ROM and 2 KByte RAM memory. ROM and RAM memory are composed of memory ICs shown in the figure. Design a memory decoder circuitry that places the memory ICs into the addres ranges shown in the figure. Use one '138 (3-to-8) decoder IC and logic gates if necassary. There should not be any overlapping addresses in your design

#2)

a) Obtain $\overline{IOR}$, $\overline{IOW}$, $\overline{MEMR}$, $\overline{MEMW}$ by using $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$ strobe signals and a '138 decoder.

b) Consider the microprocessor system given in question 1. Assume that RAM1 IC is removed from the memory decoder circuitry. Suppose also that the system program of the microprocessor system uses subroutines and hardware interrupts. Does the system program work properly? Why?

c) Explain the functions of the folbowing pins of 8085 shortly

READY, $\overline{RESET-IN}$, RESET-OUT, HOLD, HLDA, CLK-OUT,

INTRODUCTION TO MICROCOMPUTERS FIRST MIDTERM

EXAM SOLUTION MANUAL

Dr. Salih FADIL

October 24, 2008

#1)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
ROM1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 0000h	16 KB
	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 3FFFh	
ROM2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 4000h	8 KB
	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= 5FFFh	
ROM3	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	= 6000h	8 KB
	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 7FFFh	
ROM4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 8000h	4 KB
	1	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	= 8FFFh	

BLANK..!

RAM1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	= F800h	2 KB
	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= FFFFh	

16 K = $2^4\ 2^{10}$ → 14 bits change

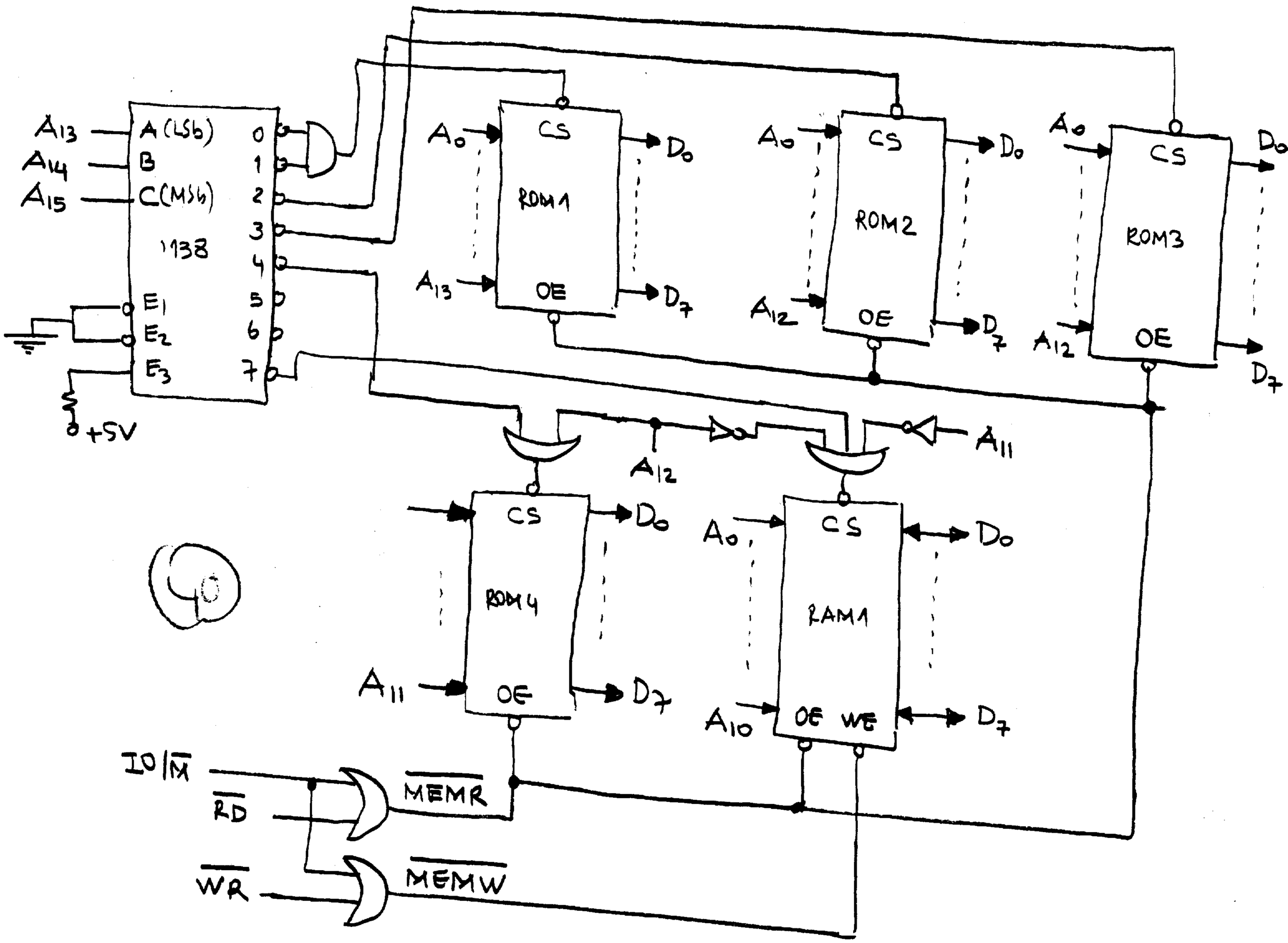
8 K = $2^3\ 2^{10}$ → 13 bits change

4 K = $2^2\ 2^{10}$ → 12 bits change

2 K = $2^1\ 2^{10}$ → 11 bits change

✓ No overlapping addresses

✓ One 3-to-8 decoder and logic gates if necessary.

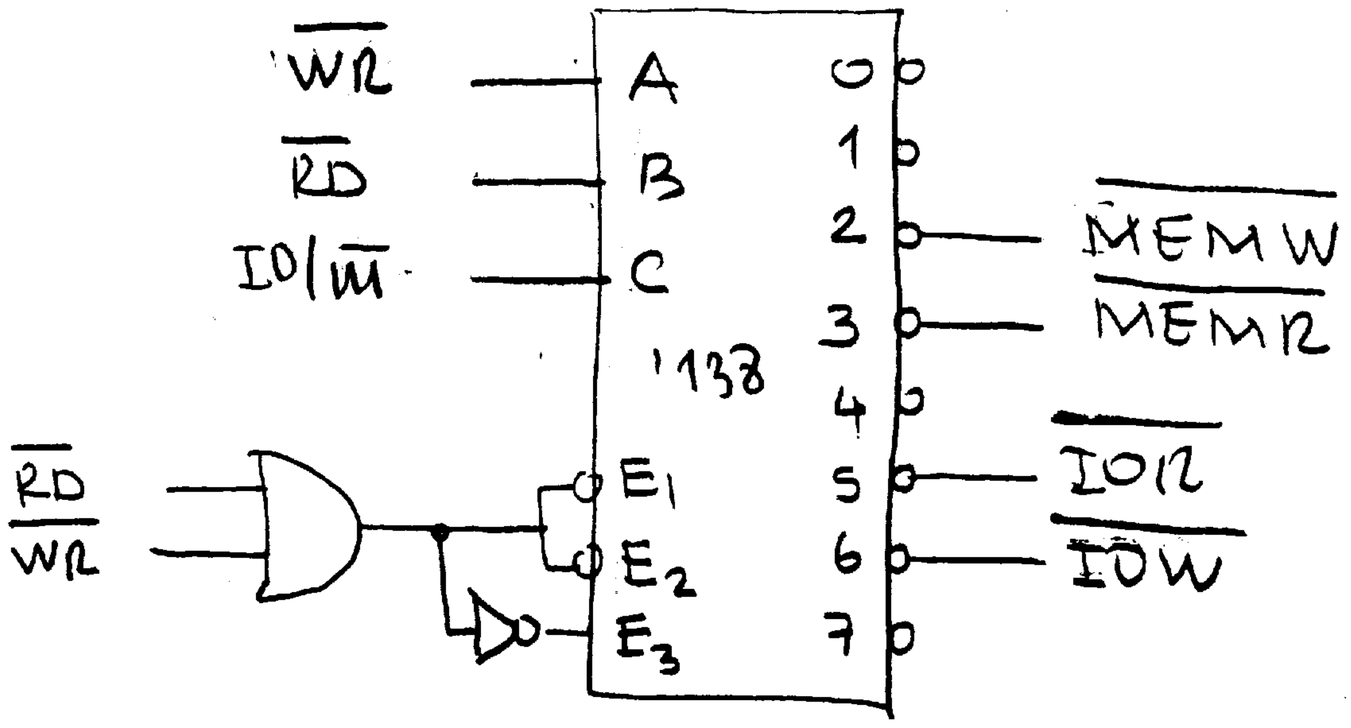


(9)

#2)

(15)

a)



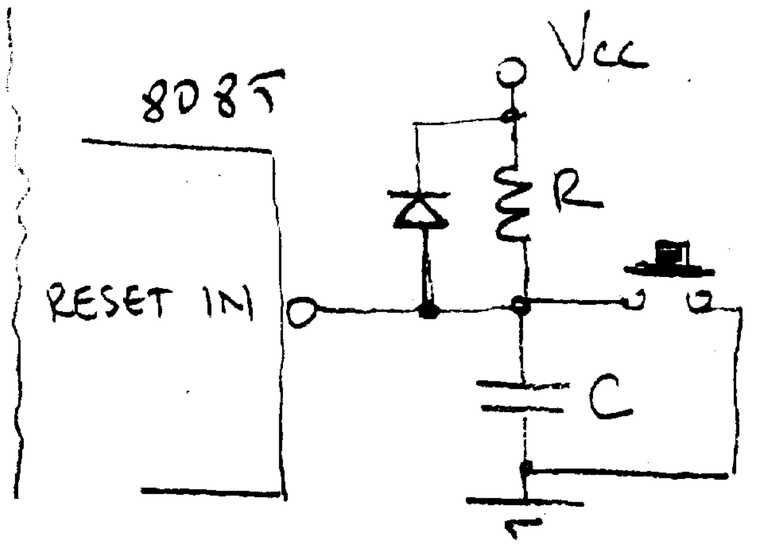
when the microprocessor neither reads nor writes, all outputs of 138 are logic 1, (disabled!)

(C)	(B)	(A)	
IO/M	RD	WR	
6 ← 1	1	0 →	IOW
5 ← 1	0	1 →	IOR
2 ← 0	1	0 →	MEMW
3 ← 0	0	1 →	MEMR

b) When RAM1 IC in the system given in problem
(17) one is removed from the memory of the system, the system program, which uses subroutines, hardware interrupts (interrupt service routines), never works properly, since to keep track of subroutine calls, the system needs a stack memory. Stack memory must a RAM memory.

c) (3) READY: It is an input pin. When it is actived (logic 1), 8085 works normaly. When it is disactivated
(18) it enters wait states, it does nothing. It can be used to interface 8085 with slow devices.

(3) $\overline{\text{RESET IN}}$: It is an active low input pin. When this pin sees a logic low signal, microprocessor is reset, that is PC is loaded with 0000h and. some internal flip-flops are loaded with default values. The necessary $\overline{\text{RESET-IN}}$ signal can be supplied by the circuit given in the above circuit



(3) RESET_OUT: It is an output pin. The complemented form of applied $\overline{\text{RESET-IN}}$ signal is seen on this pin and is used to RESET prephiral devices with high RESET,

(3) HOLD: It is an active high input pin. When it is activated microprocessor makes HLDA acknowledgement signal (output) active and then relinguishes data and address busses.

(3) HLDA: It is an output pin which gives active high acknowledgement signal indicating that 8085 relinguished the busses

(3) CLK-OUT: It is an output pin that gives a symmetric clock signal whose frequency is equal to the frequency of the cystal.