INTRODUCTION TO MICROCOMPUTERS FINAL EXAM

(Summer School - 2009)

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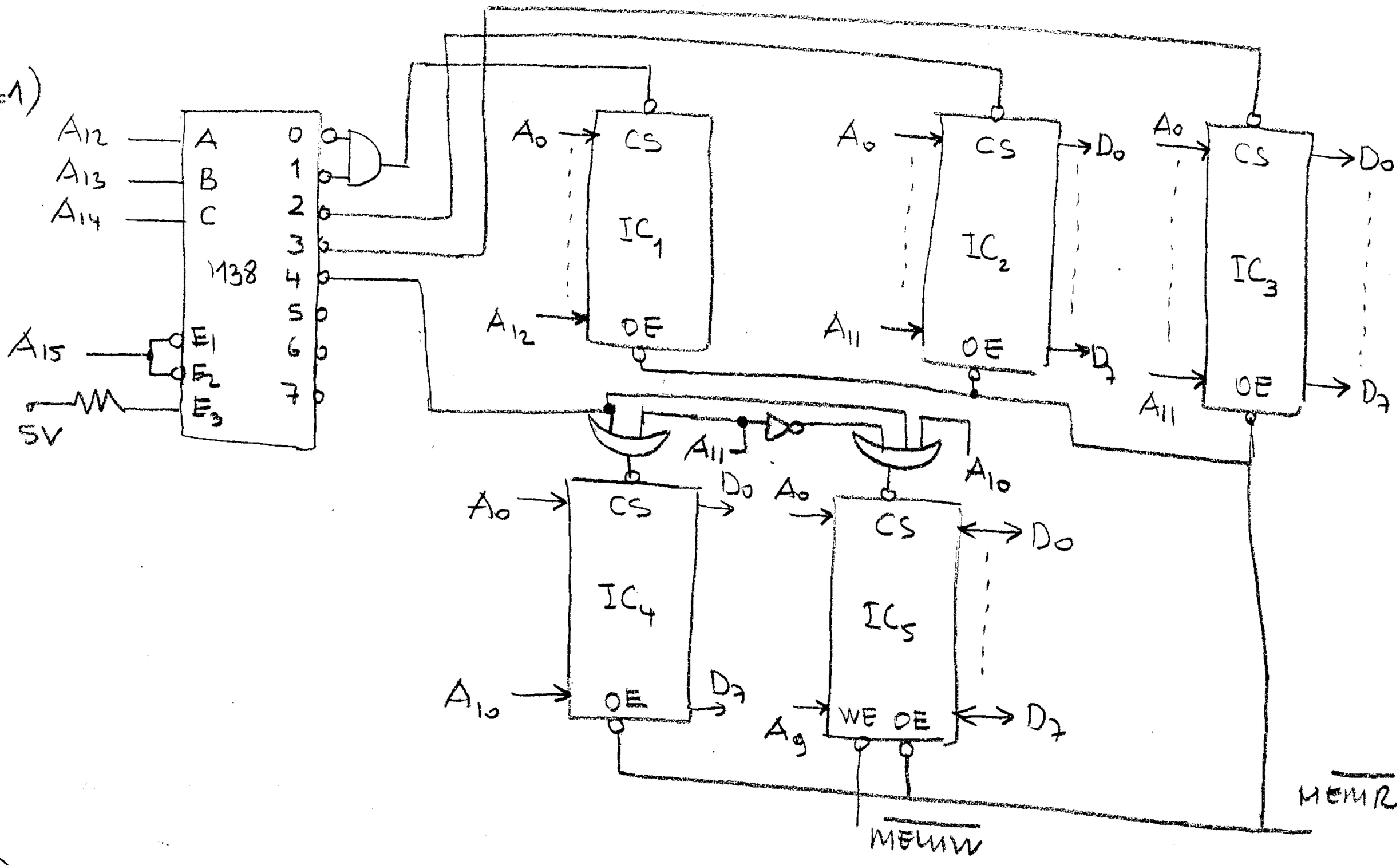
#1)



a)

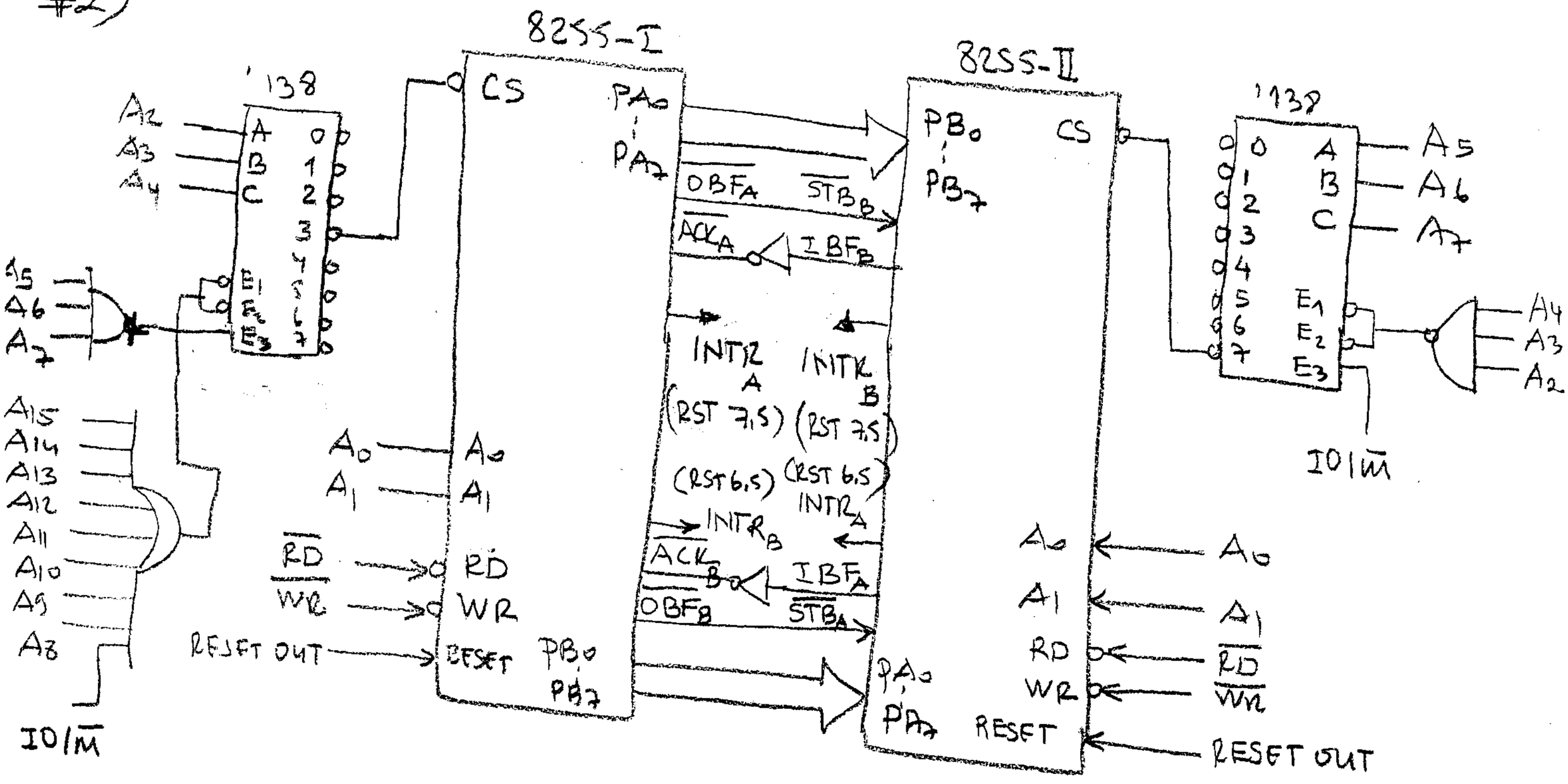
Consider the memory decoder civcuitry given in the above figure and fill the following table.

IC #	Type (ROM or RAM)	Capacity (KB)	Selected addr. range
1			
2			
3			
4			
5			

see back

b) Realize the same decoder circuitry by using minimum capacity PROM. Give the PROM programming table and connection diagram together. Assume that PROM has two enables, where one of them is active high and the other one is active low.

#2)



: This program is written for 8255-I † port A

```
        ORG   0000h
        LXI   SP, 8000h  ; 7C00h-7FFF | SRAM
        MVI   A, SAY1
        Instruction-1
        MVI   A, SAY2
        Instruction-2
        MVI   A, SAY3
        Instruction-3
```

see back

```
        MVI   A, 08h
        SIM
        EI
        NOP
        LXI   H, 7C00h
        MVI   C, 05h
        NOP
        ORG   SAY4
        JMP   iPROG_1
        NOP
        NOP
PROG_1: MOV   A, M
        STA   SAY5
        INX   H
        DCR   C
        JNZ   TAMAM
KK:     LXI   H, 7C00h
        MVI   C, 05h
TAMAM:  EI
        RET
```

; This program is written for 8255-II port B

```
        ORG   0000h
        LXI   SP, 0FFFFh ; FC00h - FFFFh SRAM.
        MVI   A, N1
        Instr-1
        MVI   A, N2
        Instr_2
        MVI   A, N3
        Instr_3
```

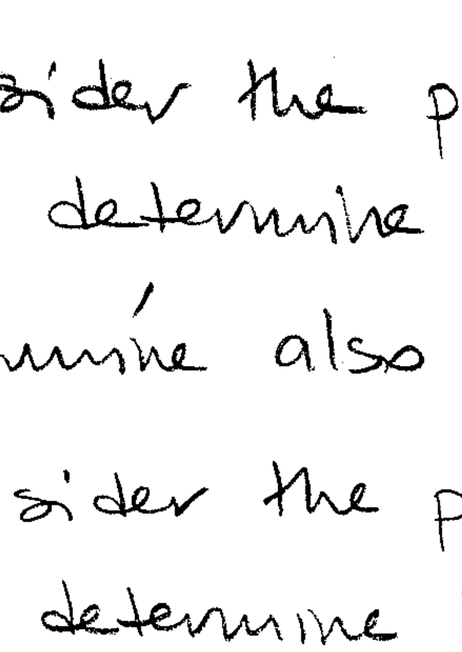
See back!

```
        MVI A, N4
        SIM
        EI
        LXI   H, 0FC00h
        MVI   B, 00h
LP:     NOP
        NOP
        NOP
        NOP
        JMP   LP
        ORG   003Ch
        JMP   SUB
        NOP
        NOP
SUB:    IN    N5
        ADD   B
        MOV   B, A
        MOV   M, B
        EI
        RET
```

a) Consider the program part written for 8255-I port A and determine the values for SAY1, SAY2, SAY3, SAY4 SAY5. Determine also Instruction-1, Instruction-2 and Instruction-3.

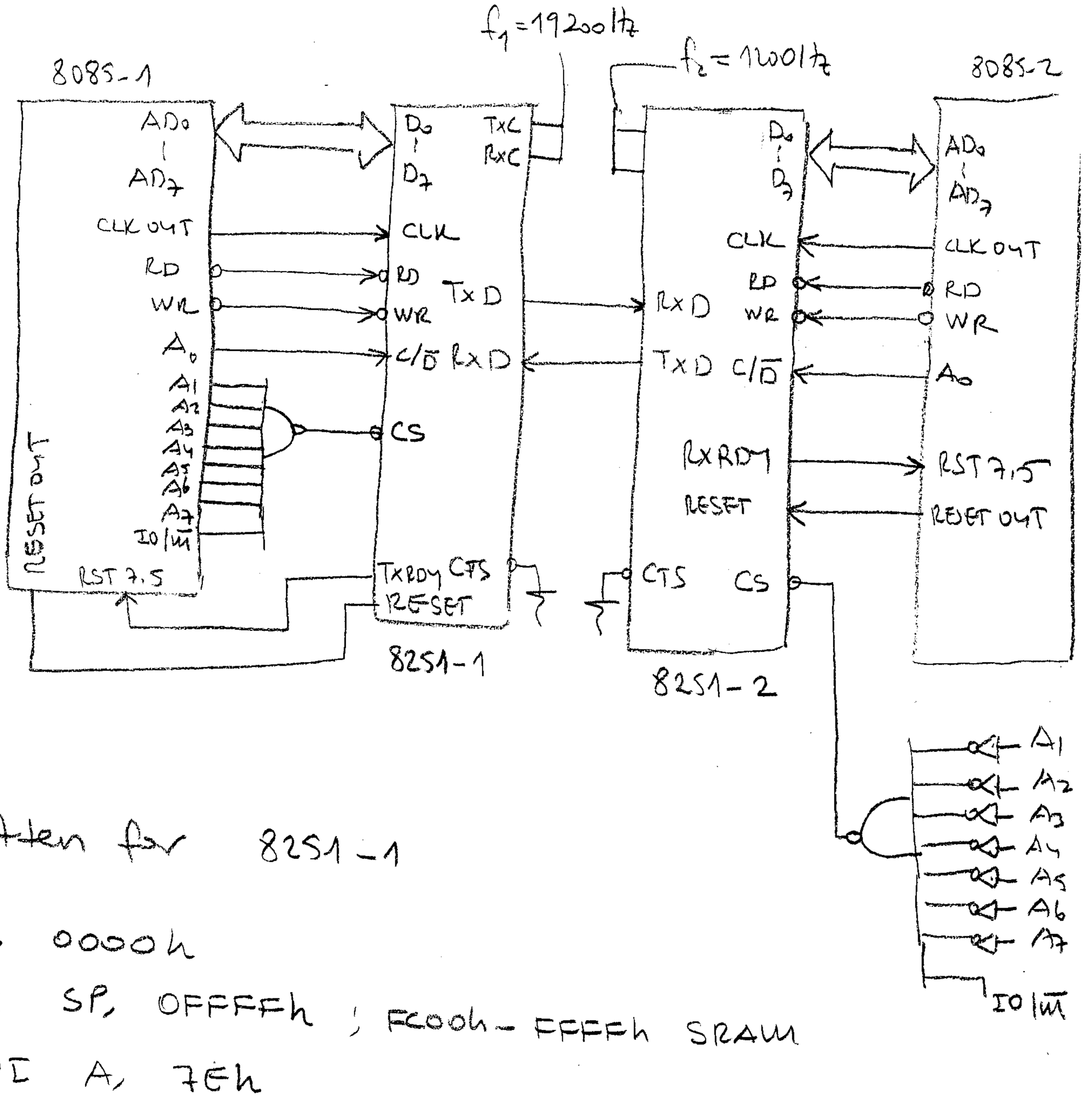
b) Consider the program part written for 8255-II port B, and determine the values for N1, N2, N3, N4, N5. Determine also, Instr-1, Instr-2 and Instr-3.

c) What do these two programs do? explain shortly.



Determine the memory content whose address is FC00h for the system shown on the right hand side when the program which is written for 8255-I, reaches the point labeled as KK.

#3)



; Written for 8251-1

```
ORG   0000h
LXI   SP, 0FFFFh ; FC00h - FFFFh SRAM
MVI   A, 7Eh
Instruction - 1
MVI   A, 51
Instruction - 2
NOP
NOP
```

```
        Instruction-3
        EI

        LXI   H, OFC00h
        ORG   003Ch
        JMP   SUBS
        NOP
SUBS:   MOV   A, M
        OUT   S2
        EI
        RET

; Written for 8251-2

        ORG   0000h
        LXI   SP, OFFFFh
        MVI   A, DAT1
        OUT   DAT2
        MVI   A, DAT3
        OUT   DAT4
        NOP
        NOP
        LXI   H, 0FC00h
        MVI   A, 08h
        Ins-1
        EI
        NOP
        NOP
        ORG   003Ch
        JMP   SUBR
DONGU1  NOP
        NOP
        JMP   DONGU
```

```
        NOP
        NOP
SUBR!   IN    DAT5
        ANI   38h
        JNZ   Hoops
        IN    DAT6
        RRC
        RRC
        RRC
        RRC
        MOV   M, A
        EI
        RET
Hoops!  HLT
```

a) Determine the values of S1, S2 given in the program part written for 8251-1. Determine also Instruction-2, Instruction-3 given in the same program.

b) Determine the values of DAT1, DAT2, DAT3, DAT4, DAT5, DAT6. Determine also Ins-1 given in the same program

c) Assume that no error occurs in serial communications between 8251s. The system shown on the left hand side contains ABh in its memory location whose address is FC00h. Determine the content of the memory location of the system, given on the right hand side, The address of the location is also FC00h.

INTRODUCTION TO MICROCOMPUTERS FINAL EXAM SOLUTION MANUAL

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#1) The following binary memory map can be written a) for the given decoder circuitry

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11} A_{10} A_9 A_8	A_7 A_6 A_5 A_4	A_3 A_2 A_1 A_0	
IC_1	0	0	0	0	0 0 0 0	0 0 0 0	0 0 0 0	= 0000h
	0	0	0	1	1 1 1 1	1 1 1 1	1 1 1 1	= 1FFFh
IC_2	0	0	1	0	0 0 0 0	0 0 0 0	0 0 0 0	= 2000h
	0	0	1	0	1 1 1 1	1 1 1 1	1 1 1 1	= 2FFFh
IC_3	0	0	1	1	0 0 0 0	0 0 0 0	0 0 0 0	= 3000h
	0	0	1	1	1 1 1 1	1 1 1 1	1 1 1 1	= 3FFFh
IC_4	0	1	0	0	0 0 0 0	0 0 0 0	0 0 0 0	= 4000h
	0	1	0	0	0 1 1 1	1 1 1 1	1 1 1 1	= 47FFh
IC_5	0	1	0	0	1 0 0 0	0 0 0 0	0 0 0 0	= 4800h
	0	1	0	0	1 0 1 1	1 1 1 1	1 1 1 1	= 4BFFh

does not change bits for '138 ↑ selection

IC #	Type (ROM or RAM)	Capacity (KB)	Selected address range
1	ROM	8 KB	0000h – 1FFFh
2	ROM	4 KB	2000h – 2FFFh
3	ROM	4 KB	3000h – 3FFFh
4	ROM	2 KB	4000h – 47FFh
5	RAM	1 KB	4800h – 4BFFh

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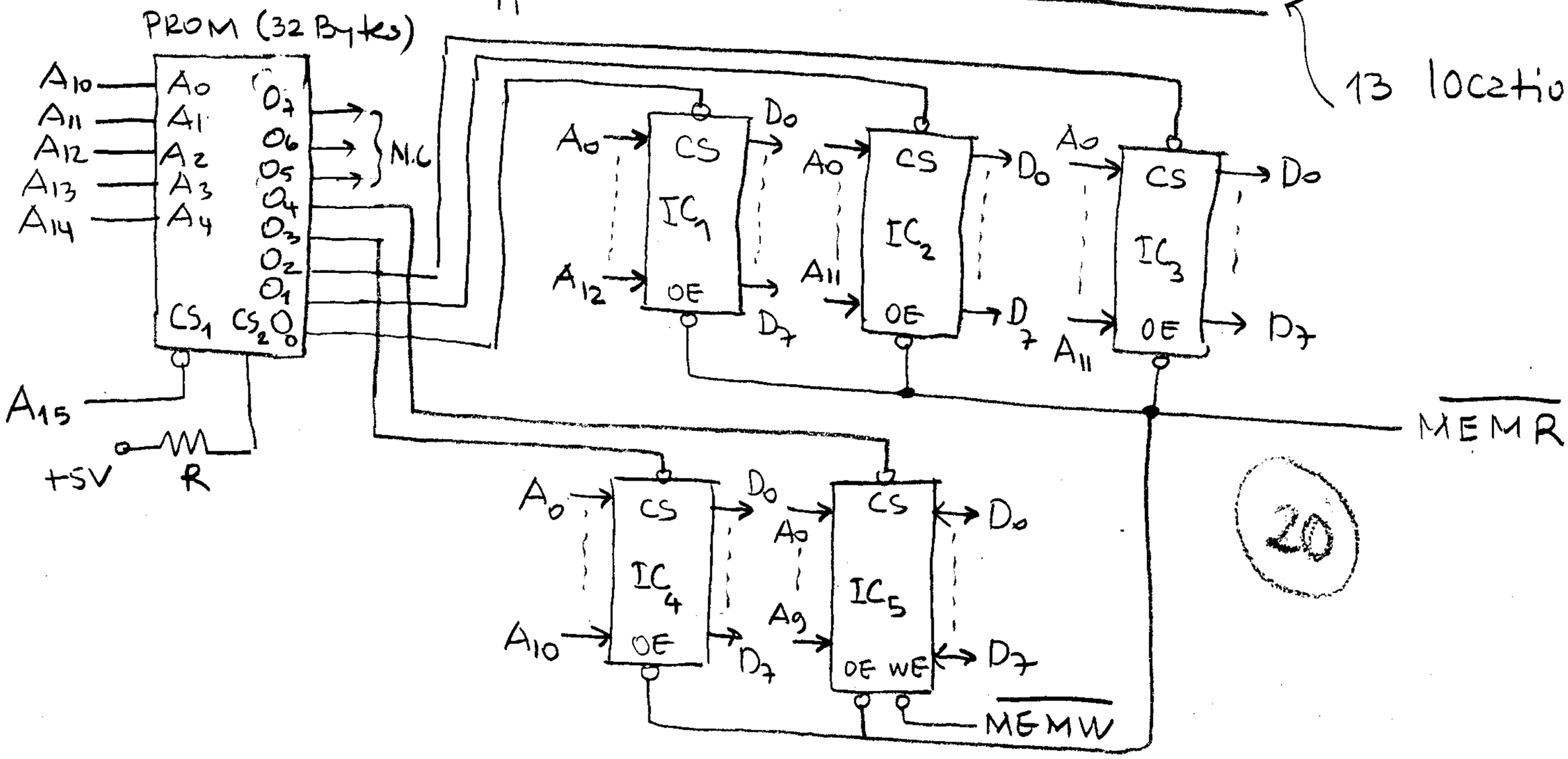
b) In order to select minimum capacity memory IC (IC_5, 1 KB), 6 most significant address bits should be used, but A_{15} remains logic 0 throughout the memory space used, A_{15} can be used to enable the PROM. So, 5 address bits should be used to select all of the IC_s.

Capacity of the PROM = $2^5 = 32$ bytes. (Minimum)

Connected addr pins

INPUTS → A_{14} A_{13} A_{12} A_{11} A_{10}					OUTPUTS O_7 O_6 O_5 O_4 O_3 O_2 O_1 O_0	
A_4	A_3	A_2	A_1	A_0		
0	0	0	0	0	1 1 1 1 1 1 1 0	for IC_1 (8 locations)
0	0	1	1	1	1 1 1 1 1 1 1 0	
0	1	0	0	0	1 1 1 1 1 1 0 1	for IC_2 (4 locations)
0	1	0	1	1	1 1 1 1 1 1 0 1	
0	1	1	0	0	1 1 1 1 1 0 1 1	for IC_3 (4 locations)
0	1	1	1	1	1 1 1 1 1 0 1 1	
1	0	0	0	0	1 1 1 1 0 1 1 1	For IC_4 (2 locations)
1	0	0	0	1	1 1 1 1 0 1 1 1	
1	0	0	1	0	1 1 1 0 1 1 1 1	For IC_5 (1 locations)
the other locations					1 1 1 1 1 1 1 1	13 locations



#2)

a) For the system on the left hand side.

It has memory mapped I/O decoder since $\overline{E_1} = \overline{E_2} = 0$ for, $IO/\overline{M} = 0$

A_{15} A_{14} A_{13} A_{12}	A_{11} A_{10} A_9 A_8	A_7 A_6 A_5 A_4	A_3 A_2	A_1 A_0	
0 0 0 0	0 0 0 0	1 1 1 0	1 1	0 0	= 00ECh
				0 1	= 00EDh
				1 0	= 00EEh
				1 1	= 00EFh

— 11 —

port-A Addr. = 00ECh
port-B Addr. = 00EDh
port-C Addr = 00EEh
control reg Addr = 00EFh

Mode word

7	6	5	4	3	2	1	0	
1	0	1	0	x	1	0	x	= A4h
				(0)			(0)	

SA11 = Mode word = 0A4h (2)

Instruction_1 ⇒ STA 00EFh (1)

BSR Word to make $INTE_A = 1$ ($PC_6 = 1$ in BSR)

7	6	5	4	3	2	1	0	
0	x	x	x	1	1	0	1	= 0Dh
	(0)	(0)	(0)					

BSR Word to make $INTE_B = 1$ ($PC_2 = 1$ in BSR)

7	6	5	4	3	2	1	0	
0	x	x	x	0	1	0	1	= 05h
	(0)	(0)	(0)					

SA12 = 0Dh (or 05h) (2)

Instruction-2 ⇒ STA 00EFh (1)

SA43 = 05 (or 0Dh) (2)

Instruction_3 ⇒ STA 00EFh (1)

SA44 = Vector addr. of RST 7.5 = 003Ch (1)

SA45 = Addr. of port A = 00ECh (1)

b) The system on the right hand side has I/O mapped I/O decoder since $E_3 = 1$ for $IO/\overline{M} = 1$

A_7	A_6	A_5	A_4	A_3	A_2	A_1 A_0	
1	1	1	1	1	1	0 0 = FCh	Addr. of port-A
	—"—					0 1 = FDh	" " port-B
						1 0 = FEh	" " port-C
						1 1 = FFh	" " control register

Mode Word

7	6	5	4	3	2	1	0	
1	0	1	1.	x	1	1	x	= B6h
				(0)			(0)	

To make $INTE_A = 1$ ($PC_4 = 1$ in BSR mode)

7	6	5	4	3	2	1	0	
0	x	x	x	1	0	0	1	= 09h
	(0)	(0)	(0)					

To make $INTE_B = 1$ ($PC_2 = 1$ in BSR mode)

7	6	5	4	3	2	1	0	
0	x	x	x	0	1	0	1	= 05h
	(0)	(0)	(0)					

N1 = Mode Word = 0B6h (2)

Instr-1 ⇒ OUT 0FFh (1)

N2 = BSR word for $INTE_A = 1$ = 09h (or 05h) (2)

Instr-2 ⇒ OUT 0FFh (1)

N3 = BSR word for $INTE_B = 1$ = 05h (or 09h) (2)

Instr-3 ⇒ OUT 0FFh (1)

MSE M7.5

7	6	5	4	3	2	1	0	
x	x	x	x	1	1	x	x	= 08h ← to open the mask of RST 7.5
(0)	(0)	(0)	(0)			(0)	(0)	

N4 = 08h (1)

N5 = Addr. of port B = 0FD h (1)

c) The program written for 8255-I sends the data located in SRAM locations of 7C00h – 7C04h continously in mode-1. It uses RST 7.5 interrupt to send data in mode-1

(6) The program written for 8255-II receives the data sent by the 8255-I and add them. The sum is also written to SRAM location of FC00h.

(5) When the program written for 8255-I reaches the point labeled as KK, all the data located at 7C00h – 7C04h has been sent to 8255-II. So the content of FC00h in the system being on the left hand side will contain the sum of data located at 7C00h - 7C04h.

$$\begin{array}{r} 10h \\ 15h \\ 20h \\ 25h \\ +\ 30h \\ \hline 9Ah \end{array}$$

(M) = 9Ah
FC00h

#3) For 8251-1 : it has I/O mapped I/O decoder

a)

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	1	1	1	0	= FEh Addr of data reg
		- 11 -					1	= FFh Addr of Control-Command-Status register

Control word

7	6	5	4	3	2	1	0	
0	1	1	1	1	1	1	0	→ So, asynchronous communication is used
1 stop bit		Even parity		8 data bits		16 x		

7Eh =

Command word : 00010101 = 15h.

Instruction-1 ⇒ OUT 0FFh (1)
S1 = Command word = 15h (2)
Instruction-2 ⇒ OUT 0FFh (2)
Instruction-3 ⇒ SIM (3)
S2 = Addr of data reg = 0FEh (2)

transmitter and receiver clock freq. = $\frac{19200}{16}$ = 1200 Hz.

b) For 8251-2 : It has also I/O mapped I/O decoder

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
0	0	0	0	0	0	0	0	= 00h
							1	= 01h

Control Word

7	6	5	4	3	2	1	0	
0	1	1	1	1	1	0	1	= 7Dh

The same as the ones belong to 8251-1

x1 → Since f_2 = 1200 Hz

DAT1 = Control Word = 7Dh (2)

DAT2 = Addr. of Control reg = 01h (2)

DAT3 = 15h = Command Word = 15h (2)

DAT4 = Addr. of Command reg. = 01h (2)

Ins-1 = SIM (2)

DAT5 = Addr. of Status reg. = 01h (2)

DAT6 = Addr. of data reg = 00h (2)

c) In those programs the data in SRAM memory location of 8085-1, whose address is FC00h, is sent to 8251-2. This data is received by 8251-2. After that it is swapped and written into SRAM memory location of 8085-2. So

(M) = ABh
FC00h
↑
8085-1

⟶

(M) = BAh
FC00h
↑
8085-2

(10)