INTRODUCTION TO MICROCOMPUTERS FINAL EXAM

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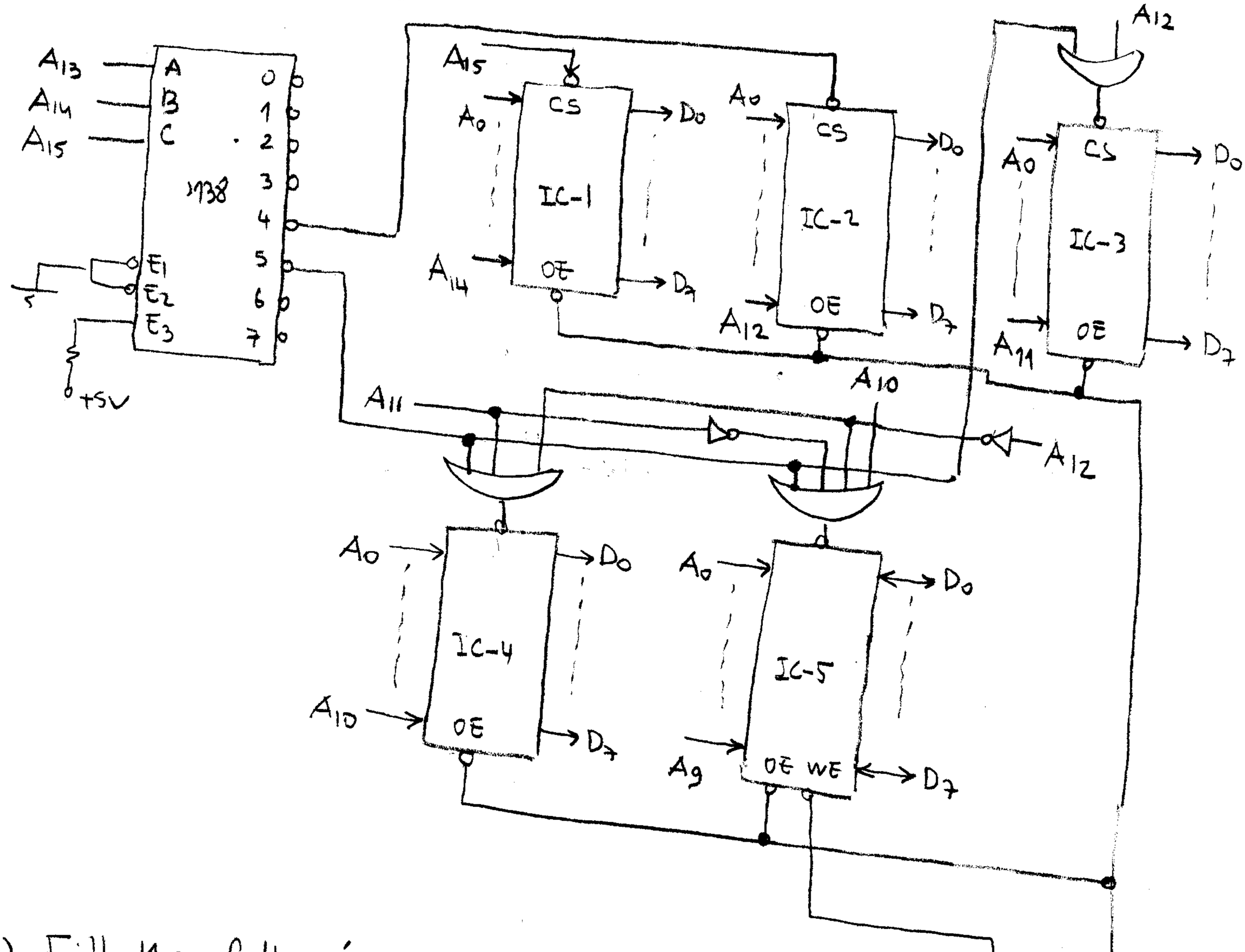
#1) Consider the following memory decoder circuitry given in the following figure.



a) Fill the following table.

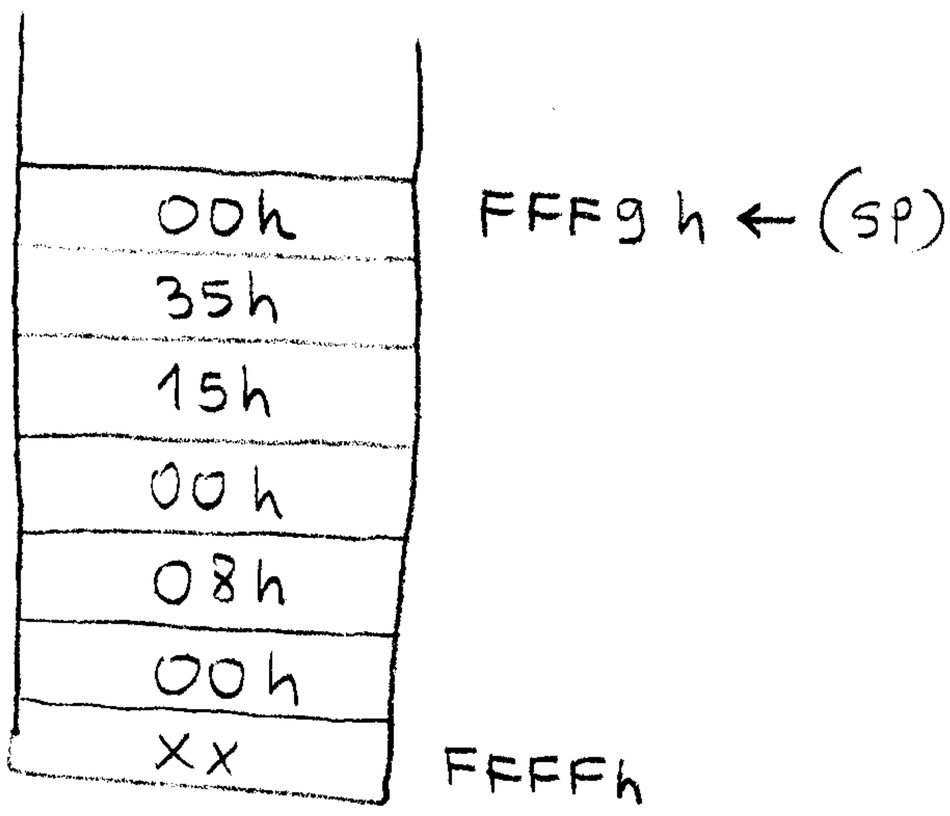
IC-#	Type	Capacity (KB)	Selected addr. range
1			
2			
3			
4			
5			

b) Design the same circuitry by using the minimum capacity PROM. Give the programming of the PROM as truth table and also draw the corresponding circuitry. Assume that PROM has two enables where one of them is active-low and the other is active-high. Note that both circuitry have no overlapping addresses.

#2)

```
        ORG   0000h
        LXI   SP, N-1
        NOP
LP:     NOP
        CALL  SBR-1
        NOP
KK:     NOP
        JMP   LP
        MVI   L, N-2
SBR-1:  MVI   H, N-3
LOOP-1: NOP
        CALL  SBR-2
        DCR   H
LL:     JNZ   LOOP-1
        RET
SBR-2:  PUSH  H
        MVI   H, 0FFh
LOOP-2: NOP
        NOP
AA:     DCR   H
        JNZ   LOOP-2
        POP   H
        RET
```

When the program reaches the point AA <u>first time</u>, (SP) = FFF9h.



Consider the assembly program part written for an 8085 microprocessor based system. The 8085 has 6 MHz qyristal.

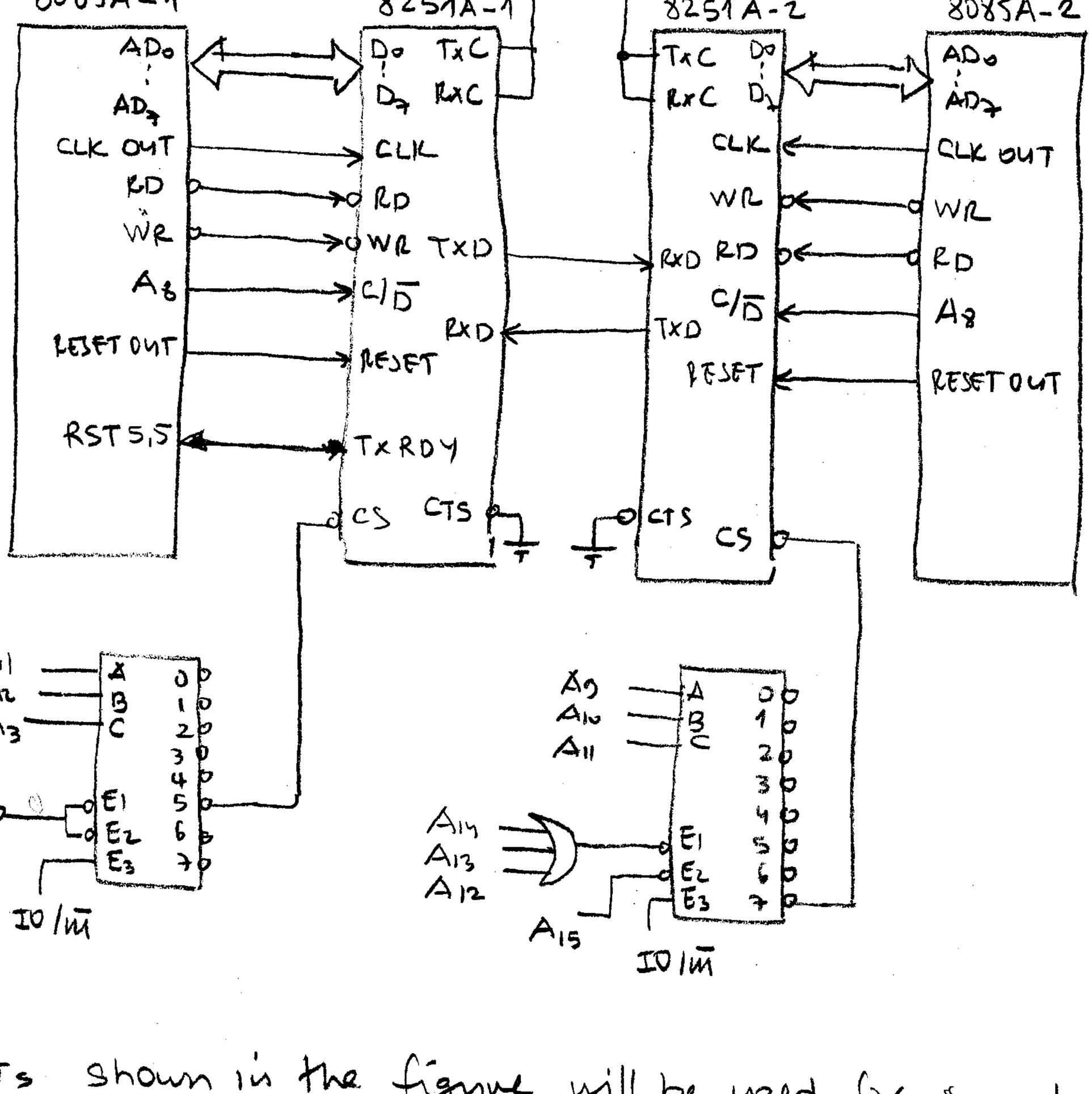
a) Determine the values for N-1, N-2 and N-3. Determine also starting addresses of the instructions labeled as KK and LL in the program. This addresses <u>must be found</u> by using the stack content.

b) Calculate the execution time for SBR-1 subroutine as ms.

see back →

c) Can the program be run correctly on the system whose memory decoder circuitry given in question 1, why ?

#3)



USARTs shown in the figure will be used for synchronous serial communication Consider the programming parts given in the following for 8251A-1 and 8251A-2

```
; for 8251A-1

    ORG   0000h
    LXI   SP, 0FFFFh ; FC00h - FFFFh, SRAM
```

```
        MVI  A, 1Ch
        OUT  N1
        MVI  A, 191h
        OUT  N3
        MVI  A, 92h
        OUT  N4
        MVI  A, N5
        OUT  N6
        MVI  A, 08h
        SIM
        EI
LOOP:   NOP
        NOP
        JMP  LOOP
        ORG  N7
        JMP  SUB
        NOP
SUB:    MVI  A, OFFh
        OUT  N8
        NOP
        EI
        RET.

; for 8251A-2

        ORG  0000h
        LXI  SP, OFFFFh ; FC00h-FFFFh. SRAM
        MVI  A, S1
        OUT  S2
        MVI  A, S3
        OUT  S4
        MVI  A, S5
        OUT  S6
        MVI  A, S7
        OUT  S8
        LXI  H, FC00h
LP:     NOP
        CALL SUB1
        NOP
        JMP  LP
        NOP
SUB1:   MVI  A, S9
        OUT  S10
LP1:    IN   S11
        ANI  40h
        JZ   LP1
LP2:    IN   S12
        ANI  02h
        JZ   LP2
        IN   S13
        ANI  S14
        JNZ  Hoops
        IN   S15
        CMA
        MOV  M, A
AA:     NOP
        RET
Hoops:  HLT
```

a) Determine the values of N1, ..., N8 in the program part written for 8251A-1

b) Determine the values of S1, ..., S15 in the program part written for 8251A-2

c) What is the value of f_2? Determine the content of memory location whose address is FC00h at point AA in the system on the right hand side. If an error occurs in serial communication between 8251A-1 and 8251A-2, what happens to the system on the right-hand side?

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SOLUTION MANUAL

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#1) The following binary memory map can be drawn from a) the examination of the given decoder circuit.

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
15 / 2 / 32 KB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 0000h	IC-1
	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 7FFFh	
13 / 2 / 8 KB	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 8000h	IC-2
	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= 9FFFh	
12 / 2 / 4 KB	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	= A000h	IC-3
	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	= AFFFh	
11 / 2 / 2 KB	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	= B000h	IC-4
	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	= B7FFh	
10 / 2 / 1 KB	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	= B800h	IC-5
	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	= BBFF	

IC-1 — IC4 : ROM type memory ICs, since they have only $\overline{OE}$ strobe signal inputs, because of it their data signals are unidirectional (input)

IC 5 : RAM type memory IC, since it has both $\overline{OE}$ and $\overline{WE}$ strobe signal inputs, because of it its data signals are bidirectional (input and output)

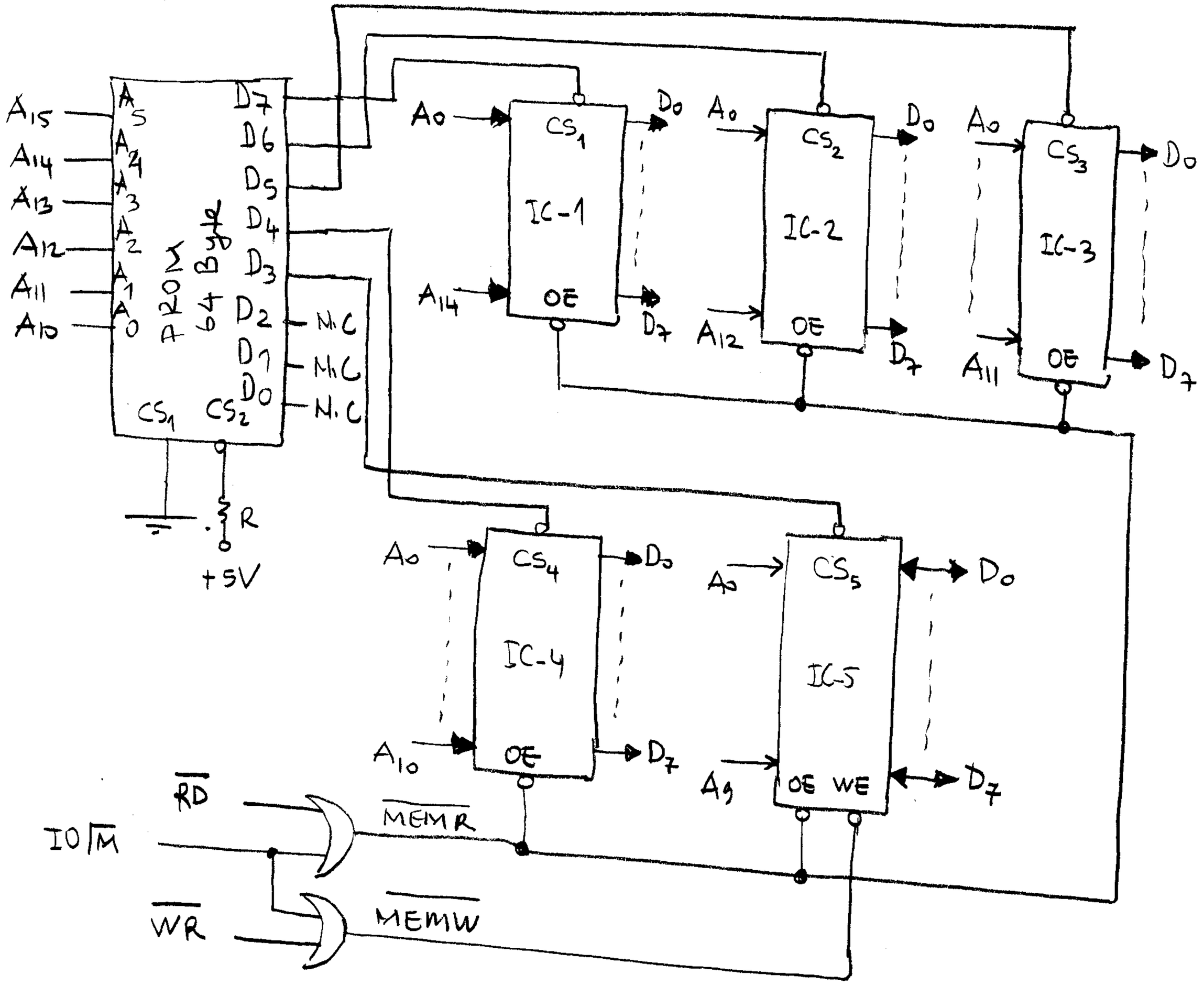
IC - #	Type	Capacity	Selected addr. range
1	ROM	32 KB	0000h – 7FFFh
2	ROM	8 KB	8000h – 9FFFh
3	ROM	4 KB	A000h – AFFFh
4	ROM	2 KB	B000h – B7FFh
5	RAM	1 KB	B800h – BBFFh

b) Since there is no any address bit that takes the same logic value, the number of necessary address inputs for PROM is determined by the capacity of the smallest memory IC (IC-5, 1KB). (in the given memory address range (0000h – BBFFh))

$2^6 = 64$ Byte

Connected addr. bits

	INPUTS						OUTPUTS								
	A_{15} A_{14} A_{13} A_{12} A_{11} A_{10}						$\overline{CS_1}$	$\overline{CS_2}$	$\overline{CS_3}$	$\overline{CS_4}$	$\overline{CS_5}$	N.C	N.C	N.C	← connected $\overline{CS}$ of ICs
	A_5	A_4	A_3	A_2	A_1	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
for IC-1	0	0	0	0	0	0	0	1	1	1	1	1	1	1	2^5 locations the same byte is written.
	⋮						⋮								
	0	1	1	1	1	1	0	1	1	1	1	1	1	1	
for IC-2	1	0	0	0	0	0	1	0	1	1	1	1	1	1	2^3 locations
	⋮						⋮								
	1	0	0	1	1	1	1	0	1	1	1	1	1	1	
for IC-3	1	0	1	0	0	0	1	1	0	1	1	1	1	1	2^2 locations
	⋮						⋮								
	1	0	1	0	1	1	1	1	0	1	1	1	1	1	
for IC-4	1	0	1	1	0	0	1	1	1	0	1	1	1	1	2^1 location
	1	0	1	1	0	1	1	1	1	0	1	1	1	1	
	1	0	1	1	1	0	1	1	1	1	0	1	1	1	$2^0 = 1$ location
the other locations							1	1	1	1	1	1	1	1	



#2) a)

* Since address for the bottom of the stack is FFFFh,
  N-1 = 0FFFFh
* the starting address of the NOP just after CALL SBR_1 is pushed onto stack in the order of High-Byte & Low-Byte. It is the first two-byte pushed onto stack.

```
      NOP    ; 0008h
KK:   NOP    ; 0009h , starting addr. in the memory
```

* the second two-byte pushed onto stack is the starting address of the instruction DCR H just after CALL SBR-2

```
        DCR   H          ; 0015h
LL:     JNZ   LOOP_1     ; 0016h
```

* the third two-byte pushed onto stack is the initial content of HL register pair (as High-Byte & Low-Byte)

(H) = 35h = N-2

(L) = 00h N-3 can not be determined!

b)

```
                                ; # of T-states
SBR-1:  MVI   H, 35h            ; 7      , 35h = 16x3+5 = 53_10
LOOP-1: NOP                     ; 4
        CALL  SBR-2             ; 18
        DCR   H                 ; 4
        JNZ   LOOP-1            ; 10/7
        RET                     ; 10
SBR-2:  PUSH  H                 ; 12
        MVI   H, OFFh           ; 7      , FFh = 255_10
LOOP-2  NOP                     ; 4
        NOP                     ; 4
        DCR   H                 ; 4
        JNZ   LOOP-2            ; 10/7
        POP   H                 ; 10
        RET                     ; 10
```

# of T-states in SBR-2 subroutine

$$12 + 7 + 254\underbrace{(4+4+4+10)}_{22} + 19 + 20 = 5646$$

# of T-states in SBR-1 subroutine

$$7 + (\underbrace{4+18+5646+4+10}_{5682}) \times 52 + 5679 + 10 = 301160$$

Execution time for SBR.1 is

$$301160 \times \frac{1}{3\times10^6} = 0.100386 \text{ sec.}$$
$$= 100.3 \text{ msec}$$

#3) For 8251A-1, sync. serial communication

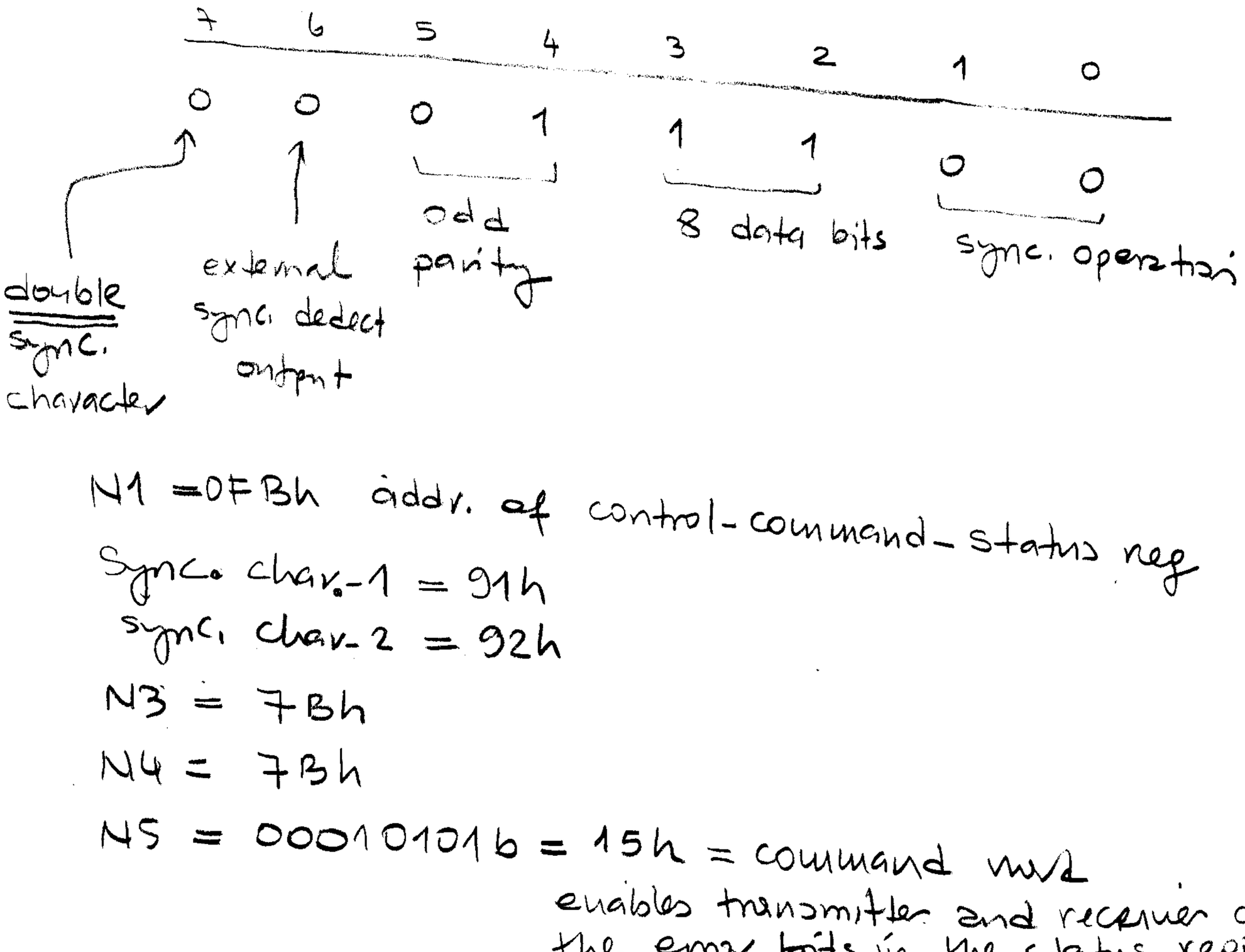
* It has isolated I/O decoder since $E_3 = 1$ for $IO/\overline{M} = 1$

OR

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	
0	1	1	1	1	0	1	0	= 7Ah → Addr. of data reg.
				11			1	= 7Bh → Addr. of control-command - status reg.

a) From examination of the program part written for 8251A-1 and the connection diagram, the followings can be deduced.

Mode word = 1Ch.



N1 = 0FBh addr. of control-command-status reg

Sync. char.-1 = 91h

sync. char-2 = 92h

N3 = 7Bh

N4 = 7Bh

N5 = 00010101b = 15h = command word
enables transmitter and receiver and clears the error bits in the status register

N6 = 7Bh

N7 = 002Ch vector addr. of RST 5.5

N8 = 7Ah addr. of data reg of 8251A-1

b) From examination of the program part written for 8251A-2 and the connection diagram, the followings can be deduced.

* It has I/O mapped I/O (isolated I/O) decoder since $E_3 = 1$ for $IO/\overline{M} = 1$.

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	
0	0	0	0	1	1	1	0	= 0Eh ← Addr. of data reg.
				- 11 -			1	= 0Fh ← Addr. of Control-Command - Status reg.

S-

S1 = 1Ch ; mode word

S2 = 0Fh ; addr. of Control-Command-Status reg.

S3 = 91h ; sync. char.-1

S4 = 0Fh

S5 = 92h ; sync. char.-2

S6 = 0Fh

S7 = 15h : command word = $\overset{0}{7}\,0\,0\,0\,1\,0\,1\,0$

S8 = 0Fh

S9 = $\underbrace{1\,0\,0\,1}_{9}\,\underbrace{0\,1\,0\,1}_{5}$ = 95h ⇒ command word 8251A-2 enters hunt mode (sync. dedect mode)

S10 = 0Fh

S11 = 0Fh addr. of status reg

40h = sync. characters dedect mask!

S12 = 0Fh addr of status reg.

02h = receiver ready dedect mask!

S13 = 0F addr of status reg.

S14 = 00111000 b = 38h FE & OE & PE dedect mask

S15 = 0E Addr. of data reg.

c) * $f_2 = f_1 = 60$ kHz.

* $(M)_{FC00h} = \overline{FFh} = 00h$

* If an error occurs (FE or OE or PE) during the communication between 8251A-1 and 8251A-2, the system on the right-hand side branches to label Hoops, that means enters halt state,