INTRODUCTION TO MICROCOMPUTERS FINAL EXAM

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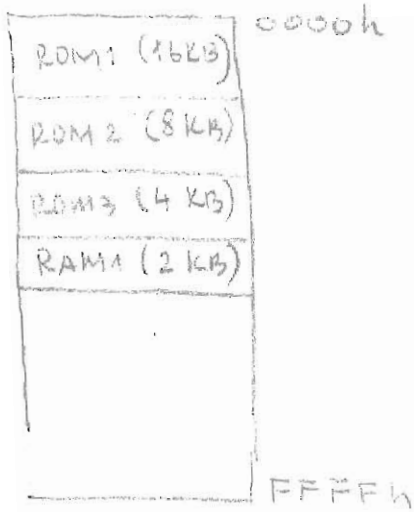
#1)



Design a completely specified decoder circuitry that uses the possible minimum capacity PROM and also places the memory ICs to the corresponding addresses shown in the figure

a) Draw the truth table of the minimum capacity PROM

b) Draw the connection diagram of the decoder circuitry. The PROM has two enable inputs. One of them is active-high and the other one is active low.

#2)

```
        ORA   0000h
        LXI   SP, DFFFFh
        LXI   H, 2000h
DNG-1:  CALL  SUB-1
        NOP
        JMP   DNG-1
        NOP
SUB-1:  NOP
LP-1:   NOP
        CALL  SUB-2
        DCR   H
        JNZ   LP-1
        RET
SUB-2:  PUSH  H
        MVI   H, 0FFh
LP-2:   NOP
AA:     DCR   H
        JNZ   LP-2
        POP   H
        RET
```

Consider the assembly program part written for an 8085 based system. The 8085 has 8 MHz crystal.

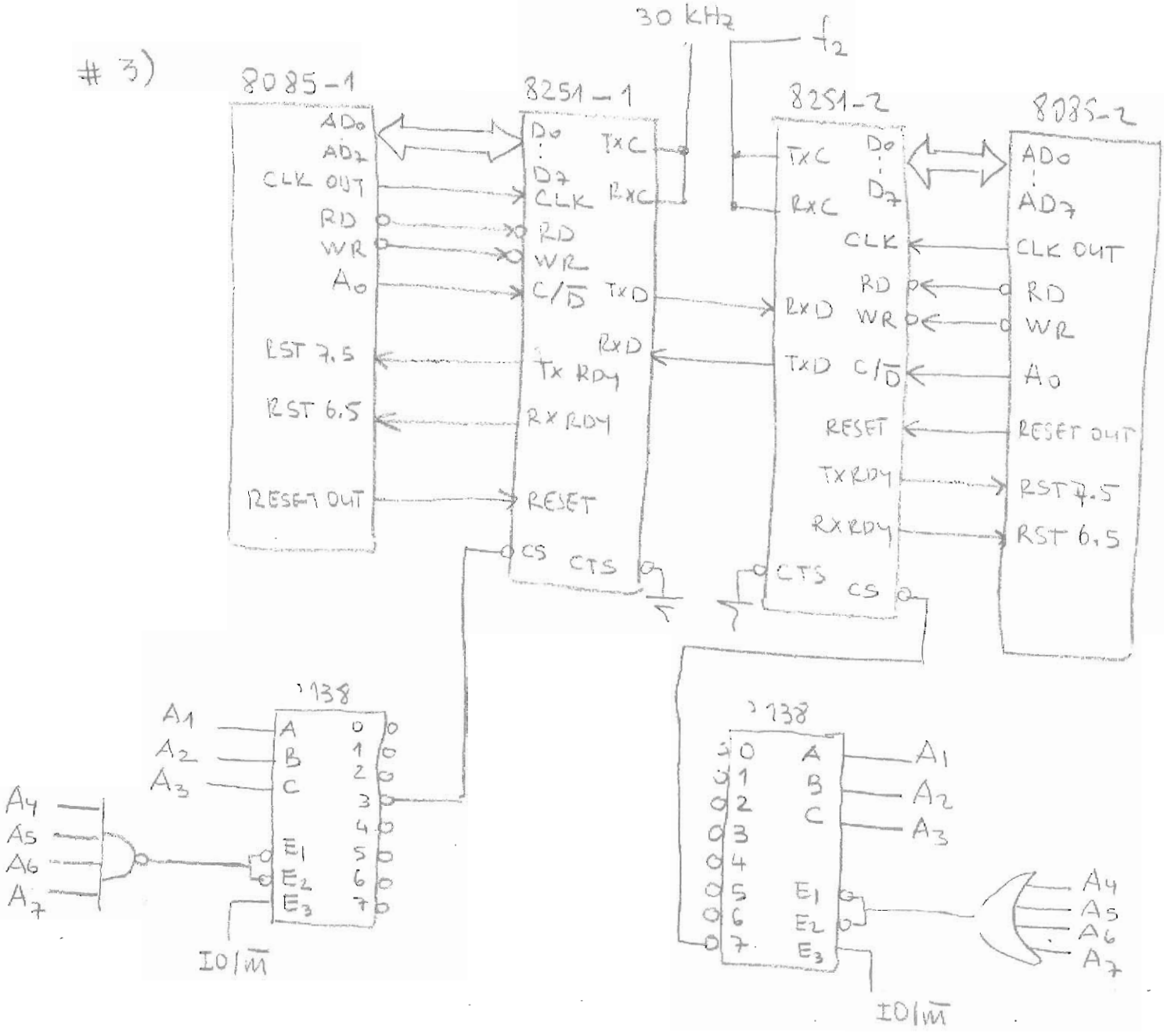
see back →

a) Calculate content of the active stack memory when the program reaches point labeled as AA in the program for the first time. Show the content of SP register in your drawing.

b) Calculate the execution time for subroutine SUB-1

c) Can the assembly program be run on the system whose memory map given in question-1? Why?

3)



USARTs shown in the figure will be used for synchronous serial communication. Consider the program parts written for 8251-1 and 8251-2 given in the following.

```
; This is for 8251-1

        ORG   0000h
        LXI   SP, 0FFFFh ; FC00h-FFFFh is for SRAM
        MVI   A, 1Ch
        Instruction-1
        MVI   A, 30h
        Instruction-2
        MVI   A, 31h
        Instruction-3
        MVI   A, 51
        Instruction-4
        MVI   A, 08h
        SIM
        EI
LOOP:   NOP
        NOP
        NOP
        JMP   LOOP

        ORG   0034h
        JMP   SUB_R
        NOP
        ORG   003Ch
        JMP   SUB_T
        NOP
SUB_R:  MVI   A, 52
        OUT   53
LP1:    IN    54
        ANI   40h
        JZ    LP1
LP2:    IN    55
        ANI   02h
        JZ    LP2
        IN    56
        ANI   57
        JNZ   SLEEP
        IN    58
        CMA
        ADI   01h
        STA   0FC00h
        NOP
        EI
        RET
SUB_T:  MVI   A, 0Fh
        OUT   59
        NOP
        EI
        RET
SLEEP:  HLT
```

See back →

```
; This is for 8251-2
        ORG     0000h
        LXI     SP, 0FFFFh ; FC00h-FFFF is for SRAM
        MVI     A, N1
        Instr-1
        MVI     A, N2
        Instr-2
        MVI     A, N3
        Instr-3
        MVI     A, N4
        Instr-4
        MVI     A,08h
        SIM
        EI
DUMMY:  NOP
        NOP
        JMP     DUMMY
        ORG     0034h
        JMP     RECEIVE
        NOP
        ORG     003Ch
        JMP     TRANSMIT
        NOP
RECEIVE: MVI    A, N5
        OUT     N6
DN61:   IN      N7
        ANI     N8
        JZ      DN61
DN62:   IN      N9
        ANI     N10
        JZ      DN62
        IN      N11
        ANI     38h
        JNZ     STUCK
        IN      N12
        CMA
        ADI     01h
        STA     0FC00h
        NOP
        EI
        RET
TRANSMIT: MVI   A, 0F0h
        OUT     N13
        EI
        RET
STUCK:  HLT
```

a) Determine Instruction-1, ... Instruction-4. Determine also S1, ... S9 in the program written for 8251-1

b) Determine Instr-1, ... Instr-4. Determine also N1, ... N13 in the program written for 8251-2

c) Determine the value of f_2. If no error occurs in the communication between two USARTs, determine the content of memory location whose address is FC00h in both system.

INTRODUCTION TO MICROCOMPUTERS FINAL EXAM SOLUTION MANUAL

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$16K = 2^{4}\,2^{10}$, $8K = 2^{3}\,2^{10}$, $4K = 2^{2}\,2^{10}$, $2K = 2^{1}\,2^{10}$

#1) a)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
16 KB ROM1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 0000h
	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 3FFFh
8 KB ROM2	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 4000h
	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= 5FFFh
4 KB ROM3	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	= 6000h
	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	= 6FFFh
2 KB RAM1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	= 7000h
	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	1	= 77FFh

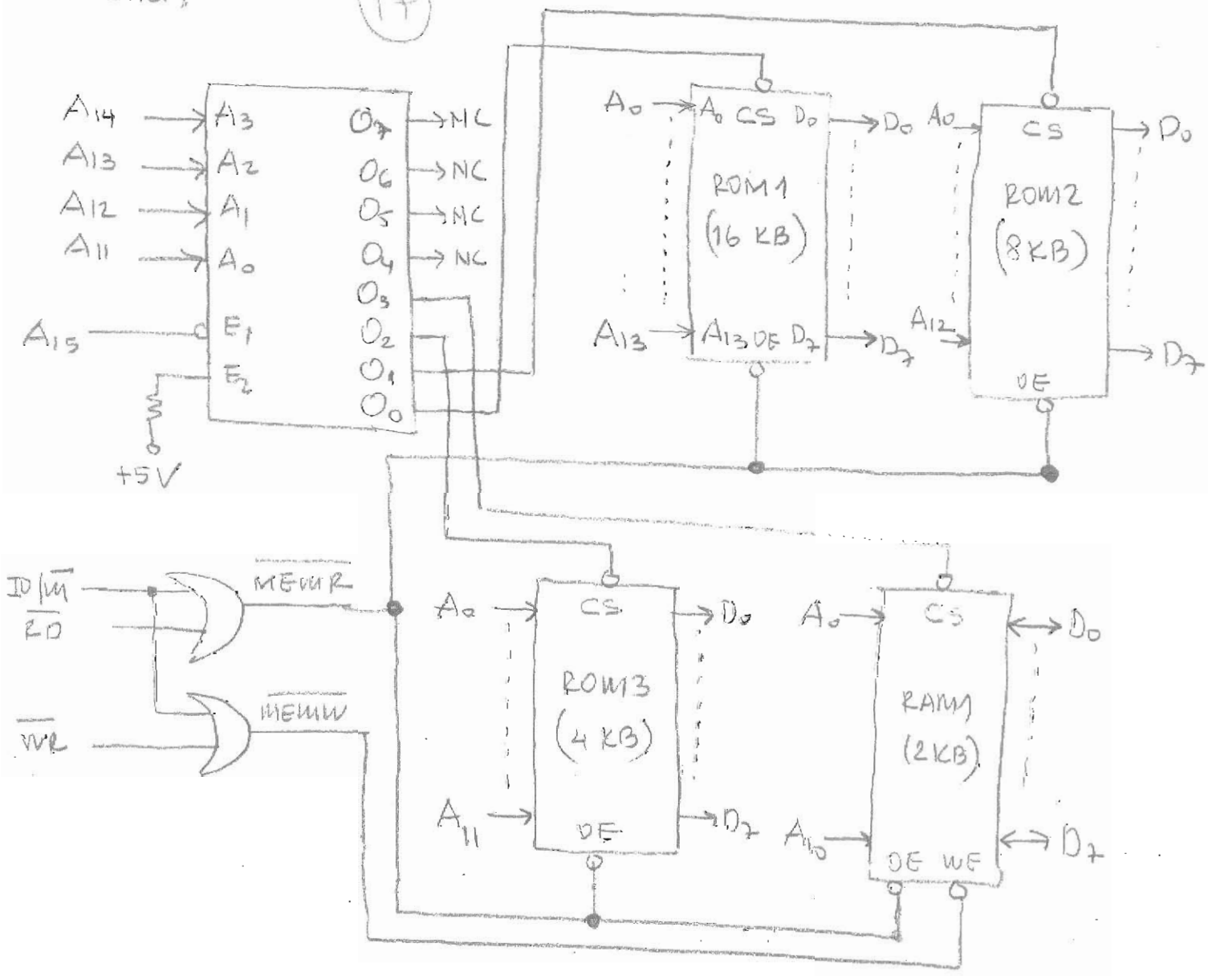
will be connected to low enable input of the PROM

To find the MINIMUM CAPACITY PROM, from the binary memory map, we see that A_{14}, A_{13}, A_{12}, A_{11} will be the inputs to the PROM. Because of this, PROM capacity will be $2^4 = 16$ Bytes. Since A_{15} remains at logic 0 in the adress range where memory ICs are located, A_{15} will be connect to low enable of the PROM.

	INPUTS				OUTPUTS							
	A_{14} A_{13} A_{12} A_{11}				N.C	N.C	N.C	N.C	$\overline{CS}_{RAM1}$	$\overline{CS}_{ROM3}$	$\overline{CS}_{ROM2}$	$\overline{CS}_{ROM1}$
	A_3 A_2 A_1 A_0				O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0
ROM1 8 loc.	0 0 0 0				1	1	1	1	1	1	1	0
	0 1 1 1				1	1	1	1	1	1	1	0
ROM2 4 loc.	1 0 0 0				1	1	1	1	1	1	0	1
	1 0 1 1				1	1	1	1	1	1	0	1
ROM3 2 loc	1 1 0 0				1	1	1	1	1	0	1	1
	1 1 0 1				1	1	1	1	1	0	1	1
RAM1 1 loc.	1 1 1 0				1	1	1	1	0	1	1	1
→ remaining 1 location	1 1 1 1				1	1	1	1	1	1	1	1

(16)

(17)



#2)

			# of T states	# of bytes	start addr
	ORG	0000h			
	LXI	SP, OFFFFh	10	3	0000h
	LXI	H, 2000h	10	3	0003h
DNG-1:	CALL	SUB_1	18	3	0006h
	NOP		4	1	0009h
	JMP	DNG_1	10/7	3	000Ah
SUB_1:	NOP		4	1	000Dh
LP_1:	NOP		4	1	000Eh
	CALL	SUB_2	18	3	000Fh
	DCR	H	4	1	0012h
	JNZ	LP_1	10/7	3	0013h
	RET		10	1	0016h
SUB_2:	PUSH	H	12	1	0017h
	MVI	H, OFFh	7	2	0018h
LP_2:	NOP		4	1	001Ah
AA:	DCR	H	4	1	001Bh
	JNZ	LP_2	10/7	3	001Ch
	POP	H	10	1	001Fh
	RET		10	1	0020h
				Σ=33	21h=33

a)

stack mem.

PUSH H	00h	FFF9h ← (SP) at point AA (first time)
	20h	FFFAh
CALL SUB_2	12h	FFFBh
	00h	FFFCh
CALL SUB_1	09h	FFFDh
	00h	FFFEh
	XX	FFFFh ← (SP)

b) # of T-states in SUB-2

$$12+7+\underbrace{(4+4+10)}_{18}\times 254+15+10+10 = 19+18\times 254+35$$
$$= 4626$$

# of T-states in SUB-1

$$4+\underbrace{(4+4626+18+4+10)}_{4662}\times 31+4659+10 = 149195$$

Execution time $= 149195 \times \frac{1}{4\ 10^{+6}} = 0{,}03729875$ s
$= 37.298$ ms

c) It can not be run, since the system given in question-1 does not have SRAM memory whose selection addresses are FFFFh or lower.

#3) a)

For 8251-1

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	0	1	1	0	= 0F6h Addr. of data reg
— " —				— " —			1	= 0F7h Addr. of control-command-status register

Mode word

7	6	5	4	3	2	1	0	
0	0	0	1	1	1	0	0	= 1Ch.
↑ double sync. char	↑ output ext. sync.	odd par.		8 data bit		sync. mode		

Instruction-1 : OUT OF7h writing mode word
Instruction-2 : OUT OF7h " SYNC1 = 30h
Instruction-3 : OUT OF7h " SYNC2 = 31h

S1 : Command word = 00010101 = 15h

Instruction-4 : OUT OF7h writing command word
S2 : Command word = 10010101 = 95h
S3 : command reg addr = OF7h
S4 : Status reg addr = OF7h
S5 : " " " = OF7h
S6 : " " " = OF7h
S7 : control mask for errors = 38h
S8 : data reg. addr = OF6h
S9 : data reg. addr = OF6h

b) For 8251-2

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	0	0	0	1	1	1	0	= OEh Addr of data reg.
— " —				— " —			1	= OFh Addr. of control — command — status reg.

N1 = mode word = 1Ch
Instr-1 : OUT OFh
N2 = Command word = 15h
Instr-2 : OUT OFh
N3 = SYNC1 = 30h
Instr-3 : OUT OFh

N4 = SYNC2 = 31h
Instr-4 : OUT OFh
N5 = Command word = 95h
N6 = Command reg. addr = OF4h
N7 = Status reg. addr = OFh

N8 = mask for checking SINDET : bit of Status register = 40h

N9 = Addr of Status reg. = OFh

N10 = mask for checking RXRDY bit of status reg. = 02h

N11 = Addr of status reg = OFh

N12 = Addr of data reg = OFh

N13 = " " " " = OEh

c) f_2 = 30 kHz

In system - ① (M) FC00h = 10h ; 2's complement of F0h = 1111 0000

In system - ② $(M)_{FC00h}$ = F1h ; 2's complement of OFh = 0000 1111

Reset → ①

f_2 → ②