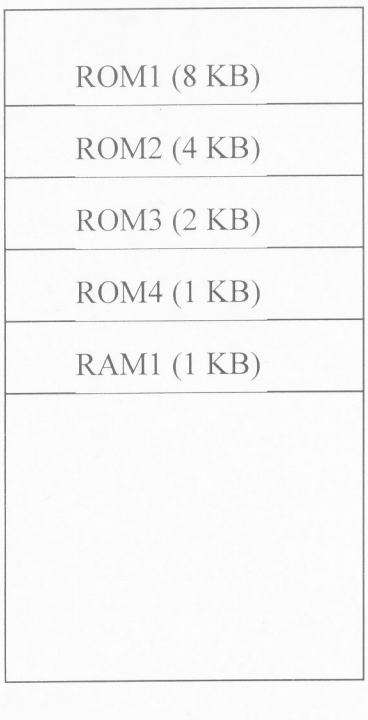
INTRODUCTION TO MICROCOMPUTERS FIRST MIDTERM EXAM

Dr. Salih FADIL **November 06, 2009**



#1) An 8085 based microprocessor system needs 15 Kbytes ROM and 1 Kbytes RAM memory. ROM and RAM memories are composed of memory ICs shown in the figure. Design a memory decoder circuitry that places the memory ICs into their respective address ranges shown in the figure. Use one '138 (3-to-8) decoder and minimum number of gates if necessary. The decoder circuitry will be a completely specified one.

#2) Realize the same decoder circuitry, which is asked in question 1, by using a PROM that has **the minimum capacity**. Show the programming of the PROM as a truth table. Draw also the circuitry of the decoder. Assume that the PROM has two enable inputs where one them is active high and the other one is active low.

#3) Consider the table where selection address ranges for each I/O device are shown. Realize the I/O decoder circuitry by using one '138 decoder and logic gates. Only data can be read from those I/O elements.

I/O Device number	Selected Address Range
0	FB00h – FB1Fh
1	FB20h – FB3Fh
2	FB40h – FB5Fh
3	FB60h – FB7Fh
4	FB80h – FB9Fh
5	FBA0h - FBBFh
6	FBC0h – FBDFh
7	FBE0h – FBFFh

INTRODUCTION TO MICROCOMPUTERS1 FIRST MIDTERM EXAM SOLUTION MANUAL

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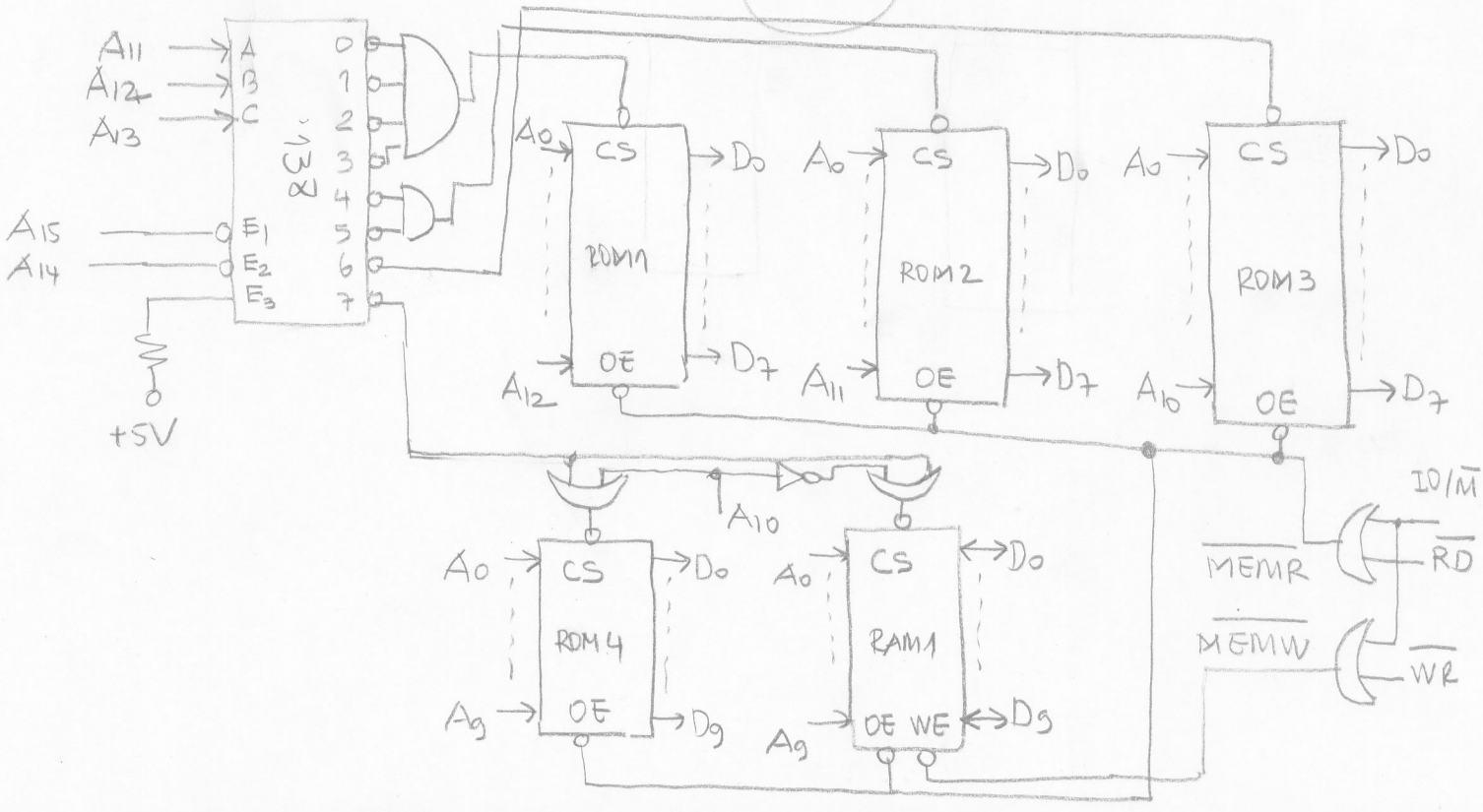
#1)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
ROM1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 0000h
	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= 1FFFh
ROM2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	= 2000h
	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	= 2FFFh
ROM3	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	= 3000h
	0	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	= 37FFh
ROM4	0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	= 3800h
	0	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	= 3BFFh
RAM1	0	0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	= 3C00h
	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 3FFFh

10

23



#2) Since A_{15} A_{14} bits remains at logic 0 in the used memory region and the minimum capacity memory IC is 1 KByte, the inputs to the PROM will be A_{13} A_{12} A_{11} A_{10}. So the minimum capacity PROM will be $2^4 = 16$ Byte. Note that A_{15} A_{14} are connected to the enables of the PROM.

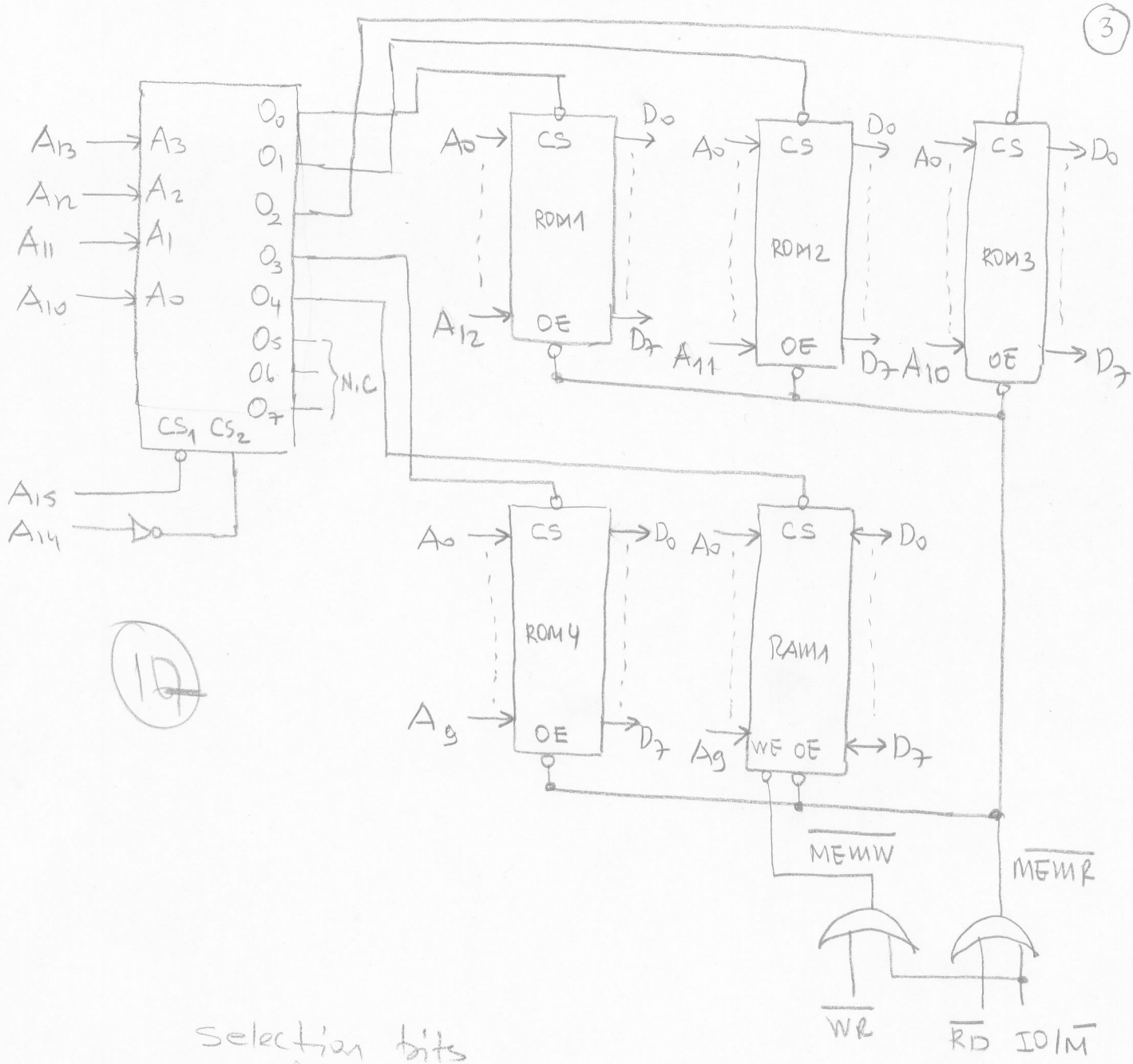
Connected Addr. bits →

INPUTS				OUTPUTS								
A_{13}	A_{12}	A_{11}	A_{10}									
A_3	A_2	A_1	A_0	O_7	O_6	O_5	O_4	O_3	O_2	O_1	O_0	
0	0	0	0	1	1	1	1	1	1	1	0	8 location (ROM1)
0	0	0	1	the same								
⋮												
0	1	1	1	1	1	1	1	1	1	1	0	
1	0	0	0	1	1	1	1	1	1	0	1	4 location (ROM2)
1	0	0	1	1	1	1	1	1	1	0	1	
1	0	1	0	1	1	1	1	1	1	0	1	
1	0	1	1	1	1	1	1	1	1	0	1	
1	1	0	0	1	1	1	1	1	0	1	1	2 location ROM3
1	1	0	1	1	1	1	1	1	0	1	1	
1	1	1	0	1	1	1	1	0	1	1	1	1 location ROM4
1	1	1	1	1	1	1	0	1	1	1	1	1 location RAM1

(17)

programming truth table of the PROM (16 Bytes)

All locations are programmed!



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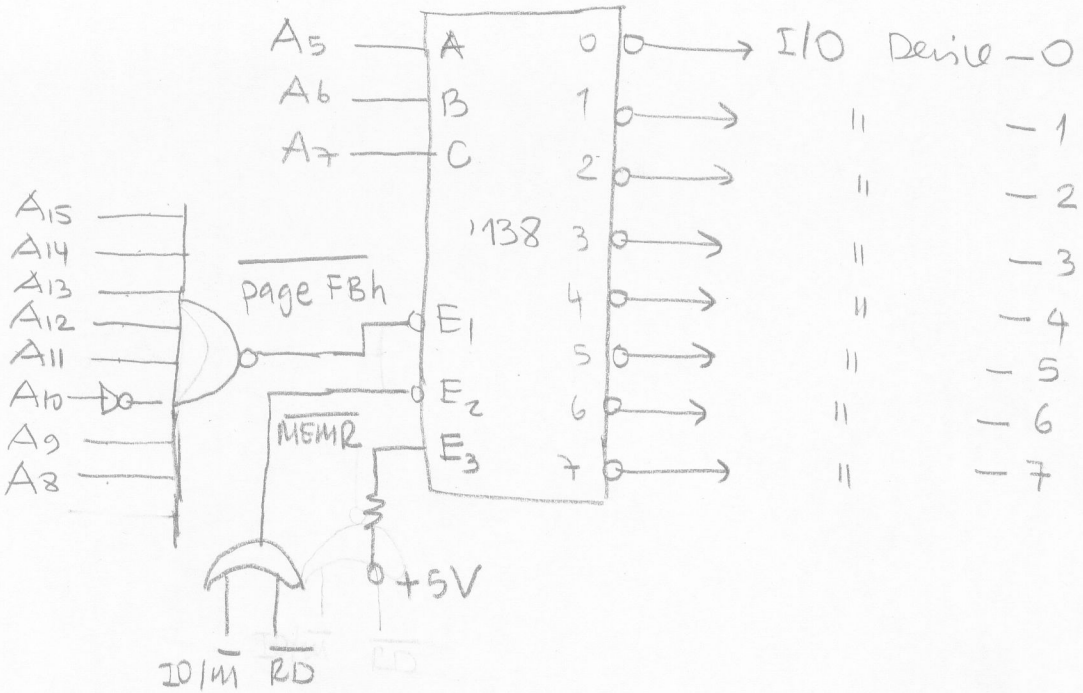
selection bits

05

#3)

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		I/O Device #
1	1	1	1	1	0	1	1	0	0	0	0	0	0	0	0	= FB00h	0
								0	0	0	1	1	1	1	1	= FB1Fh	
								0	0	1	0	0	0	0	0	= FB20h	1
								0	0	1	1	1	1	1	1	= FB3Fh	
								0	1	0	0	0	0	0	0	= FB40h	2
								0	1	0	1	1	1	1	1	= FB5Fh	
								0	1	1	0	0	0	0	0	= FB60h	3
								0	1	1	1	1	1	1	1	= FB7Fh	
								1	0	0	0	0	0	0	0	= FB80h	4
								1	0	0	1	1	1	1	1	= FB9Fh	
								1	0	1	0	0	0	0	0	= FBA0h	5
								1	0	1	1	1	1	1	1	= FBBFh	
								1	1	0	0	0	0	0	0	= FBC0h	6
								1	1	0	1	1	1	1	1	= FBDFh	
								1	1	1	0	0	0	0	0	= FBE0h	7
								1	1	1	1	1	1	1	1	= FBFFh	


A5
A6
A7
A
B
C
138
0
1
2
3
4
5
6
7
I/O Device-0
-1
-2
-3
-4
-5
-6
-7
A15
A14
A13
A12
A11
A10
A9
A8
page FBh
E1
E2
E3
MEMR
+5V
IO/M
RD

28