INTRODUCTION TO MICROCOMPUTERS FIRST EXAM
(Summer School – 2008)

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#1) The truth table of a PROM, which is used in the decoder circuitry of a 8085 based system, is given in the following

→ A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} / A_6 A_5 A_4 A_3 A_2 A_1	O_8 O_7 O_6 O_5 O_4 O_3 O_2 O_1	
0 0 0 0 0 0	1 1 1 1 1 1 1 0	
0 0 0 0 0 1	1 1 1 1 1 1 1 0	
⋮ ⋮ ⋮ ⋮ ⋮ ⋮ (same pattern)	⋮	5
0 1 1 1 1 1	1 1 1 1 1 1 1 0	
1 0 0 0 0 0	1 1 1 1 1 1 0 1	
1 0 0 0 0 1	1 1 1 1 1 1 0 1	
⋮ ⋮ ⋮ ⋮ ⋮ ⋮ (same)	⋮	4
1 0 0 1 1 1	1 1 1 1 1 1 0 1	
1 0 1 0 0 0	1 1 1 1 1 0 1 1	
1 0 1 0 0 1	1 1 1 1 1 0 1 1	
1 0 1 0 1 0	1 1 1 1 1 0 1 1	3
1 0 1 0 1 1	1 1 1 1 1 0 1 1	
1 0 1 1 0 0	1 1 1 1 0 1 1 1	
1 0 1 1 0 1	1 1 1 1 0 1 1 1	2
1 0 1 1 1 0	1 1 1 0 1 1 1 1	
The other locations	1 1 1 1 1 1 1 1	1

The used PROM has two chip selects; one of them is active-low and the other one is active-high. The lowest capacity memory chip is a RAM and the other memory chips are EPROMs.

a) Draw the complete decoder circuitry
b) Determine the capacities of each memory IC, and their selection ranges. Determine also capacity of the PROM.

SEE BACK ↘

Note that there is no overlapped addressing in the decoder circuitry.

#2) Reconsider the memory decoder circuitry described in question 1, realize the same circuitry by using only one "138 (3-to-8) decoder and logic gates if necessary.

#3)
```
        ORG   0000h
        LXI   SP, OFFFFh
        NOP
LP:     NOP
        CALL  SUB
        NOP
        NOP
        JMP   LP
        MVI   L, 00h
SUB:    MVI   H, COUNT
LP1:    NOP
        CALL  SUB1
        DCR   H
        JNZ   LP1
        RET
SUB1:   PUSH  H
        MVI   H, 0FFh
LP2:    NOP
        NOP
AA:     DCR   H
        JNZ   LP2
        POP   H
        RET
```

c) Does this assembly program work on the system given in problem 1 and 2 correctly? Why?

Consider the above assembler program which will be run on a 8085 based system

a) Draw the stack memory content together with the content of SP when the program reaches the point labeled as AA first time.

b) If the total execution time for SUB is to be 1 ms, determine the value of COUNT. Assume that cyristal frequency of the system, where the above program is run, is 6 MHz.

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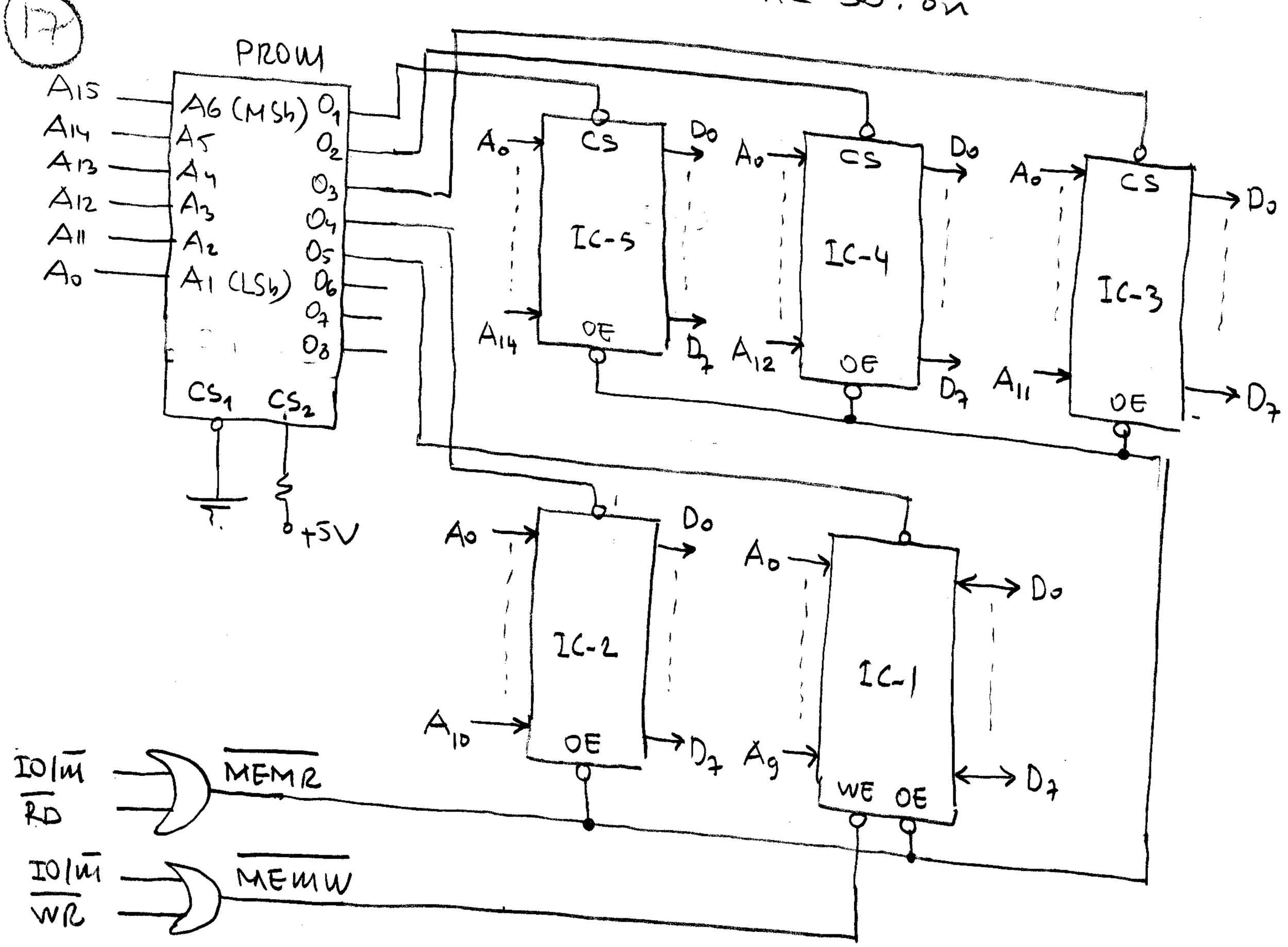
341

#1) a) Since there is no overlapped addressing in the decoder circuitry, the minimum capacity memory IC should be the one that has minimum number of location for the PROM programmed for it. Therefore, minimum capacity memory IC has 10 address inputs (1KB RAM), The second IC has 11 bit address inputs (A_{10} is input both the memory IC and PROM), so it is 2KB EPROM. The third IC has 12 bit address inputs (A_{10}, A_{11} are inputs both the memory IC and PROM), so it is 4 KB EPROM and so on.

(2)



b)

IC #	type	Capacity	Selection Range
5	EPROM	32 KByte	0000h — 7FFFh
4	EPROM	8 KByte	8000h — 9FFFh
3	EPROM	4 KByte	A000h — AFFFh
2	EPROM	2 KByte	B000h — B7FFh
1	RAM	1 KByte	B800h — BBFFh

The capacity of the PROM is $2^6 = 64$ Byte.

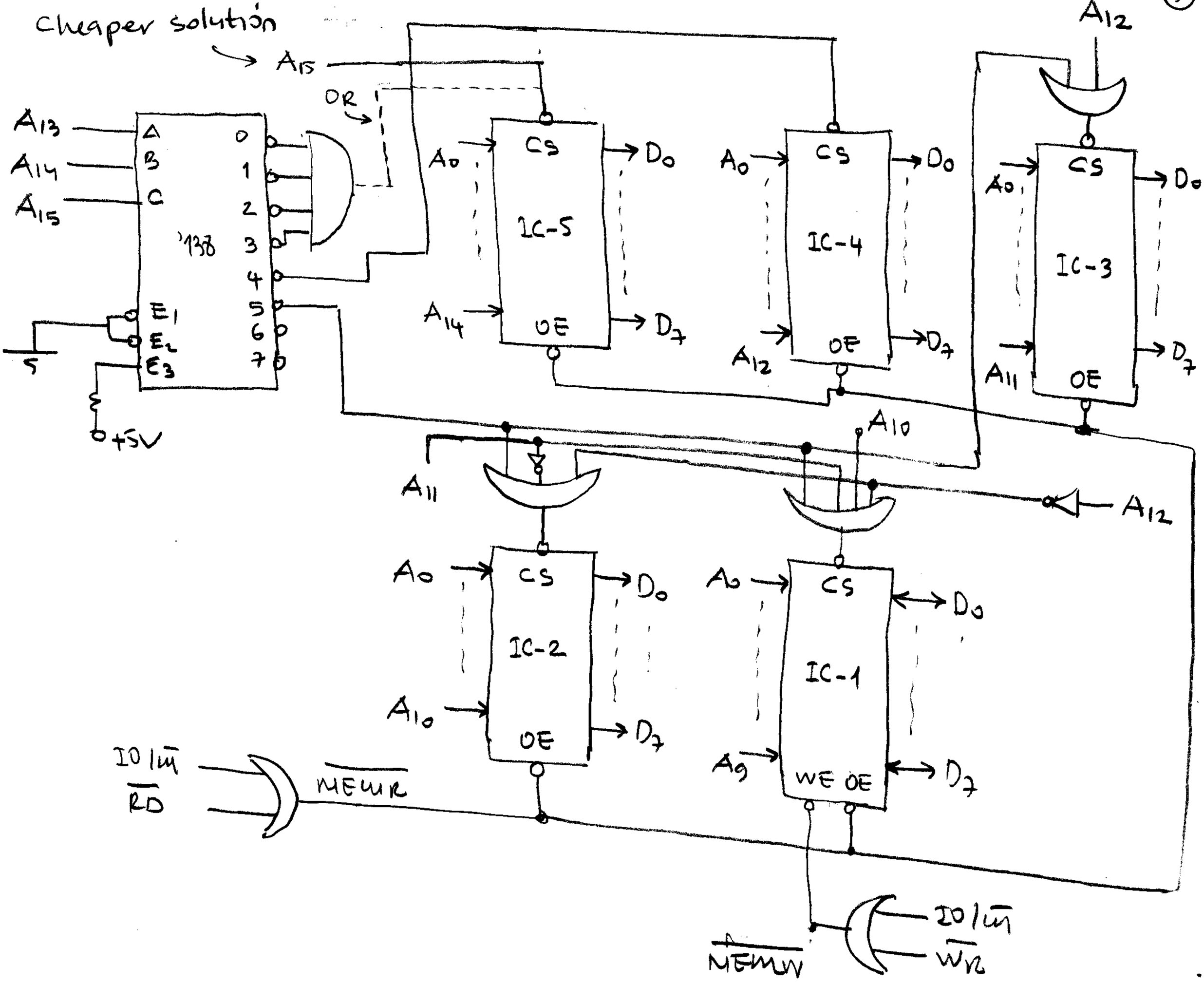
#2)

chosen chip select bits

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
32 KB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 0000h
	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 7FFFh
8 KB	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 8000h
	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= 9FFFh
4 KB	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	= A000h
	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	= AFFFh
2 KB	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	= B000h
	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	= B7FFh
1 KB	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	= B800h
	1	0	1	1	1	0	1	1	1	1	1	1	1	1	1	1	= BBFFh

IC-5 | IC-4 | IC-3 | IC-2 | IC-1

Cheaper solution



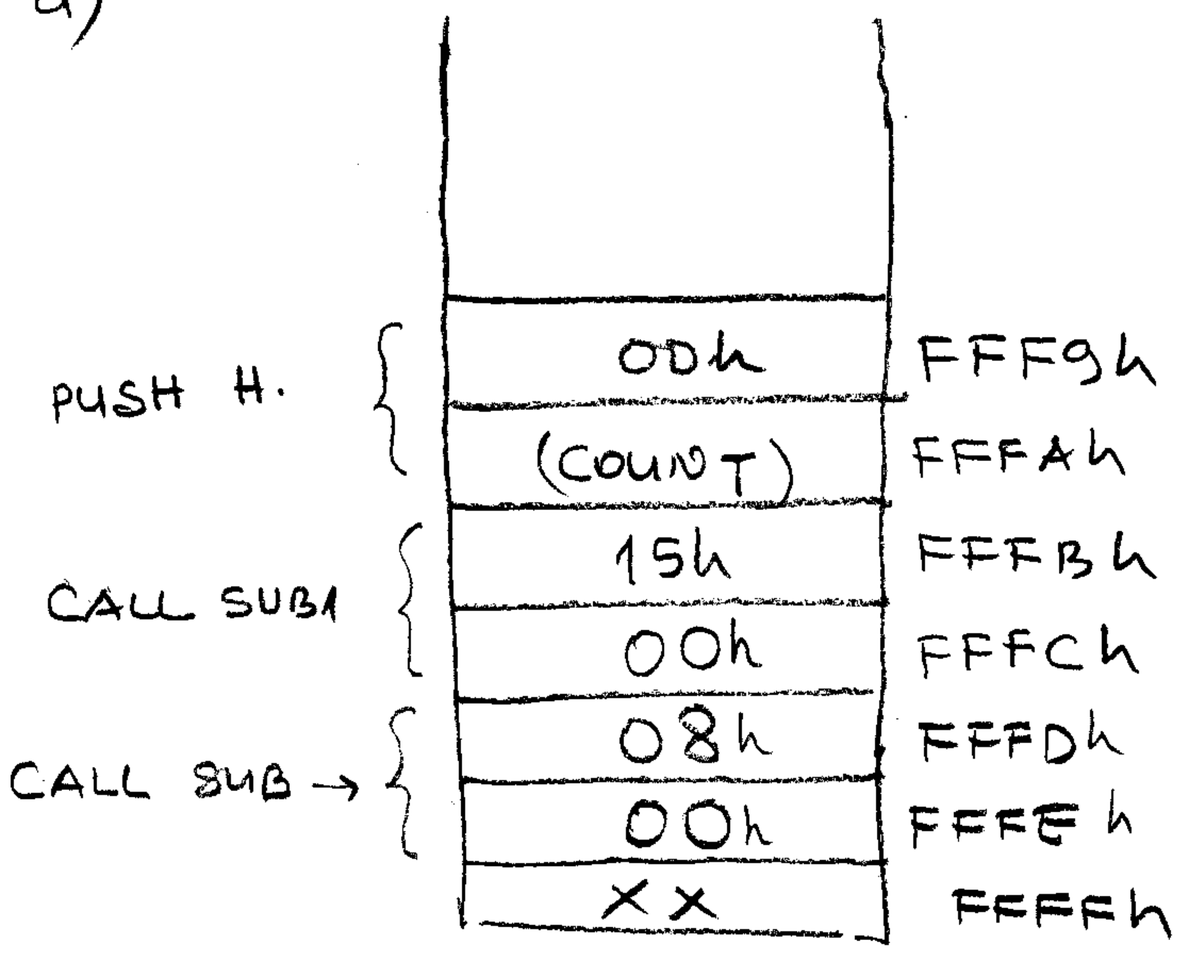
#3)

```
                                    ; # of    addr
                                    ; bytes
        ORG   0000h
        LXI   SP, OFFFFh            ; 3  ,  0000h
        NOP                         ; 1  ,  0003h
LP:     NOP                         ; 1  ,  0004h
        CALL  SUB                   ; 3  ,  0005h
        NOP                         ; 1  ,  0008h
        NOP                         ; 1  ,  0009h
        JMP   LP                    ; 3  ,  000Ah
        MVI   L,00h                 ; 2  ,  000Dh
SUB:    MVI   H, COUNT              ; 2  ;  000Fh , 7
LP1:    NOP                         ; 1  ,  0011h , 4
        CALL  SUB1                  ; 3  ,  0012h , 18
        DCR   H                     ; 1  ,  0015h , 4
        JNZ   LP1                   ,       , 10/7
        RET                         ,       , 10
```

```
SUB1:   PUSH  H                     ;       ; 12
        MVI   H, OFFh               ;       ; 7
LP2:    NOP                         ;       ; 4
        NOP                         ;       ; 4
AA:     DCR   H                     ;       ; 4
        JNZ   LP2                   ;       ; 10/7
        POP   H                     ;       ; 10
        RET                         ;       ; 10
```

↑ # of T-states

a)



b)

# of T-states in SUB1

$$12+7+(4+4+4+10)\times 254+19+10+10 = 19+22\times 254+19+2$$

$$= 5646 \longrightarrow \text{execution time} = 5646\ \frac{1}{3}\ 10^{-6} = \underline{1,882\ ms}\ !$$

# of T-states in SUB

$$7+\overbrace{(4+18+5646+10)}^{5678}(COUNT-1)+5675+10$$

$$= 5678\ (COUNT-1)+5692 = 5678\times(COUNT)-5678+5692$$

$$=(COUNT)\times 5678+14 = \frac{10^{-3}}{\frac{1}{3}\ 10^{-6}} = 3000$$

$$COUNT = \frac{3000-14}{5678} = 0,525$$

↖ It does not make sense!

Since execution's time for SUB1 is 1.882 ms > 1 ms.

$f_{cyc} = 6\ MHz$

$f_{clk} = 3\ MHz$

$T_{clk} = \frac{1}{3}\ 10^{-6}\ s.$

<u>for 100 ms</u> execution time for SUB

$$COUNT = \frac{300000-14}{5678} = 52.83 \rightarrow COUNT = 53_{10} = 35h.$$