INTRODUCTION TO MICROCOMPUTERS SECOND EXAM
(Summer School - 2008)

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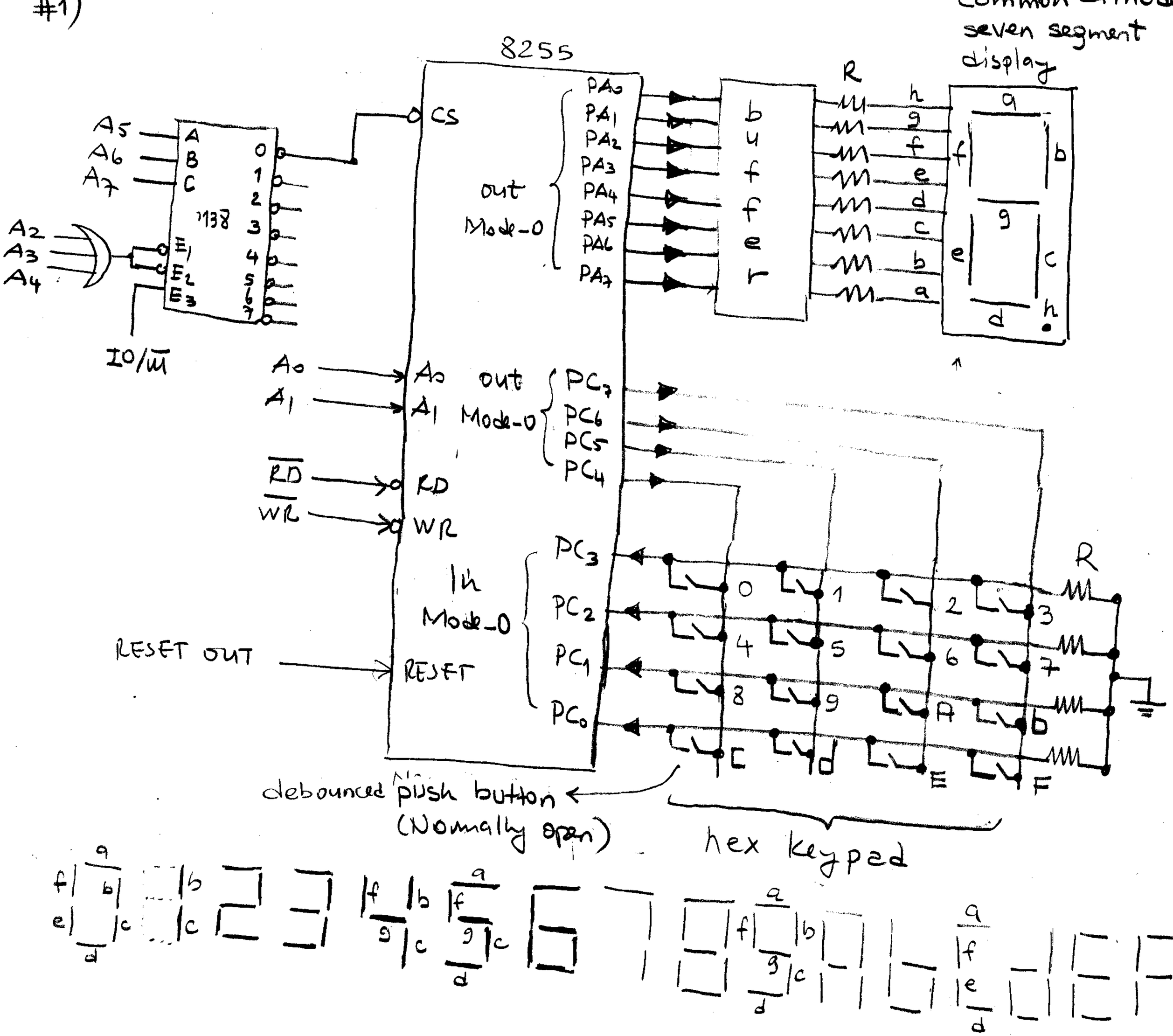
#1)



The following 8085 assembly program is written for the above system. Port B is not used.

see back

```
PORT_A   EQU   SAY-1
PORT_C   EQU   SAY-2
CONREG   EQU   SAY-3
CONWRD   EQU   SAY-4
;
         ORG   0000h
         MVI   A, CONWRD
         OUT   CONREG
BEGIN:   NOP
         NOP
         MVI   A, 00010000b
COLMN-1: OUT   PORT_C    ; First column
         IN    PORT_C
         ANI   00001000b
         JZ    FOUR
         MVI   A, 11111100b
         OUT   PORT_A
FOUR:    IN    PORT_C
         ANI   00000100b
         JZ    EIGHT
         MVI   A, 01100110b
         OUT   PORT_A
EIGHT:   IN    PORT_C
         ANI   00000010b
         JZ    TWELVE
         MVI   A, 11111110b
         OUT   PORT_A
TWELVE:  IN    PORT_C
         ANI   00000001b
         JZ    COLMN_2
         MVI   A, 10011100b
         OUT   PORT_A.
         NOP
COLMN-2: MVI   A, 00100000b
         OUT   PORT_C
         IN    PORT-C
         ANI   00001000b
         JZ    FIVE
```

```
        MVI  A, 01100000b
        OUT  PORT_A.
FIVE:   IN   PORT_C
        ANI  0000 0100b
        JZ   NINE
        MVI  A, 10110110b
        OUT  PORT_A.
NINE:   Instruction -1
        instruction -2
        instruction -3
        instruction -4
        instruction -5
THIRTEEN : ...
           ...
           .
           .
           .
           .
           .
COLMN_3 : MVI  A, 0100 0000b
          OUT  PORT_C
          IN   PORT_C
          .
          .
          .
COLMN_4 : MVI  1000 0000b
          OUT  PORT_C
          IN   PORT_C
          .
          .
          .
          .
          .
          JMP  BEGIN
```

a) Consider the program given in the above. Determine SAY-1, SAY-2, SAY-3, SAY-4. Take don't cares as zeros

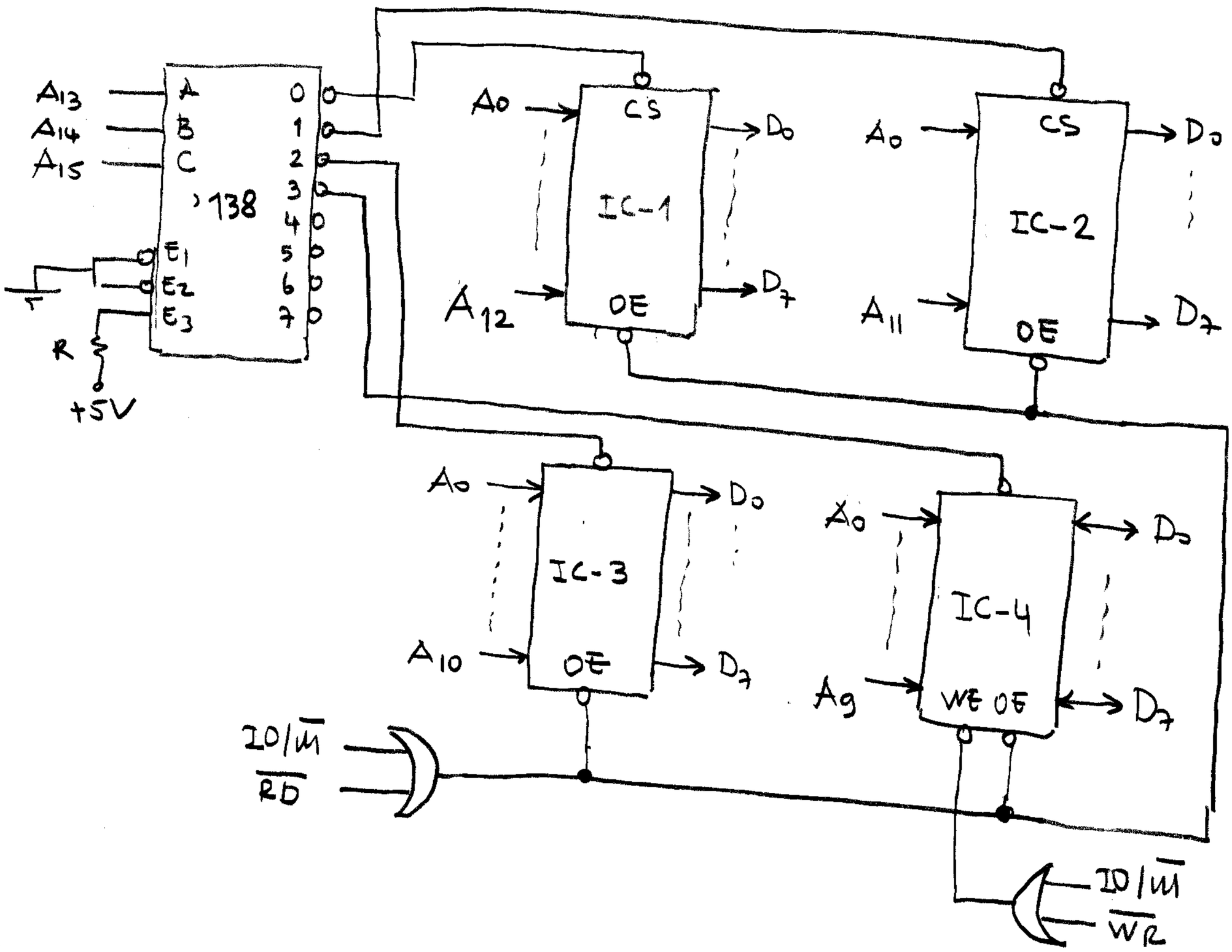
b) What does this program do? Explain shortly (<u>not line by line!</u>)

c) Determine Instruction-1, Instruction-2, Instruction-3, Instruction-4 and Instruction-5

Note that all parts starting at COLMN_i (i=1,2,3,4) looks like each other as a structure.

See back →

#2)



An incompletely specified memory decader circuitry is shown in the above figure

a) Determine each memory ICs selection address ranges

b) Determine all addresses which select the last memory place (byte) in each memory IC.

c) Determine each memory ICs type (ROM or RAM) and capacity.

#3)

```
        ORG   0000h
        LXI   SP, OFFFFh ; FC00h-FFFFh SRAM.
        LXI   H, OFC00h
        MUI   B, 0Fh.
        MUI   A, 00h
LP_1 :  MOV   M, A
        INR   A
        INX   H.
        DCR   B
        JNZ   LP_1
        NOP
        MVI   A, OFh
        SIM
        EI
LP_2:   NOP
AA:     NOP
        NOP
BB:     NOP
        NOP
CC:     NOP
        JMP   LP_2
        NOP
        ORG   0024h
        JMP   ISR-1
        NOP
        ORG   003Ch
        JMP   ISR_2
        NOP
        NOP
ISR-1:  LXI   H, OFC00h
        MVI   C, OFh
LP_3:   MOV   A, M
        CMA
        ADI   01h
        MOV   M, A.
        INX   H
        DCR   C
        JNZ   LP_3
        MUI   A, 08h
        SIM
SS:     EI
        RET
        NOP
ISR_2:  LXI   H, OFC00h
        MVI   C, OFh
LP_4:   MOV   A, M
        SUI   01h
        MOV   M, A
        INX   H
        DCR   C
        JNZ   LP_4
        EI
        RET
```

Consider the assembly program part written for an 8085 microprocessor based system. Assume that all sequence of events given each part occur just after hardware reset.

a) An RST7.5 hardware interrupt signal arrives the microprocessor at point AA. What are the contents of RAM memory places whose addresses are FC00h - FC0Fh. at point CC.

b) A TRAP hardware interrupt signal arrives the microprocessor at point AA. What are the contents of RAM memory places whose addresses are FC00h - FC0Fh. at point CC.

See back →

c) A TRAP hardware interrupt signal arrives the microprocessor at point AA. Just after that an RST7.5 hardware interrupt signal arrives at point BB. What are the content of RAM memory places whose addresses are FC00h - FC0Fh at point CC.

d) Assume that the instruction labeled as SS is removed from the program. Answer the question given in part c in this case.

GOOD LUCK.... ☺

INTRODUCTION TO MICROCOMPUTERS SECOND EXAM SOLUTION MANUAL (Summer School - 2008)

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#1) The system shown in the figure has isolated I/O decoder

a) since E_3 of 138 decoder is enabled when $IO/\overline{M} = 1$.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	0	0	0	0	0	0	= 00h	addr. of port A
						0	1	= 01h	" " port B
						1	0	= 02h	" " port C
						1	1	= 03h	" " control reg

— " —

Control word

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	0	0	0	0	x	1	= 81h
						(0)		

SAY-1 = addr. of port-A = 00h
SAY-2 = addr. of port-C = 02h
SAY-3 = addr. of control reg. = 03h
SAY-4 = control word = 81h

b) The assembly program given in this question is a basic hex keypad scan program.

* At the begining of the program, ports of 8255 are programmed in mode 0 as shown in the figure
* After that each key in each column is checked whether it is pressed or not. For example, the keys in column

one (key-0, key-4, key-8 and key-C) are checked as follows:
From port-C, $PC_7\,PC_6\,PC_5\,PC_4 = 0001$ is output. If key-0 is pressed the data read from PC_L will be $PC_3\,PC_2\,PC_1\,PC_0 = 1000$. Therefore data is read from port-C and it is ANDed with mask 00001000b. If the result is nonzero, key-0 is pressed.
↑ PC_3
In this case, seven segment code of numeral zero is output ($PA_7\,PA_6\,PA_5\,PA_4\,PA_3\,PA_2\,PA_1\,PA_0 = abcdefgh = 11111100$) from port A. Note that the seven segment display is common cathode type. If the result is zero, key-4 is checked and so on.

To check the keys in column two, $PC_7\,PC_6\,PC_5\,PC_4 = 0010$ is output. The checking mechanism is the same. When checking of keys is finished, the program returns to begining of the program.

c)
```
instruction-1 ⟶  IN    PORT_C
"      -2 ⟶  ANI   00000010b
"      -3 ⟶  JZ    THIRTEEN   ; a b c d e f g h
                                ; PA7 PA6 PA5 PA4 PA3 PA2 PA1 PA0
"      -4 ⟶  MVI   A,11110110b ; 1  1  1  1  0  1  1  0
-      -5 ⟶  OUT   PORT_A
```

In this part of the program key-9 in column-2 is checked. If it is pressed, its seven segmend code is sent to the display from port A. If it is not, the program jumps to checking of key-d (key-thirteen).

#2)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
IC-1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 0000h	①
	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= 1FFFh	
IC-2	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	= 2000h	①
	0	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	= 2FFFh	
	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	= 3000h	②
	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 3FFFh	
IC-3	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 4000h	①
	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	= 47FFh	
	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	= 4800h	②
	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= 4FFFh	
	the same			1	0												= 5000h	③
																	= 57FFh	
	the same			1	1												= 5800h	④
																	= 5FFFh	
IC-4	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	= 6000h	①
	0	1	1	0	1	1	1	1	1	1	1	1	1	1	1	1	= 63FFh	
	the same			0	0	1											= 6400h	②
				0	1	1											= 67FFh	
	the same			0	1	0											= 6800h	③
	0	1	1	0	1	1											= 6BFFh	
	the same			0	1	1											= 6C00h	④
				0	1	1											= 6FFFh	
	the same			1	0	0											= 7000h	⑤
				1	0	0											= 73FFh	
	the same			1	0	1											= 7400h	⑥
				1	0	1											= 77FFh	
	the same			1	1	0											= 7800h	⑦
				1	1	0											= 73FFh	
	the same			1	1	1											= 7C00h	⑧
				1	1	1											= 7FFFh	

a)

Memory chip	Selected address ranges
IC-1	(0000h – 1FFFh)
IC-2	(2000h – 2FFFh), (3000h – 3FFFh)
IC-3	(4000h – 47FFh), (4800h – 4FFFh), (5000h – 57FFh), (5800h – 5FFFh)
IC-4	(6000h – 63FFh), (6400h – 67FFh), (6800h – 6BFFh), (6C00h – 6FFFh), (7000h – 73FFh), (7400h – 77FFh), (7800h – 7BFFh), (7C00h – 7FFFh)

b)

Memory Chip	Addresses that select the last byte
IC-1	1FFFh
IC-2	2FFFh, 3FFFh
IC-3	47FFh, 4FFFh, 57FFh, 5FFFh
IC-4	63FFh, 67FFh, 6BFFh, 6FFFh, 73FFh, 77FFh, 7BFFh, 7FFFh

c)

Memory chip	capacity	type
IC-1	$2^{13} = 2^3\,2^{10} \longrightarrow$ 8 KB	ROM
IC-2	$2^{12} = 2^2\,2^{10} \longrightarrow$ 4 KB	ROM
IC-3	$2^{11} = 2^1\,2^{10} \longrightarrow$ 2 KB	ROM
IC-4	$2^{10} \longrightarrow$ 1 KB	RAM

#3)

a) Since at begining of the program all masks are in place and RAM locations whose addresses are between FC00h – FC0Fh are written as follows, RST 7.5 interrupt request is NOT recognized by the processor. The content of RAM locations whose addresses are FC00h - FC0Fh remain the same as shown on the left hand side

00	FC00h
01	FC01h
02	FC02h
03	FC03h
04	FC04h
05	FC05h
06	FC06h
07	FC07h
08	FC08h
09	FC09h
0A	FC0Ah
0B	FC0Bh
0C	FC0Ch
0D	FC0Dh
0E	FC0Eh
0F	FC0Fh

← Figure-1

b) Since TRAP is NMI, the microprocessor writes the address of NOP just after AA into stack and jumps to 0024h (interrupt vector address of TRAP). From there it jumps to ISR-1. In ISR_1, memory contents in FC00h – FC0Fh are changed with their two's complement and become as follows.

00	FC00h
FF	FC01h
FE	FC02h
FD	FC03h
FC	FC04h
FB	FC05h
FA	FC06h
F9	FC07h
F8	FC08h
F7	FC09h
F6	FC0Ah
F5	FC0Bh
F4	FC0Ch
F3	FC0Dh
F2	FC0Eh
F1	FC0Fh

← Figure-2

number		2's comp.
0000 0000	→	0000 0000h = 00h
0000 0001	→	1111 1111 = FFh
0000 0010	→	1111 1110 = FEh
0000 0011	→	1111 1101 = FDh
0000 0100	→	1111 1100 = FCh
0000 0101	→	1111 1011 = FBh

0000 1111 → 1111 0001

Toward at the end of ISR-1, all masks are removed, interrupt i's enzbled and returned to NOP instruction just after AA. As a result content of RAM memory between FC00h - FC0Fh will be as shown in the above at point CC.

c) In this case, the microprocessor will write the address of NOP just after label AA into stack and jump to 0024h, from there it will jump to ISR-1. After that it will return to NOP instruction. The content of the RAM locations in FC00h - FC0Fh will be as shown in Figure-2. Since all masks are removed at this point, when an RST7.5 interrupt request arrives the microprocessor at BB, it jumps to 003Ch, from there it jumps to ISR-2. Inside ISR-2, the content of each location is decremented by one, and becomes as follows.

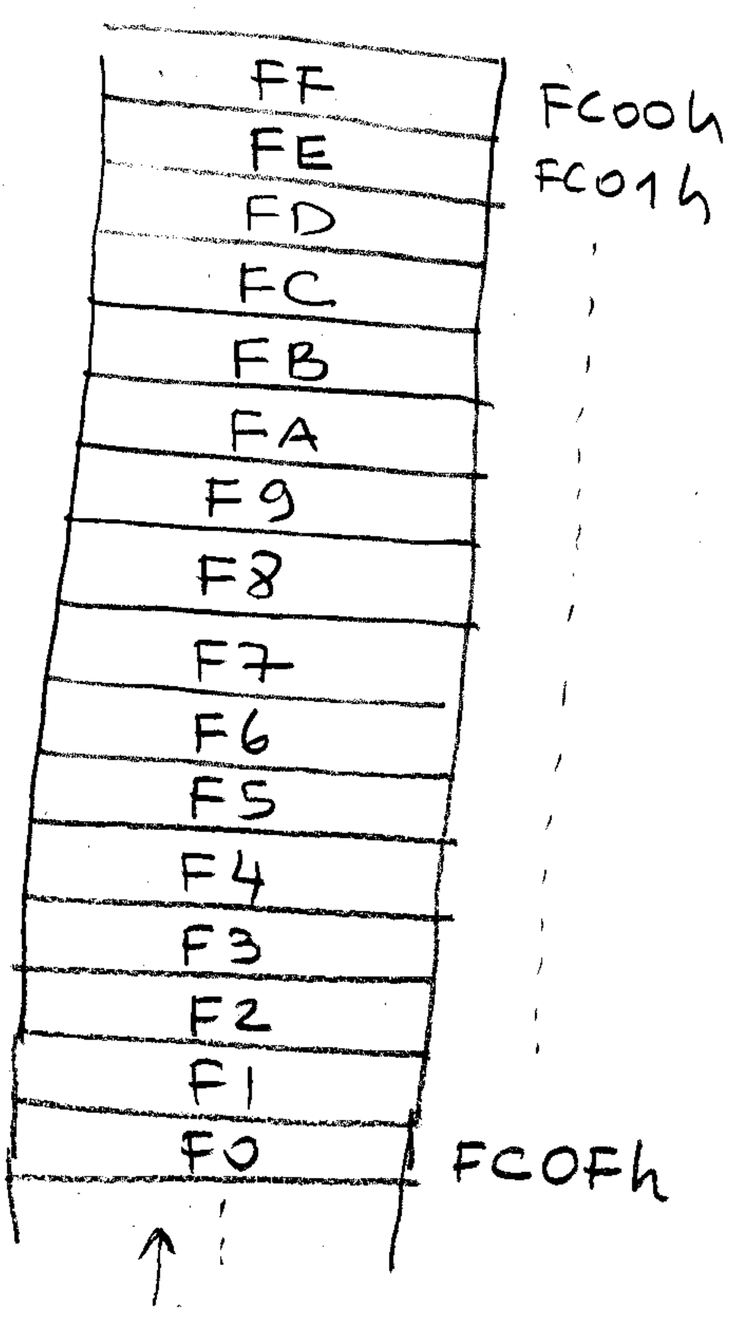

Figure-3

So, the content of RAM locations will be as shown in Figure-3 at point CC.

d) After recognition of an interrupt request, interrupt enzble S-R flip-flop is reset (interrupt is disabled). Since, interrupt is NOT enzbled before leaving the TRAP's ISR (ISR-1), RST7.5 interrupt request will not be recognized by the microprocessor. Therefore the contents of the RAM locations in FC00h - FC0Fh will be as shown in Figure-2 at point CC.