INTRODUCTION TO MICROCOMPUTERS FINAL EXAM

(Summer School - 2008)

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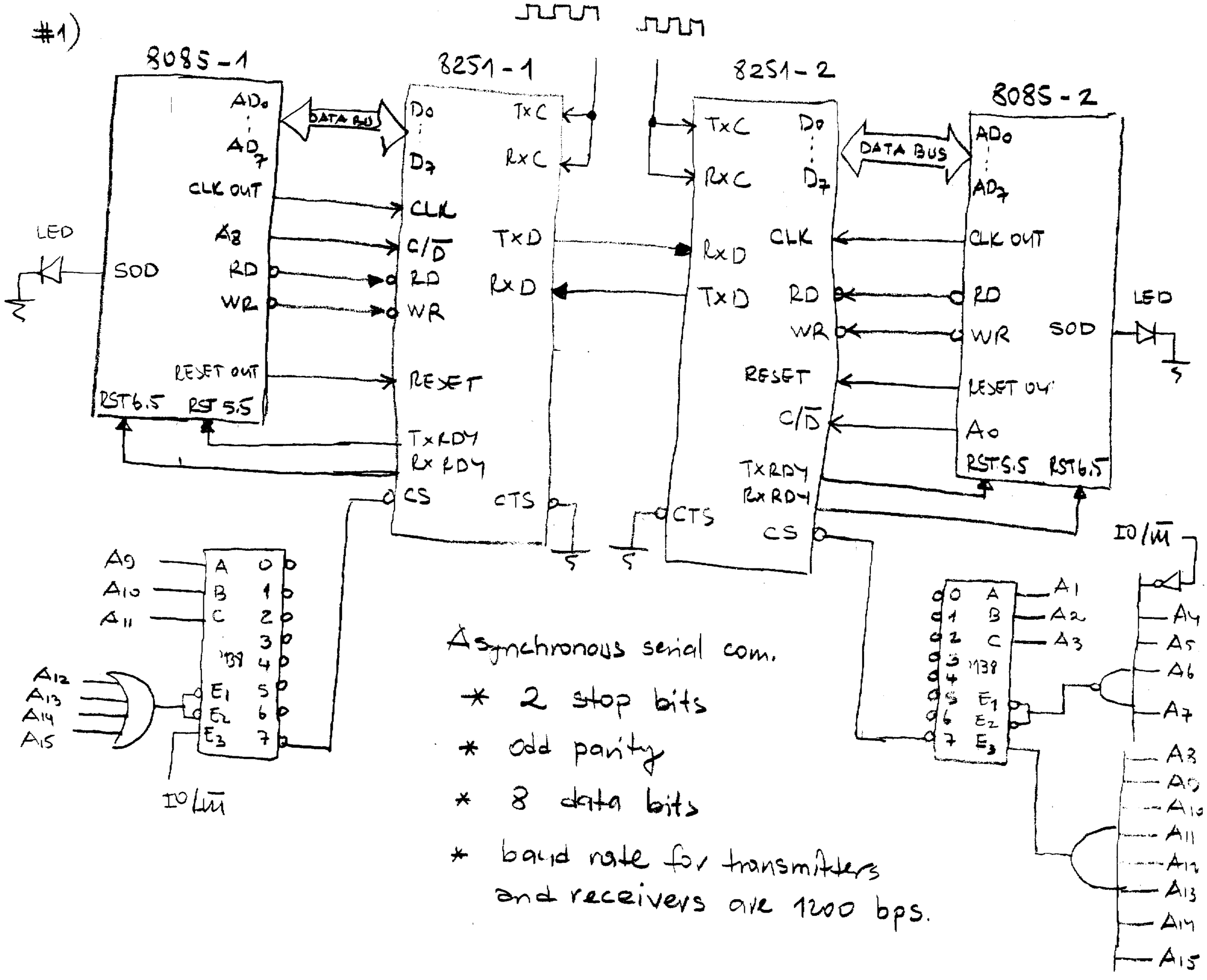
August 21, 2008

#1)



Asynchronous serial com.

* 2 stop bits
* odd parity
* 8 data bits
* baud rate for transmitters and receivers are 1200 bps.

Consider the assembly program parts written for the above system.

see back →

```
        ; It is written for 8251-1

        ORG  0000h
AA:     LXI  SP, 8000h ; 7C00h-7FFFh is SRAM
        MVI  A, N1
        Instruction-1
        MVI  A, N2
        Instruction-2
        NOP
        NOP
        ORG  002Ch
        JMP  KIRAZ
        NOP
        NOP
        ORG  0034h
        JMP  ERIK
        NOP
        NOP
        MVI  A  01001110b
        SIM
        EI
LOOP:   NOP
        NOP
        NOP
        JMP  LOOP
        NOP
        NOP
KIRAZ:  MVI  A, OFF
        OUT  N3
        MVI  A, 00001100b
        EI
        RET
        NOP
        NOP
ERIK:   IN   N4:
        ANI  38h
        JNZ  AYVA
        IN   N5
        ADI  01h
        STA  7C00h  ; ??

        NOP
        NOP
AYVA:   MVI  A, 11000000b
        SIM
        HLT
```

```
; It is written for 8251-2
ORG 0000h
LXI SP, 8000h ; 7c00h-7FFFh is SRAM.
MVI A, S1
Instruction-1
MVI A, S2
Instruction-2

NOP
NOP
ORG 002Ch
JMP ELMA
NOP
NOP
ORG 0034h
JMP ARMUT
NOP
NOP
MUI A, 01001101
SIM
EI
LP: NOP
    NOP
    NOP
    JMP LP
    NOP
    NOP
ARMUT: LDA S3
    ANI 00110000b
    JNZ VISNE
    LDA S4
    ADI 01h
    STA 7C00h. ;??
    NOP
    MVI A, 00001100b
    SIM.
    EI
    RET

    NOP
    NOP
ELMA: MUI A, 11h
    STA S5
    EI
    RET
VISNE: MUI A, 11000000b
    SIM
    HLT
```

a) Consider the program part written for 8251-1 and determine values for N1, N2, N3, N4, N5 and determine also Instruction-1, Instruction-2.

b) Consider the program part written for 8251-2 and determine values for S1, S2 S3, S4, S5 and determine also Instruction-1, Instruction-2

c) Determine the content of the first SRAM location in both system.

d) If a parity error occurs during the communication what happens in both system, explain shortly.

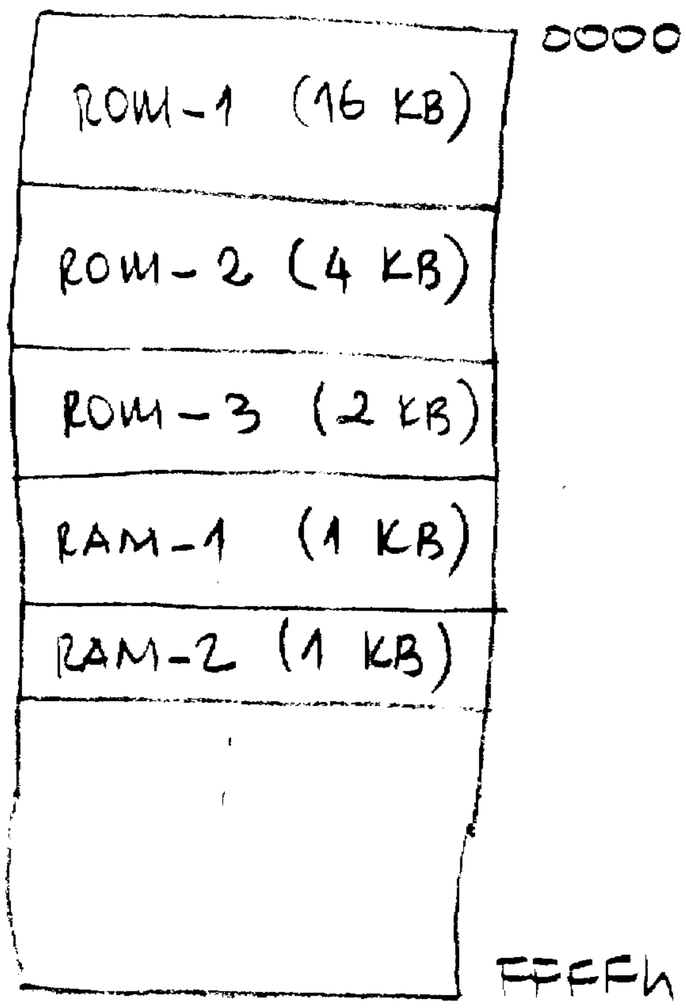
e) In the program part written for 8251-1, if the instruction labeled as AA is changed as LXI SP, 0FC02h, what happens explain?

↘ see back

f) What do those programs do? Explain shortly. (4)

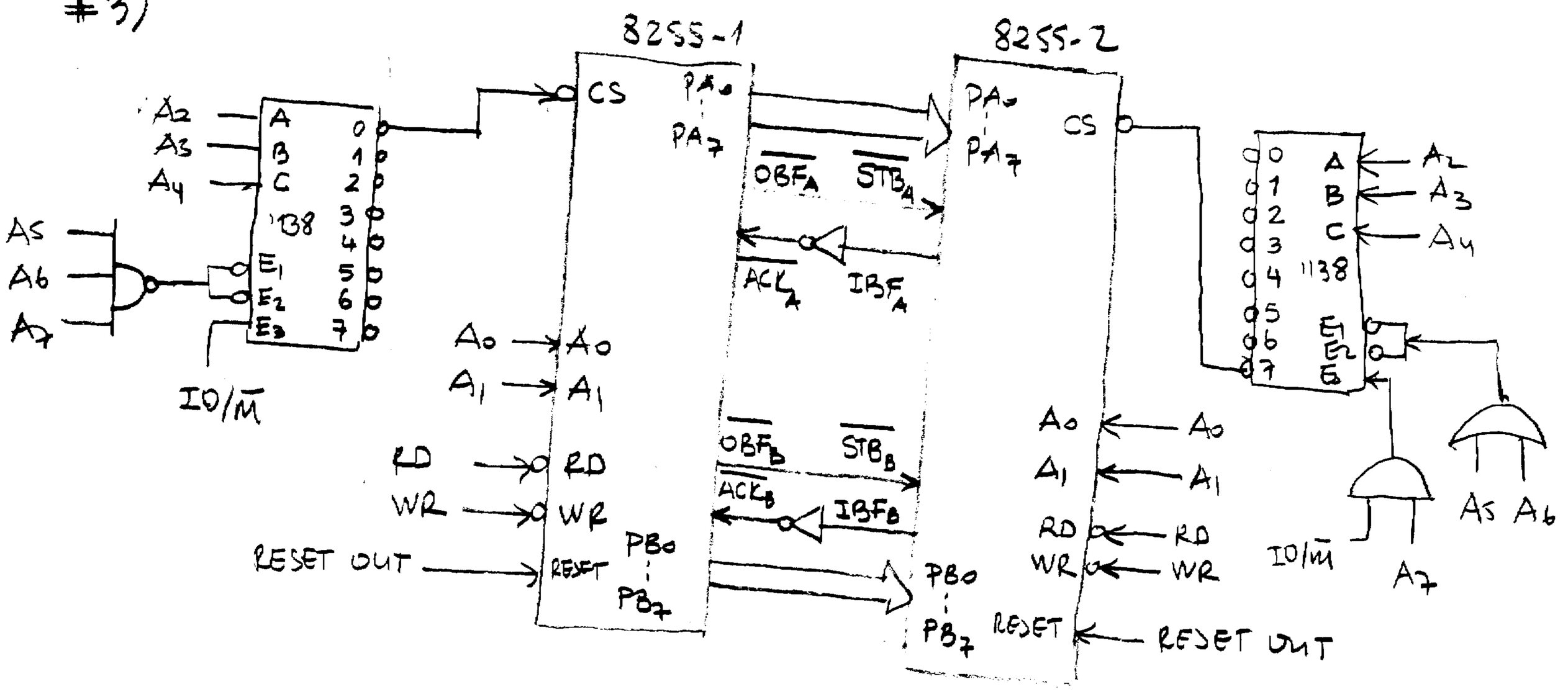
#2)

Memory map



In a 8085 based microprocessor system, 22 KByte ROM, 2 KByte RAM memory is needed. Locations of memory ICs are shown in the memory map shown in the figure. Design a memory decoder circuitry placing the memory ICs into the address ranges shown in the figure. Use a <u>minimum capacity PROM</u> in your design. There is going to be no overlapping addresses in your design. Draw the truth table of the PROM and complete decoder circuitry. Assume that PROM has two chip select inputs, one of them is active high, the another one is active low.

#3)



Consider the system shown in the above. The following assembly programs are written for 8255-1 and 8255-2.

```
; It is written for 8255-1

ORG   0000h
LXI   SP, 0FFFFh ; FC00h-FFFFh SRAM.
MVI   A, SA41
Instruction_1
NOP
NOP
SALIH: IN   SA42
       ANI  80h
       JZ   LABEL1
       MVI  A, 0AAh
       OUT  SA43
       IN   SA44
       ANI  02h
       JZ   LABEL2
       MUI  A, 0BBh
       OUT  SA45
       JMP  SALIH
       NOP
       NOP
       NOP

; It is written for 8255-2
ORG   0000h
LXI   SP, 0FFFFh ; FC00h- FFFFh SRAM
      MVI  A, NUM1
      Instruction_2
      NOP
      NOP
FADIL; IN   NUM2
      ANI  00100000
      JZ   ETKT1
      IN   NUM3
      STA  0FC00h
      NOP
      NOP
      IN   NUM4
      ANI  00000010
      JZ   ETKT2
      IN   NUM5
      MOV  B, A.
      LDA  0FC00h
      ADD  B
      STA  0FC00h
      JMP  FADIL
```

see back

a) Consider the program part written for 8255-1 and determine the values for SAY1, SAY2, SAY3, SAY4, SAY5. Determine also Instruction-1, LABEL1 and LABEL2. For LABEL1 and LABEL2, write the label and then the instruction.

b) Consider the program part written for 8255-2 and determine NUM1, NUM2, NUM3, NUM4, NUM5. Determine also Instruction-2, ETKT1, ETKT2. For ETKT1 and ETKT2, write the label and then the instruction.

c) What is the content of RAM location, whose address is FC00h, of the system on the right hand side.

d) What does this system do? Explain shortly.

Note! Take don't cares as zero in all problems!

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SOLUTION MANUAL (Summer School - 2008)

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#1) For 8251-1

a)

* It has isolated I/O decoder since $E_3 = 1$ for $IO/\overline{M} = 1$

(7)

A_{15} A_{14} A_{13} A_{12} A_{11} A_{10} A_9	A_8	
0 0 0 0 1 1 1	0	= 0Eh → Data reg. addr.
—11—	1	= 0Fh → Control - command - status reg. addr.

Mode word

D_7 D_6	D_5 D_4	D_3 D_2	D_1 D_0	
1 1	0 1	1 1	1 0	= DEh
2 stop bits	odd parity	8 data bits	16x	

$\frac{19200}{1200} = 16$

Command word

D_7 D_6	D_5 D_4	D_3 D_2	D_1 D_0	
0 0	0 1	0 1	0 1	= 15h
reset error bits	↑	Enable receiver	Enable transmitter	

From examination of the program part written for 8251-A we can write the followings

N1 = Mode word = 0DEh

Instruction-1 ⇒ OUT 0Fh

N2 = Command word = 15h

Instruction-2 ⇒ OUT 0Fh

For 8251-1

TxRDY ⟶ RST 5.5 ISR for RST 5.5 should include transmit routine
RxRDY ⟶ RST 6.5 ISR for RST 6.5 " " receive "

Vector addr. for RST 5.5 → 002Ch ⇒ KIRAT ISR ⇒ trans. routine
" " " RST 6.5 → 0034h ⇒ ERIK ISR ⇒ Receive ".

N3 = Addr. of data reg. = 0Eh
N4 = Addr of status reg = 0Fh
N5 = Addr of data reg = 0Eh

b) 8251-2 has memory mapped I/O decoder since $\overline{E}_2 = \overline{E}_1 = 0$ for $IO/\overline{M} = 0$.

A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	= FFFEh
															1	= FFFFh

— 11 —

FFFFh : Addr. of Control- Command- Status reg.
FFFEh : Addr of Data reg.

Mode and command words will be the same.

Mode word = DEh
Command word = 15h

S1 = Mode word = 0DEh
Instruction-1 ⇒ STA 0FFFFh
S2 = Command word = 15h ✓
Instruction-2 ⇒ STA 0FFFFh ✓

Again for 8251-2

TxRDY → RST 5.5 → 002Ch → ELMA ISR → transmit routine
RxRDY → RST 6.5 → 0034h → ARMUT ISR → receive routine.

S3 = Addr. of Status reg = OFFFFh ✓

S4 = Addr. of Data reg = OFFEh ✓

S5 = Addr of Data reg = OFFEh ✓

c) In the program part written for 8251-1, mask of RST5.5 (transmission) is removed first. For 8251-2, mask of RST6.5 (reception) is removed first.

In KIRAZ ISR (RST5.5), 8251-1 sends FFh to 8251-2 and removes RST6.5's mask also.

In ARMUT ISR (RST6.5), 8251-2 checks if there is any transmission error. If there is any transmission error (FE or PE or OE) is jumps to VISNE subroutine and makes the LED connected to SOD pin on and the microprocessor enters halt mode. If there is no transmission error, it receives the data (FFh) and increment it (00h) finally stores it at memory location 7C00h. So (M) = 00h. Before leaving the ISR, mask of RST5.5 is also removed

In ISR EIZIK of 8251-1, the similar things are done. So, $(M)_{7C00h} = 12h$. As a result

8085-1 → $(M)_{7C00h} = 12h$

8085-2 → $(M)_{7C00h} \equiv 00h$ (5)

d) If the parity error (or any type of error) occurs in reception, the systems make the LED, which are connected to SOD pins of 8085's, on and enter halt state. (5)

e) In the program part written for 8251-1, if the instruction LXI SP, 8000h is changed with LXI SP, OFC02h, the program crushes since interrupt structure uses stack memory, and there is no any RAM memory in the addr region FC00h – FFFFh. (5)

f) The structure of both program parts written for 8251-1 and 8251-2 are the same.

* At the beging mode and control words are written to control and command registers.
* After that transmission (in 8251-1) and reception (in 8251-2) are enabled by removing respective masks.
* In the system, 8251-1 sends FFh to 8251-2, and 8251-2 receives this data, increments it (00h) and stores it in RAM location of 7C00h . Similarly, 8251-2 sends 11h to 8251-1 and 8251-1 receives the data and increments it (12h) and store it in RAM location 7C00h ..
* If there is an error in reception, both system make the LED connected to 800 pin on and enter halt states.

(5)

$16K = 2^4 \cdot 2^{10}$ $\quad 2K \rightarrow 2^1 \cdot 2^{10}$.

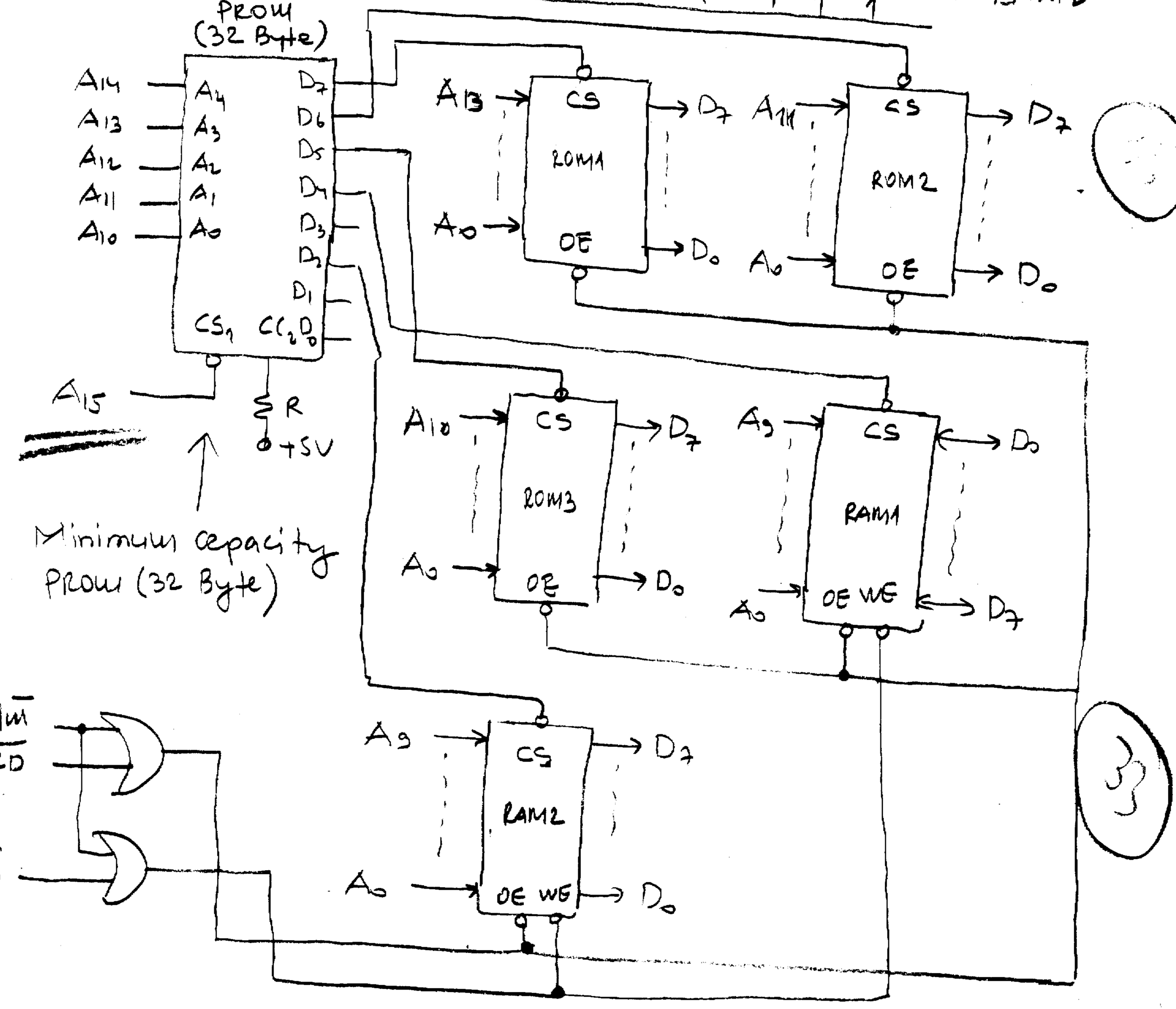
$4K = 2^2 \cdot 2^{10}$ $\quad 1K \rightarrow 2^{10}$

#2)

	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
ROM1 16 KB	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 0000h
	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 3FFFh
ROM2 4 KB	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 4000h
	0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	= 4FFFh
ROM3 2 KB	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	= 5000h
	0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	= 57FFh
RAM1 1 KB	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	= 5800h
	0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	= 5BFFh
RAM2 1 KB	0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	= 5C00h
	0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= 5FFFh

Remains the same! → they should be used to select ICs

Connected Addr lines →	INPUTS A_{14} A_{13} A_{12} A_{11} A_{10}					OUTPUT D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0								
	A_4	A_3	A_2	A_1	A_0									
	0	0	0	0	0	0	1	1	1	1	1	1	1	16 locations for ROM1.
	0	1	0	0	0	0	1	1	1	1	1	1	1	
			⋮			⋮	⋮				⋮			
	0	1	1	1	1	0	1	1	1	1	1	1	1	
	1	0	0	0	0	1	0	1	1	1	1	1	1	4 locations for ROM2
	1	0	0	0	1	1	0	1	1	1	1	1	1	
	1	0	0	1	0	1	0	1	1	1	1	1	1	
	1	0	0	1	1	1	0	1	1	1	1	1	1	
	1	0	1	0	0	1	1	0	1	1	1	1	1	2 locations for ROM3
	1	0	1	0	1	1	1	0	1	1	1	1	1	
	1	0	1	1	0	1	1	1	0	1	1	1	1	1 location for RAM1
	1	0	1	1	1	1	1	1	1	0	1	1	1	1 location for RAM2
OTHER LOCATIONS						1	1	1	1	1	1	1	1	



#3) For 8255-1 (3)

a)

* It has Isolated I/O decoder since $E_3 = 1$ for $IO/\overline{M} = 1$

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	1	1	0	0	0	0	0	= E0h → Addr. of port_A
			‖			0	1	= E1h → ‖ ‖ port-B
						1	0	= E2h → ‖ ‖ port-C
						1	1	= E3h → ‖ ‖ control-reg.

Control word

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	1	0	x (0)	1	0	x (0)	= A4h.

SA11 = Control word = 0A4h

Instruction-1 → OUT 0E3h

SA12 = Addr. of status reg. = 0E2h

SA13 = Addr. of port-A = 0E0h

SA14 = Addr of status reg = 0E2h

SA15 = Addr. of port-B = 0E1h.

$\overline{OBF_A}$ ↓

ANI 80h ; 1000 0000

LABEL1 = SA11H. $\overline{OBF_B}$ ↓

ANI 02h ; 0000 0010

LABEL2: IN SA14

b) For 8255-2

* It has Isolated I/O decoder since $E_3 = 1$ for $IO/\overline{M} = 1$, $A_7 = 1$.

A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0	
1	0	0	1	1	1	0	0	= 9Ch → Addr. of port_A
		-11-				0	1	= 9Dh → ‖ ‖ port-B
						1	0	= 9Eh → ‖ ‖ port-C
						1	1	= 9Fh → ‖ ‖ control-reg.

Control word

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
1	0	1	1	x (0)	1	1	x (0)	= B6h

NUM1 = Control word = 0B6h

Intruction-2 ⇒ OUT 9Fh

NUM2 = Addr. of Status reg = 9Eh

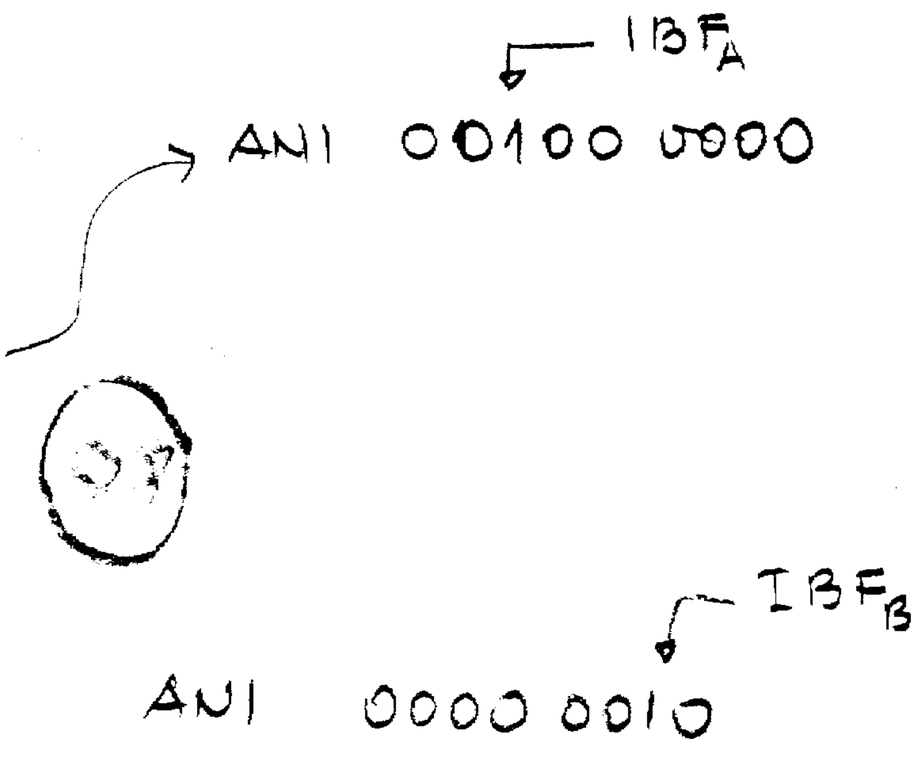
ETIKT1 = FADIL

NUM3 = Addr. of port-A = 9Ch

NUM4 = Addr. of status reg = 9Eh

ETIKT2 : IN NUM4

NUM5 = Addr. of port-B = 9Dh



c)
$$\begin{array}{r} AAh \\ +\ BBh \\ \hline 165h \end{array}$$
↑ carry

(8)

$(M)_{FC00h} = 65h$

see the explanation given in part d.

(9)

d) 8085 system on the left sends AAh through port A and BBh through port B to the 8085 system on the right in mode-1. 8085 system on the right gets AAh through its port A and BBh through its port B and it adds them. Consequently the result is written into RAM location with FC00h address.