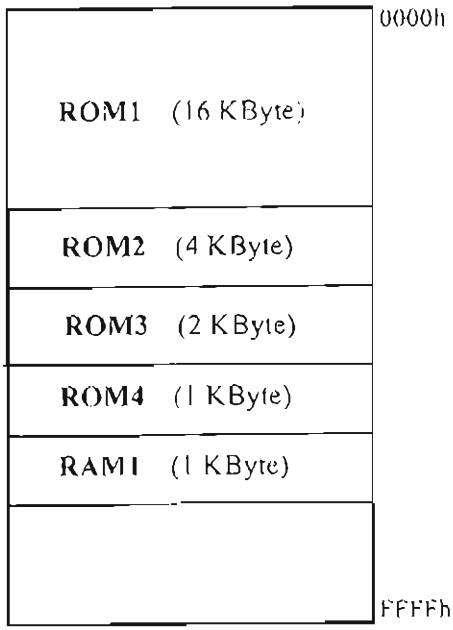
INTRODUCTION TO MICROCOMPUTERS FIRST EXAM

[redacted]

Dr. Salih FADIL November 03 2010

#1) In a 8085 microprocessor based system 23 KByte ROM, 1 KByte RAM memory is needed. Lolcation of the memory ICs is shown in the figure. Design a memory decoder circuitry placing the memoiry ICS into the address ranges shown in the figure. Use only one '138 (3-to-8 decoder) and logic gates if necessary. There will be no overlapping addresses in your design.

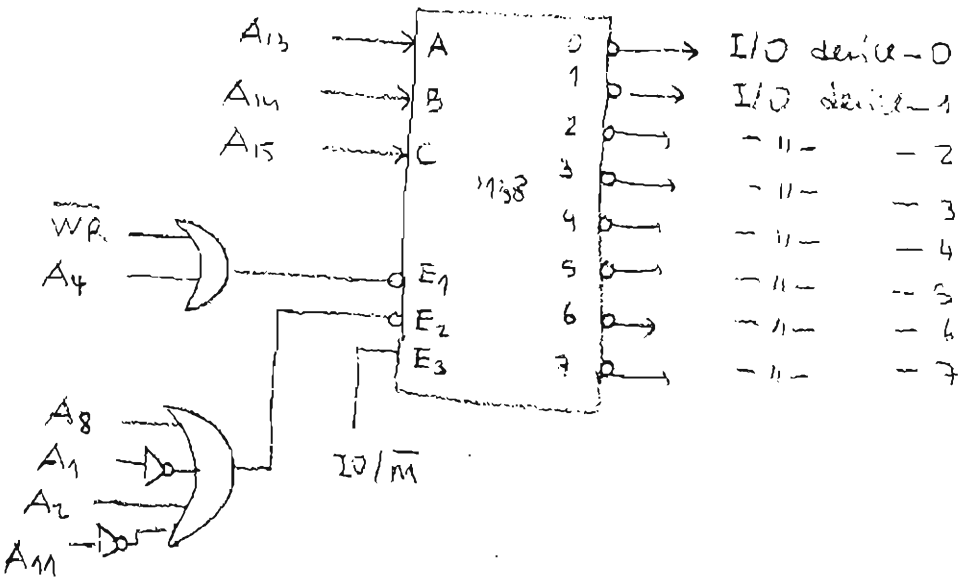


#2) Realize the same decoder circuitry by using a PROM that has the **minimum capacity**. Show the programming of the PROM as a truth table. Draw also the circuitry of the decoder. Assume that the PROM has two enable inputs where one of them is active high, and the other one is active low.

#3) Consider the I/O decoder circuitry shown in following figure.

a) What type I/O decoder circuit is it? Why?

b) Determine the selection addresses/address ranges of each I/O element. Under what condition are they selected?



GOOD LUCK ☺

INTRODUCTION TO MICROCOMPUTERS FINAL EXAM

SOLUTION MANUAL

November 03, 2010

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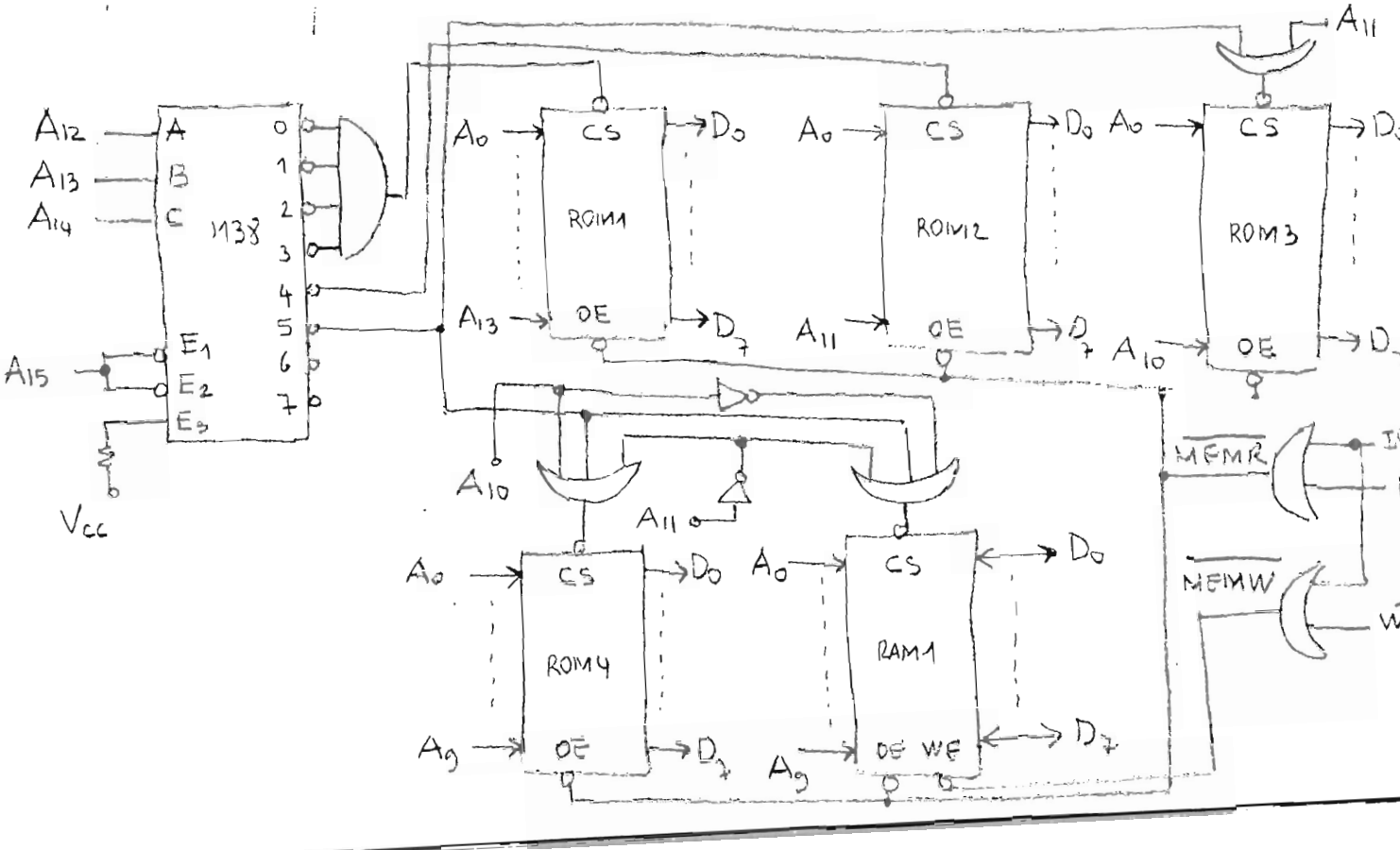
#1)

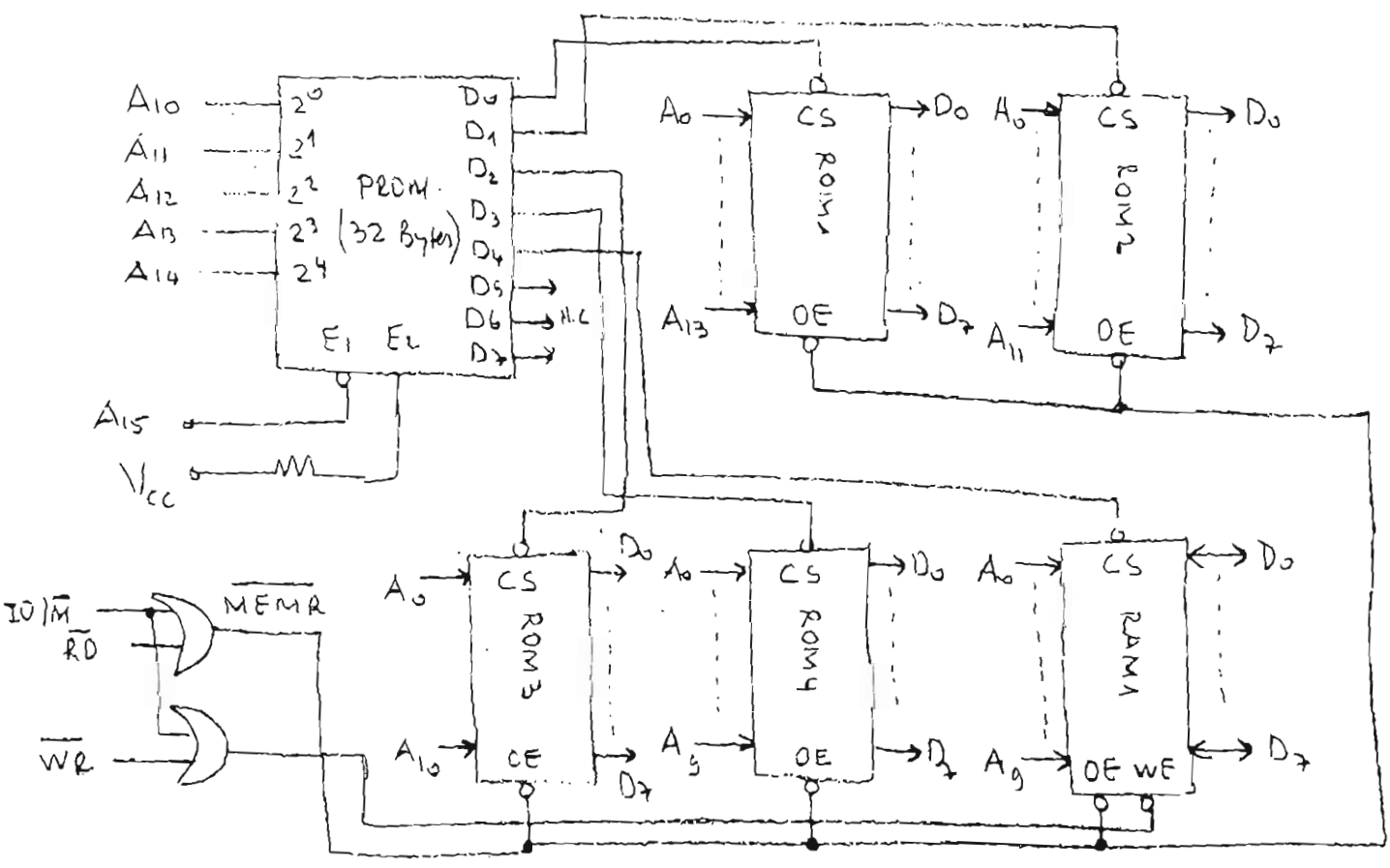
A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	A_7	A_6	A_5	A_4	A_3	A_2	A_1	A_0		
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 0000h	ROM1
0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	= 3FFFh	
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	= 4000h	ROM2
0	1	0	0	1	1	1	1	1	1	1	1	1	1	1	1	= 4FFFh	
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	= 5000h	ROM3
0	1	0	1	0	1	1	1	1	1	1	1	1	1	1	1	= 57FFh	
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	= 5800h	ROM4
0	1	0	1	1	0	1	1	1	1	1	1	1	1	1	1	= 5BFFh	
0	1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	= 5C00h	RAM1
0	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	= 5FFFh	



#2) Minimum capacity for PROM = 2^5 = 32 Byte

Programming of the PROM

INPUTS A_{14} A_{13} A_{12} A_{11} A_{10} / A_4 A_3 A_2 A_1 A_0	OUTPUTS D_7 D_6 D_5 D_4 D_3 D_2 D_1 D_0	
0 0 0 0 0	1 1 1 1 1 1 1 0	for ROM 1, 16 bytes
0 0 0 0 1		
:	– the same –	
0 1 1 1 1		
1 0 0 0 0	1 1 1 1 1 1 0 1	for ROM 2, 4 bytes
1 0 0 0 1		
1 0 0 1 0	– the same –	
1 0 0 1 1		
1 0 1 0 0	1 1 1 1 1 0 1 1	for ROM 3, 2 bytes
1 0 1 0 1	1 1 1 1 1 0 1 1	
1 0 1 1 0	1 1 1 1 0 1 1 1	for ROM 4, 1 byte
1 0 1 1 1	1 1 1 0 1 1 1 1	for RAM 1, 1 byte
the other locations	1 1 1 1 1 1 1 1	8 bytes



#3)

a) It is an isolated I/O decoder since $E_3 = 1$ for $IO/\overline{M} = 1$.

b)

A_7 A_6 A_5 / A_{15} A_{14} A_{13}	A_4 A_3 A_2 A_1 A_0 / A_{12} A_{11} A_{10} A_9 A_8	Hex Addr	Selected I/O device #
0 0 0	0 1 0 1 0	0Ah	0
0 0 1	— " —	2Ah	1
0 1 0	— " —	4Ah	2
0 1 1	— " —	6Ah	3
1 0 0	— " —	8Ah	4
1 0 1	— " —	AAh	5
1 1 0	— " —	CAh	6
1 1 1	— " —	EAh	7

They are selected when $\overline{WR} = 0$, therefore they are selected when data is read from those I/O devices.