
Logic and Computer Design Fundamentals

Verilog

Part 2 – Chapter 5 – Behavioral and Hierarchical Descriptions

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Overview

■ Part 2

- **Behavioral Descriptions**

- **Using:**

- Assignment statements
 - Higher level operators

- **Verilog Hierarchy**

- **Using:**

- Modules
 - Module instantiation

- **Example: Adder-Subtractor**

- Assignment statements using addition operator and vector XOR operator
 - Hierarchy with adder module and 1's complementer module

Behavioral & Hierarchical Verilog Example

- Circuit function can be described by assign statements at higher than the logic level:

```
module addsub (A, B, R, sub);  
    input [3:0] A, B;  
    output [3:0] R;  
    input sub; //sub ? subtract : add  
    wire[3:0] data_out  
    //Instantiate add and M1comp modules  
    add A1 (A, data_out, sub, R);  
    M1comp C1 (B, data_out, sub);  
endmodule
```

Behavioral & Hierarchical Verilog Example

(continued)

```
module add (X, Y, C_in, S);  
    input [3:0] X, Y;  
    input C_in;  
    output [3:0] S;  
    assign S = X + Y + {3'b0, C_in};  
endmodule  
  
module M1comp (data_in, data_out, comp);  
    input [3:0] data_in;  
    input comp;  
    output [3:0] data_out;  
    assign data_out = {4{comp}} ^ data_in;  
endmodule // {n{x}} means concatenate  
           // n copies of x
```

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