Logic and Computer Design Fundamentals Verilog

Part 4 – Chapter 7 – Registers and Counters

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Overview

Part 4

- Registers
- Shift Registers
- Counters
- Example
 - 4-bit Left Shift Register with Reset
 - 4-bit Binary Counter with Reset

Verilog for Registers and Counters

Register – same as flip-flop except multiple

```
bits: reg[3:0] Q;
    input[3:0] D;
   always@(posedge CLK or posedge RESET)
   begin
          if (RESET) Q \leq 4'b0000;
          else Q \leq D;
   end
```

Shift Register – use concatenate:

```
Q \le \{Q[2:0], SI\};
```

Counter – use increment/decrement:

```
count <= count + 1; or count <= count - 1</pre>
```

Verilog Description of Left Shift Register

```
// 4-bit Shift Register always@(posedge CLK or
  with Reset
                                        posedge RESET)
module srg 4 r v (CLK,
                           begin
  RESET, SI, Q, SO);
                              if (RESET)
   input CLK, RESET, SI;
                                 Q \le 4'b0000;
   output [3:0] Q;
   output SO;
                              else
   req [3:0] Q;
                                 Q \le \{Q[2:0], SI\};
   assign SO = Q[3];
                           end
                           endmodule
```

Verilog Description of Binary Counter

```
always@(posedge CLK or
// 4-bit Binary Counter with
                                posedge RESET)
  Reset
                              begin
module count 4 r v (CLK,
                                 if (RESET)
  RESET, EN, Q, CO);
                                    count <= 4'b0;
   input CLK, RESET, EN;
                                 else if (EN)
   output [3:0] Q;
                                    count <= count + 1;
   output CO;
                              end
                              endmodule
   reg [3:0] count;
   assign Q = count;
   assign CO = (count ==
  4'b1111 & EN == 1'b1) ? 1
  : 0;
```

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