DIGITAL SYSTEMS – II SECOND MIDTERM EXAM

Dr. Salih FADIL **April 28, 2009**

#1) A sequential circuit with three positive edge-triggered D flip-flops A, B and C and one input COUNT is to be designed. When COUNT=0, the state of the circuit remains the same. When COUNT=1, the circuit goes through state transitions from 000 to 001 to 010 to 011 to 100 to 101 to 110 to 111, back to 000 and then repeats (3-bit binary up counter).

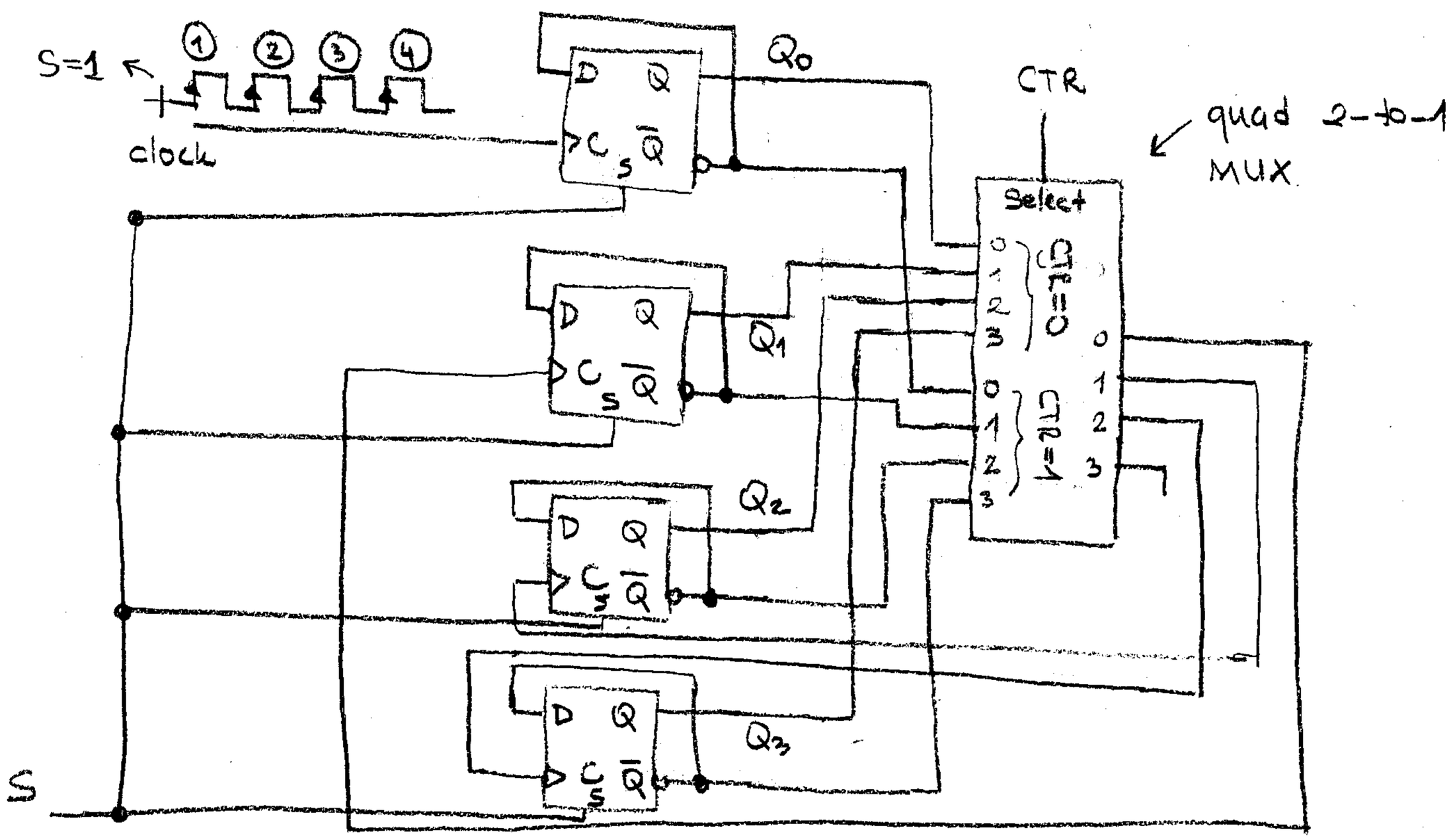
a) Draw state diagram of the circuit.
b) Draw two-dimensional state table of the circuit.
c) Obtain minimum SOP form of flip-flop input equations and realize the circuit by using AND, OR and NOT gates.

#2) Function table for a 4-bit rotator is given as follows;

Mode Control		*Register operation*
S_1	S_0	
0	0	No change
0	1	Rotate left
1	0	Rotate right
1	1	Load parallel data

Realize the 4-bit rotator by using multiplexers and positive edge triggered D flip-flops.

#3 Consider the following sequential circuit. Assume that S=1 is made before the first active clock edge. Determine the Q outputs of the D flip-flops after the third active clock edge when CTR=1. Determine also $\overline{Q}$ outputs of the D flip flops after the second active clock edge when CTR=0. What does this sequential circuit do?



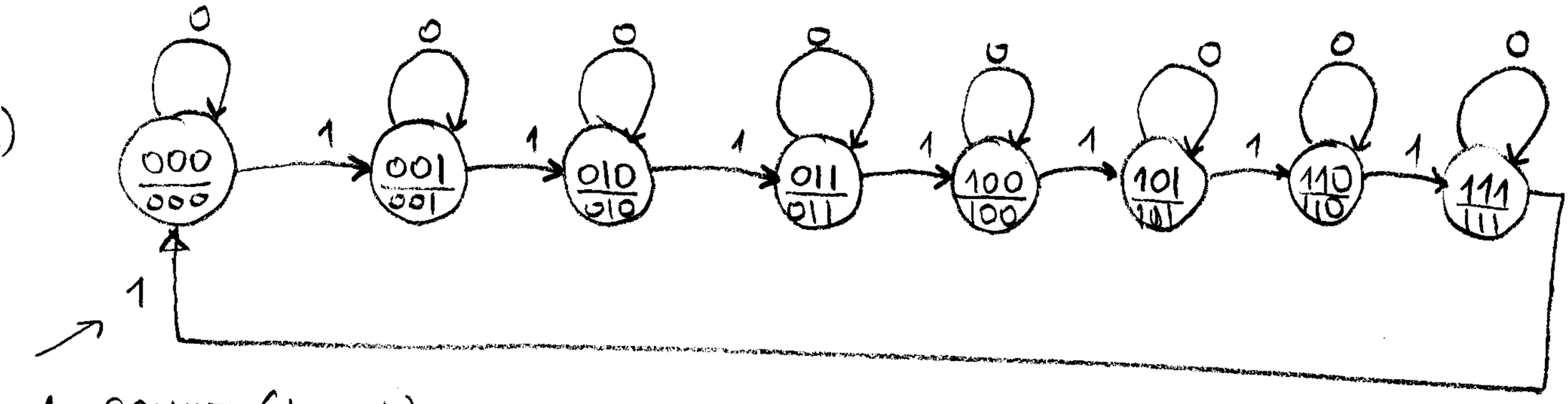
DIGITAL SYSTEMS - II SECOND MIDTERM EXAM

SOLUTION MANUAL

Dr. Salih FADIL

April 28, 2009

#1) a)



The outputs of the circuit are the Q output of the D flip-flops (A, B and C)

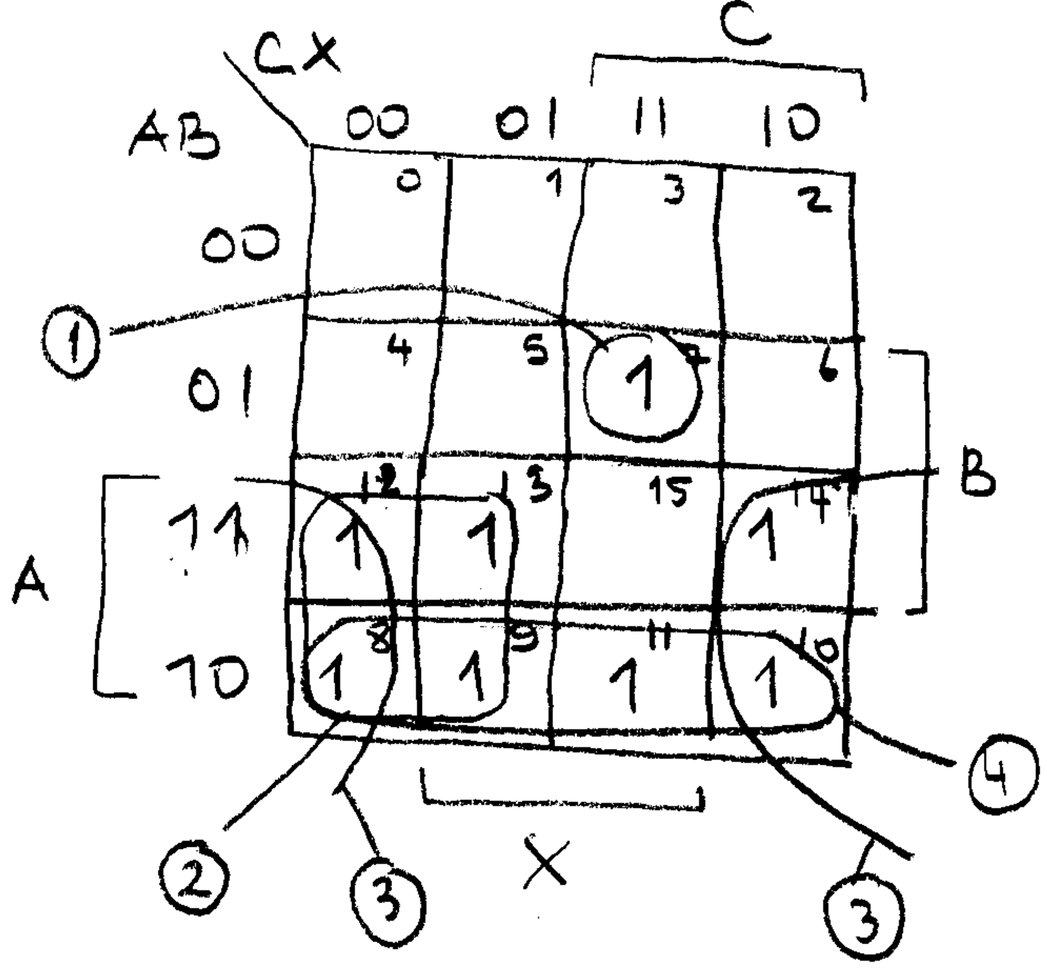
b)

present state	Next State x=1	Next State x=0
A B C	A B C	A B C
0 0 0 0	0 0 1	0 0 0
1 0 0 1	0 1 0	0 0 1
2 0 1 0	0 1 1	0 1 0
3 0 1 1	1 0 0	0 1 1
4 1 0 0	1 0 1	1 0 0
5 1 0 1	1 1 0	1 0 1
6 1 1 0	1 1 1	1 1 0
7 1 1 1	0 0 0	1 1 1

c) $D_A(A, B, C, X) = \sum m(8, 10, 12, 14, 7, 9, 11, 13)$

$D_B(A, B, C, X) = \sum m(4, 6, 12, 14, 3, 5, 11, 13)$

$D_C(A, B, C, X) = \sum m(2, 6, 10, 14, 1, 5, 9, 13)$



for D_A

step-1) (1)

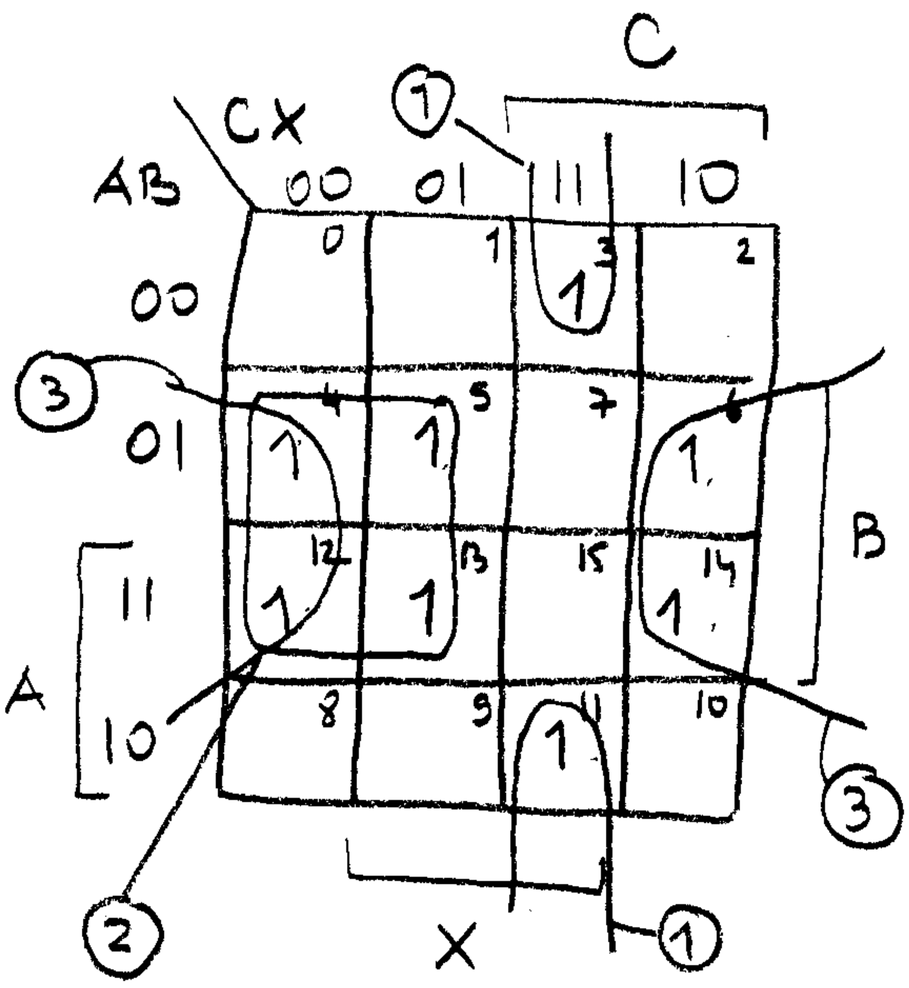
step-2) None

step-3) (2), (3), (4) stop.

$$D_A = \bar{A}BCX + A\bar{C} + A\bar{X} + A\bar{B}$$

$$= \bar{A}BCX + A(\overline{BCX})$$

$$D_A = A \oplus (BCX)$$



for D_B

step-1) None

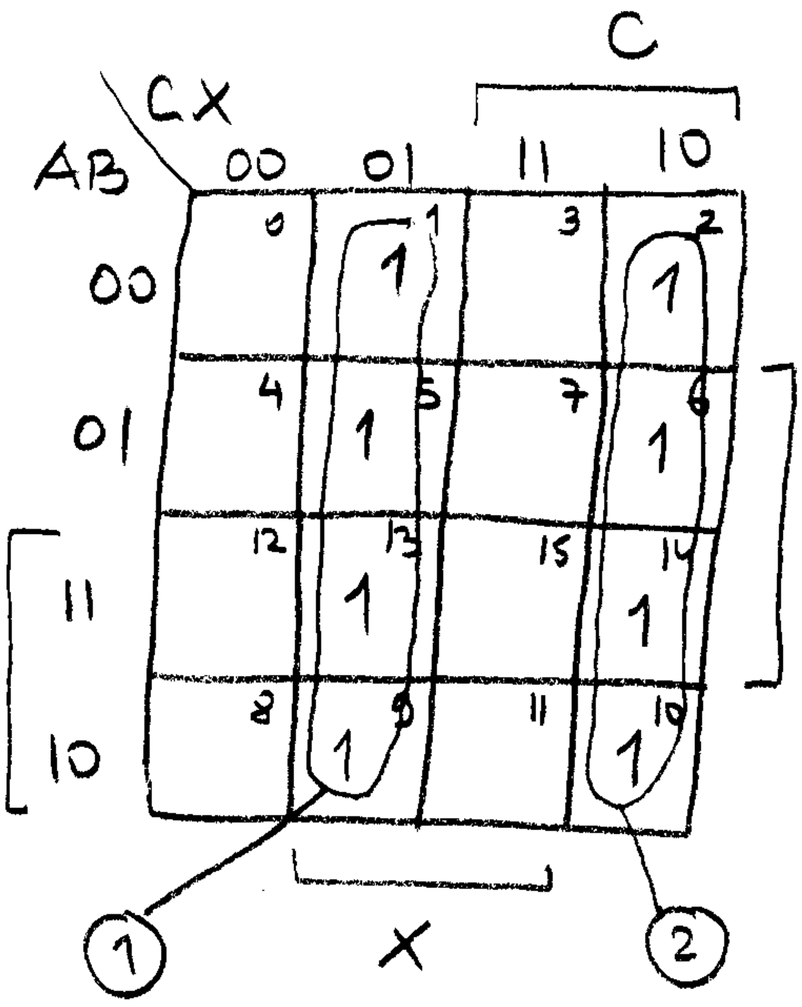
step-2) (1)

step-3) (2), (3) stop.

$$D_B = \bar{B}CX + B\bar{C} + B\bar{X}$$

$$= \bar{B}CX + B(\overline{C \cdot X})$$

$$D_B = B \oplus (CX)$$



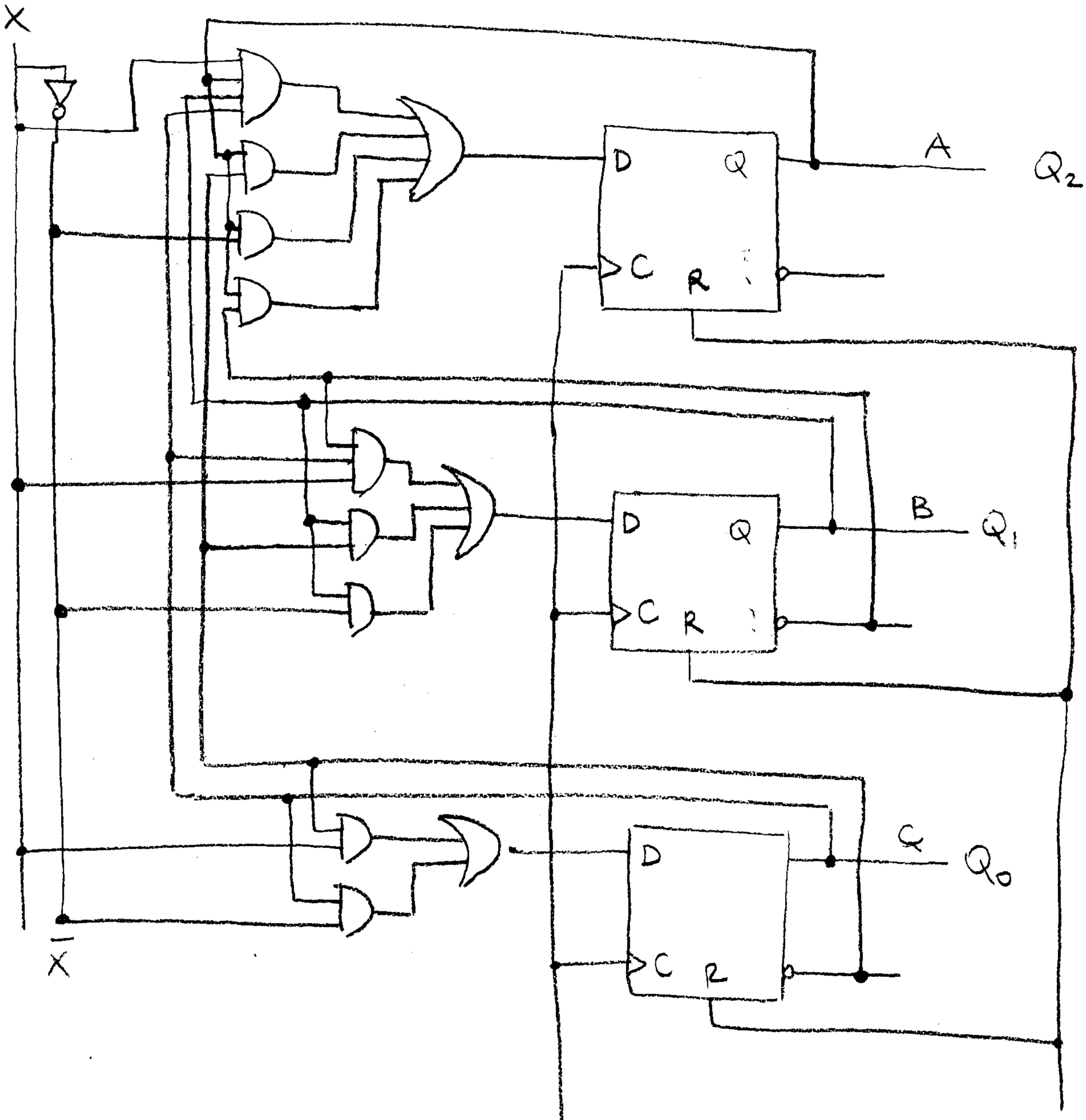
for D_C

step-1) None

step-2) None

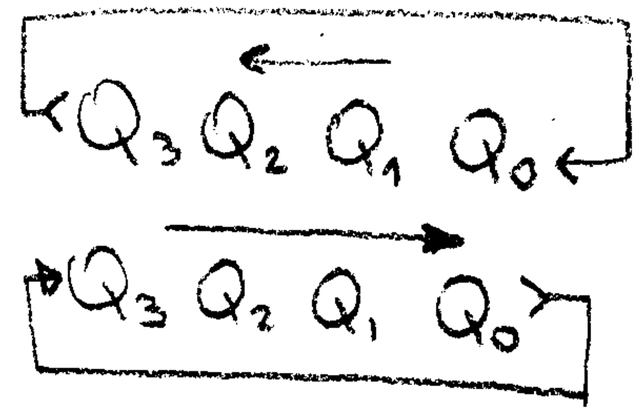
step-3) (1), (2)

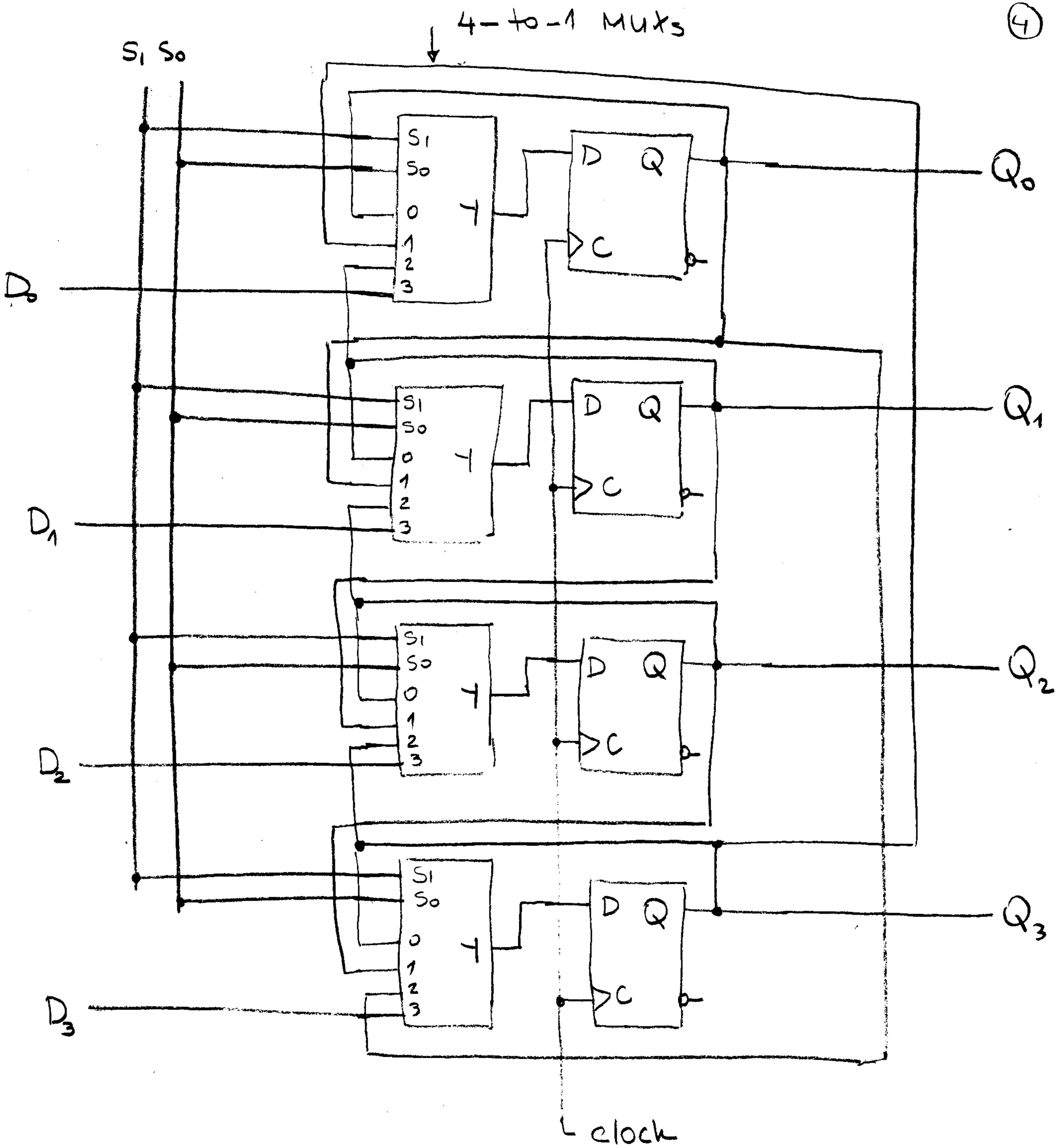
$$D_C = \bar{C}X + \bar{X}C = C \oplus X.$$



#2)

Mode control S_1	S_0	Register operation
0	0	No change
0	1	Rotate left
1	0	Rotate right
1	1	Load parallel data





#3) From examination of the given sequential ckt, we can see the following connections

CTR = 1.

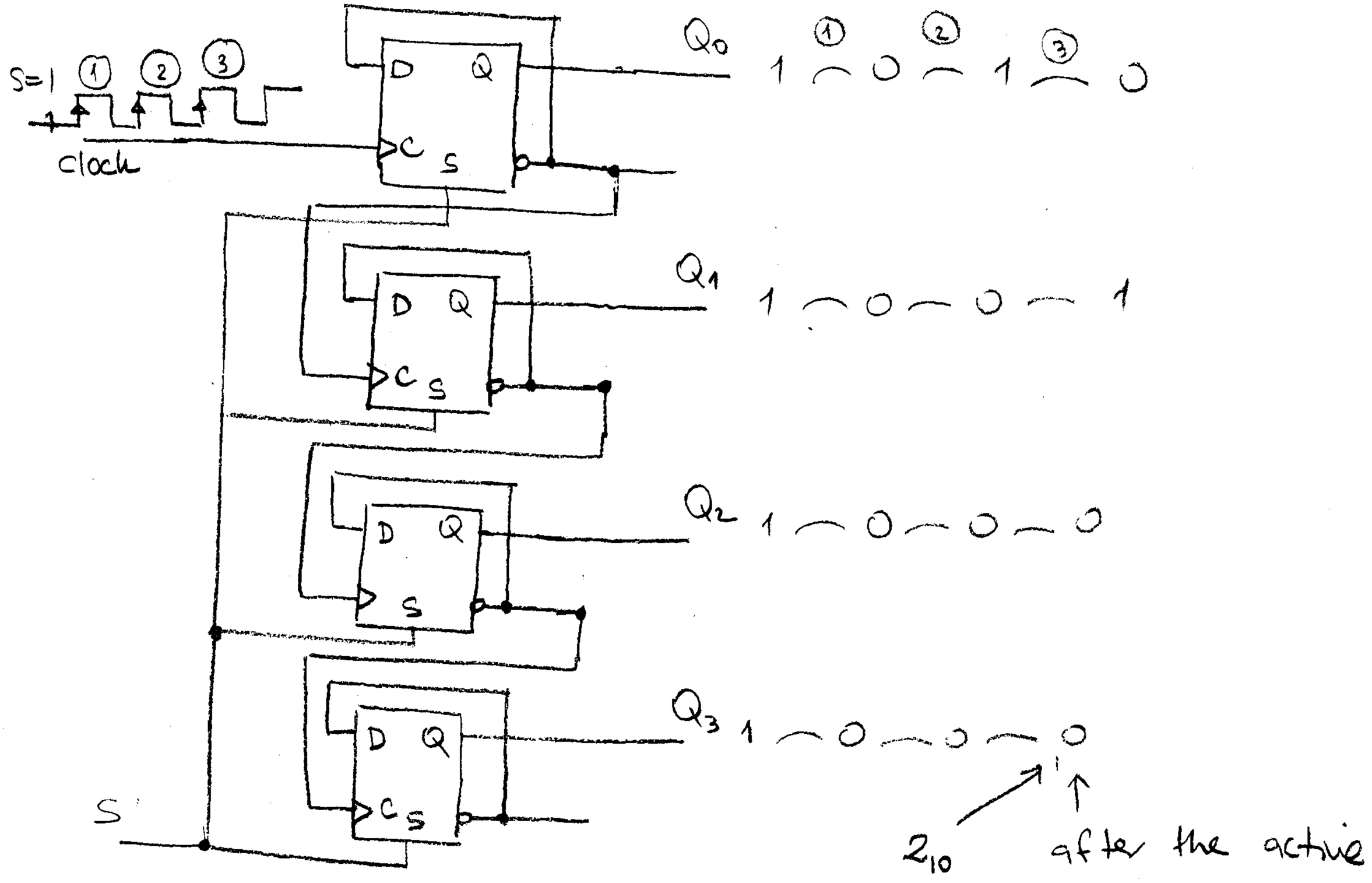
$\bar{Q}_0$ → C input of 1st flip-flop.
$\bar{Q}_1$ → C " " 2nd " "
$\bar{Q}_2$ → C " " 3rd " "

} 4-bit ripple up counter

When CTR = 0

Q_0 → C input of 1st flip-flop
Q_1 → C " " 2nd " "
Q_2 → C " " 3rd " "

} 4-bit ripple down counter



When CTR=1, the circuit becomes a 4-bit ripple <u>up</u> counter

When CTR=0 the circuit becomes a 4-bit ripple <u>down</u> counter