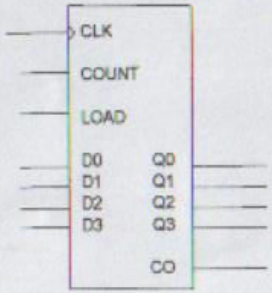
Name :
Student ID :

SOLUTIONS

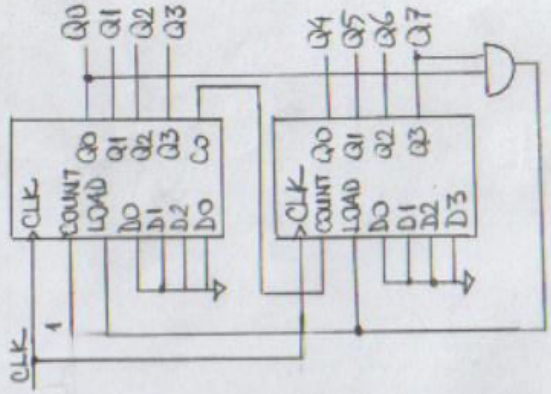
Digital Systems II
2007-08 Summer
Quiz III
13/08/08

Binary Counter with parallel load

1. Construct a binary counter that counts from decimal 0 to decimal 129 using two binary counters with parallel load and logic gates. [20pts]



	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	0	0
				⋮				
129	1	0	0	0	0	0	0	1



Register Cell Design

2. Design a register cell for register A, which has the following register transfers:

ADD ~~INCR~~: $A \leftarrow A + B$

$SHFT : A \leftarrow sl\ A$

$$S_i = A_i \oplus B_i \oplus C_i$$
$$C_{i+1} = A_iB_i + A_iC_i + B_iC_i$$

Minimize the lateral connections between the cells. Design the cell with D flip-flops. Use multiplexer approach. [20pts]

$LOAD = ADD + SHFT$ 04 pts

$D_{i,FF} = \overline{LOAD}\, A_i + LOAD.D_i$ 04 pts

$D_i = A_i(t+1) = ADD(A_i \oplus B_i \oplus C_i) + SHFT.C_i$ 06pts

$C_{i+1} = ADD(A_iB_i + A_iC_i + B_iC_i) + SHFT.A_i$ for i>

06pts

For cell 0, $C0 = 0$

$D_0 = A_0(t+1) = ADD(A_i \oplus B_i \oplus C_i)$

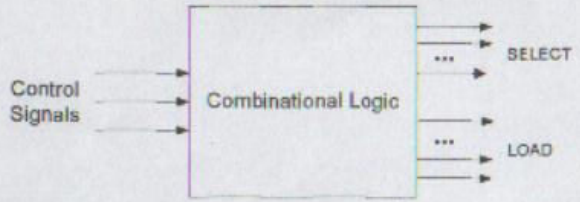
$C_1 = ADD(A_iB_i + A_iC_i + B_iC_i) + SHFT.A_0$

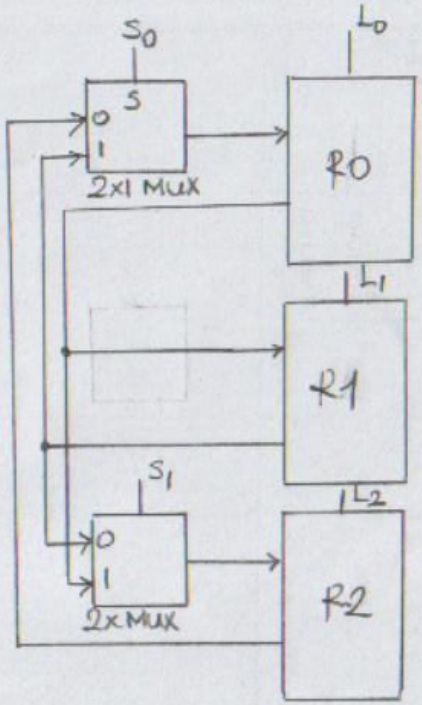
3. A system is to have the following set of register transfers, implemented using dedicated multiplexers:

$$C_A : R1 \leftarrow R0$$
$$C_B : R0 \leftarrow R1, R2 \leftarrow R0$$
$$C_C : R0 \leftarrow R2, R2 \leftarrow R1$$

a) Using the registers and the dedicated multiplexers, draw the logic diagram of the system hardware that implements these register transfers. [10pts]

b) Design a combinational logic circuit (encoder) that converts the control variables C_A, C_B and C_C as inputs to outputs that are the SELECT inputs for multiplexers and LOAD signals for the registers. [15pts]





Microoperation	C_A	C_B	C_C	S_1	S_0	L_0	L_1	L_2
R1 ← R0	1	0	0	x	x	0	1	0
R0 ← R1, R2 ← R0	0	1	0	1	1	1	0	1
R0 ← R2, R2 ← R1	0	0	1	0	0	1	0	1
	0	0	0	x	x	0	0	0

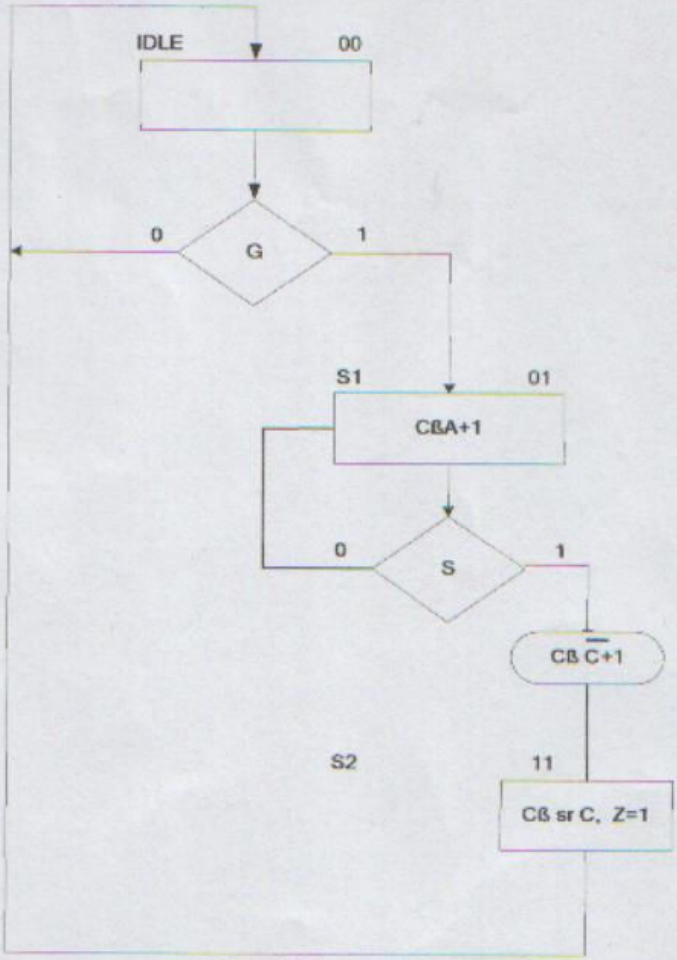
$L_0 = C_B + C_C$

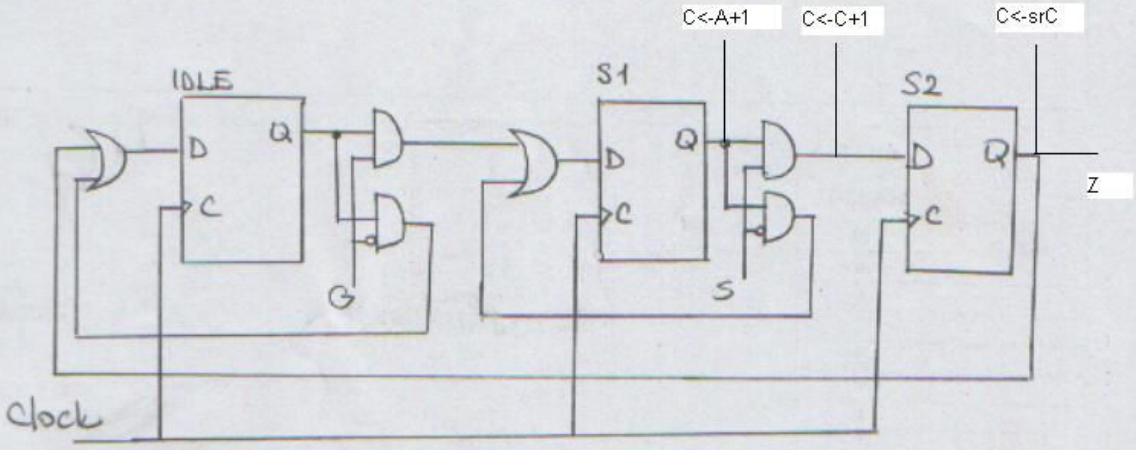
$L_1 = C_A$

$L_2 = L_0$

$S_1 = S_0 = C_B$

4. Implement the ASM chart by using the one flip-flop per state [25pts].





Memory Basics

5. The following memories are specified by the number of words times the number of bits per word. How many address lines and input-output data lines are needed for the following cases? a) 128Kx32 b) 1024x64. [10pts]

a. $128K = 2^7 \times 2^{10} = 2^{17}$

17 address lines
32 input-output data lines

b. $1024 = 2^{10}$

10 address lines
64 input-output data lines