Name :
Student ID :

24.03.2009

Digital Systems II

Midterm I

2008-09 Spring

No script sheet is allowed.

SOLUTIONS

1.	
2.	
3.	
4.	

Good Luck

Sequential Circuit Design

1. A Universal Serial Bus (USB) communication link requires a circuit that produces the sequence 00000001. Design a synchronous sequential circuit that starts producing this sequence for input E=1. If E=1, during the last output in the sequence, the sequence repeats (Fig. 1). Otherwise, if E=0, the output remains constant at 1 (Fig. 2).

a. Draw the Moore state diagram for the circuit. [15pts]
b. Find the state table and make state assignments using Gray codes. [10pts]
c. Design the circuit using D flip-flops and logic gates. Do not draw the logic diagram. [15pts]

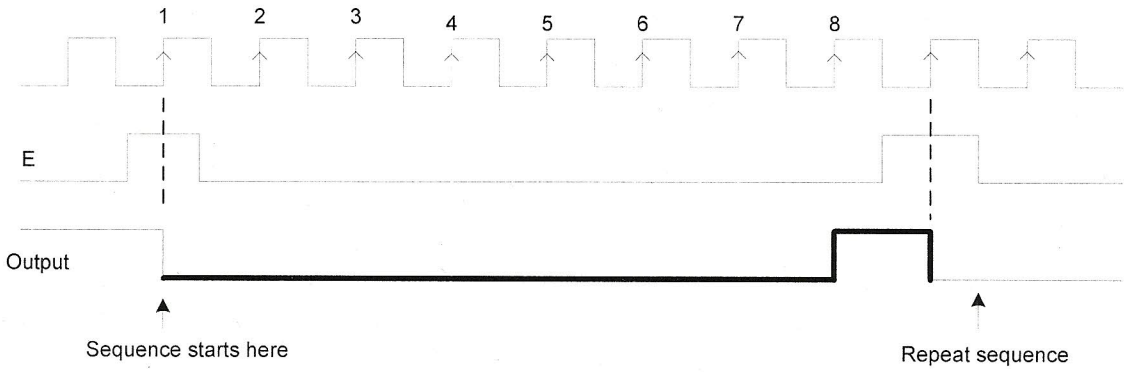


Fig.1 Repeat the sequence if E=1 during the last output sequence

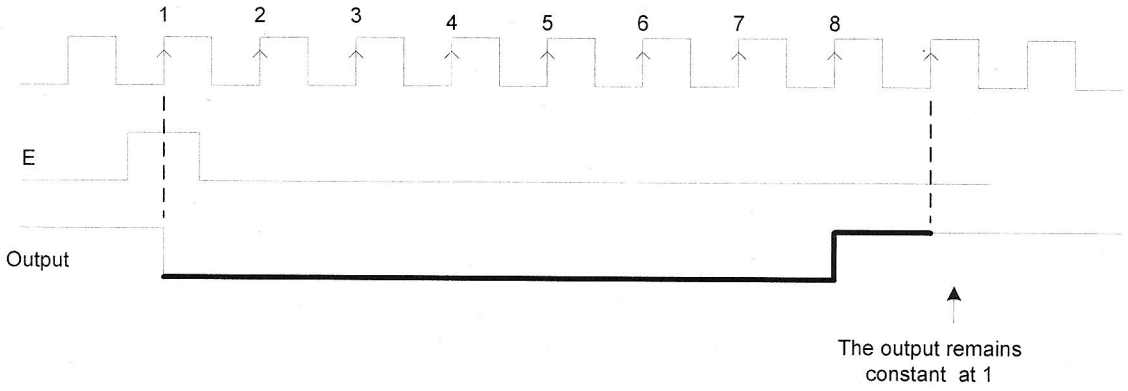
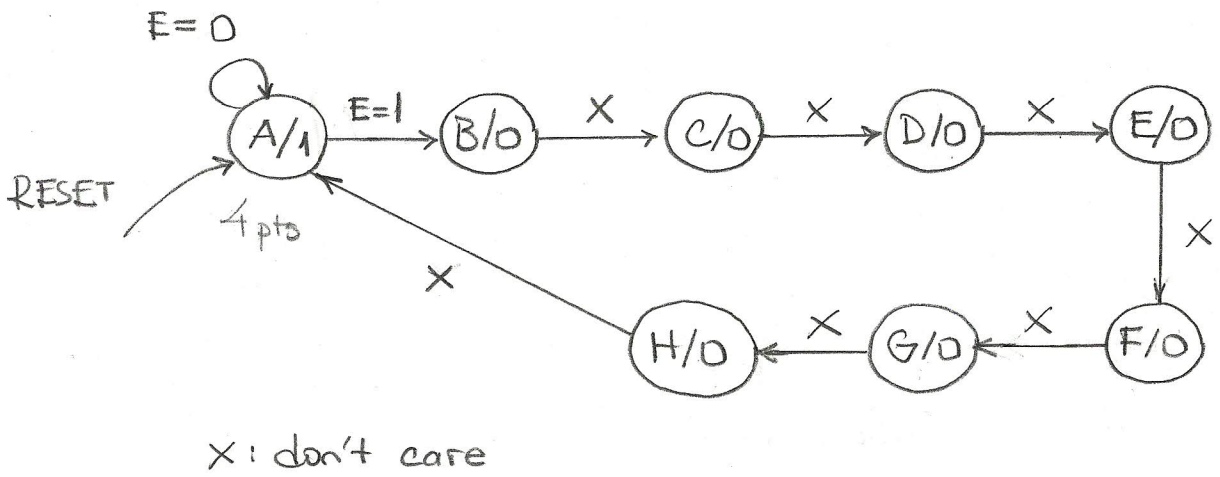


Fig.2 E=0, the output remains at the logic 1.



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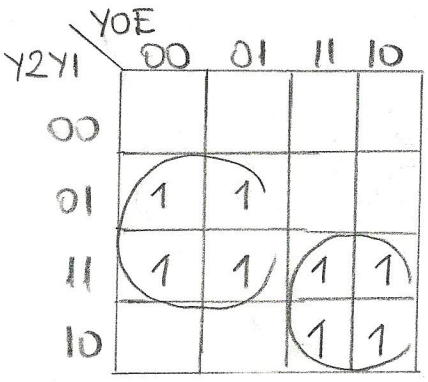
b.

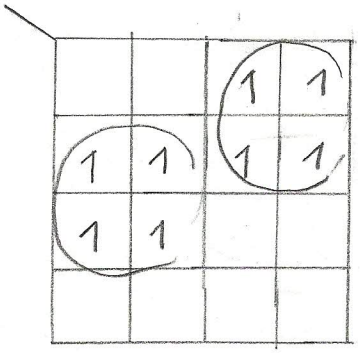
Present State	Next State E=0	Next State E=1	Output
A	A	B	1
B	C	C	0
C	D	D	0
D	E	E	0
E	F	F	0
F	G	G	0
G	H	H	0
H	A	A	0

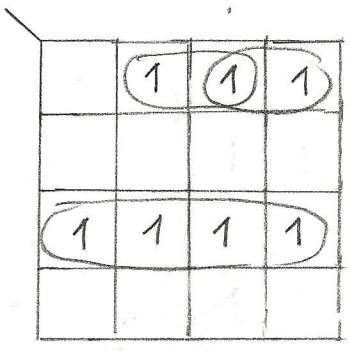
A=000
B=001
C=011
D=010
E=110
F=111
G=101
H=100

c.

Present State $Y_2Y_1Y_0$	Input E	Next State $Y_2Y_1Y_0$	Output Z
0 0 0	0	0 0 0	1
0 0 0	1	0 0 1	1
0 0 1	X	0 1 1	0
0 1 1	X	0 1 0	0
0 1 0	X	1 1 0	0
1 1 0	X	1 1 1	0
1 1 1	X	1 0 1	0
1 0 1	X	1 0 0	0







$Y_2(t+1) = D_{Y_0} = Y_1\bar{Y}_0 + Y_2Y_0$ $Y_1(t+1) = D_{Y_1} = Y_1\bar{Y}_0 + \bar{Y}_2Y_0$ $Y_0(t+1)$

04 pts

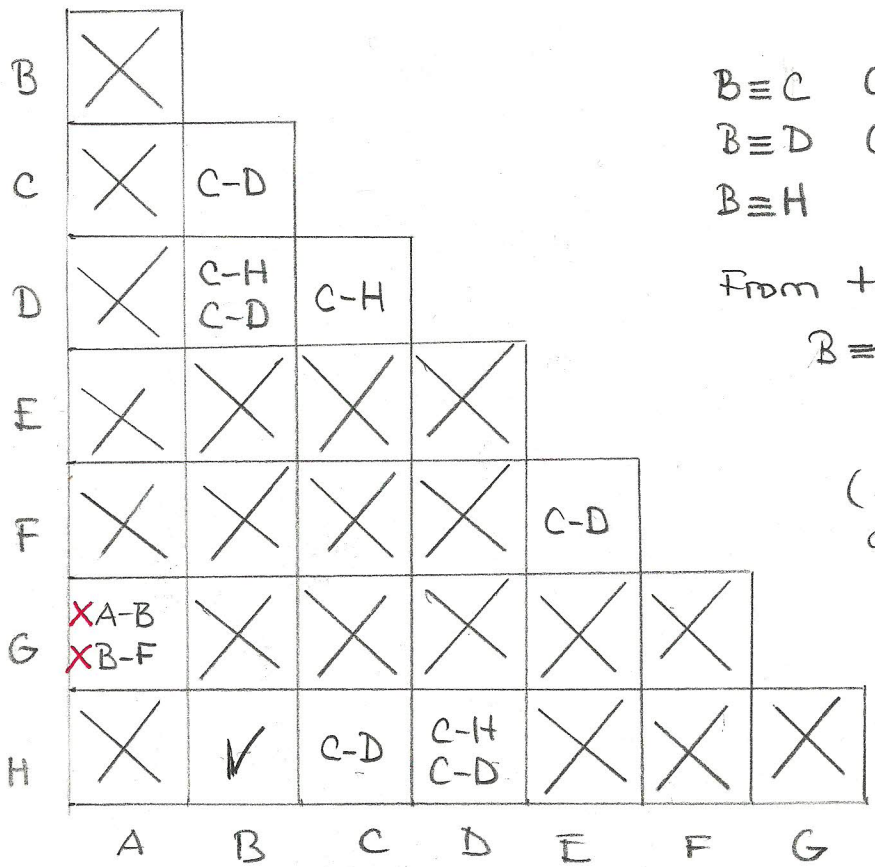
$Y_0(t+1) = D_{Y_0} = \bar{Y}_2\bar{Y}_1Y_0 + \bar{Y}_2\bar{Y}_1E + Y_2Y_1$

Output $Z = \bar{Y}_2\bar{Y}_1\bar{Y}_0$

State Reduction

2. Eliminate the redundant states, if any, from the following state tables using implication table. Make the reduced state table. [20pts]

Present State	Next State		Output (Z)	
	X=0	X=1	X=0	X=1
A	A	B	0	0
B	H	C	1	0
C	H	D	1	0
D	C	D	1	0
E	C	E	1	1
F	D	E	1	1
G	B	F	0	0
H	H	C	1	0



B≡C C≡D D≡H E≡F
B≡D C≡H
B≡H

From transitive property
B≡C≡D≡H

(A) (B, C, D, H) (E, F) (G)
q_0 q_1 q_2 q_3

	Present State	Next State X=0	Next State X=1	Output X=0	Output X=1
A	q_0	q_0	q_1	0	0
B, C, D, H	q_1	q_1	q_1	1	0
E, F	q_2	q_1	q_2	1	1
G	q_3	q_1	q_2	0	0

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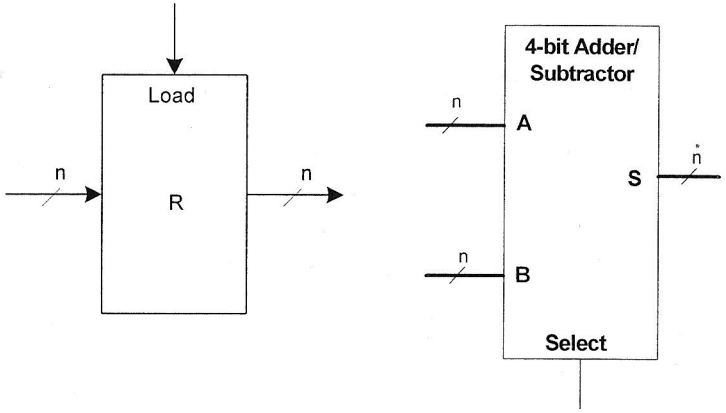
Hardware Design for Register Transfers

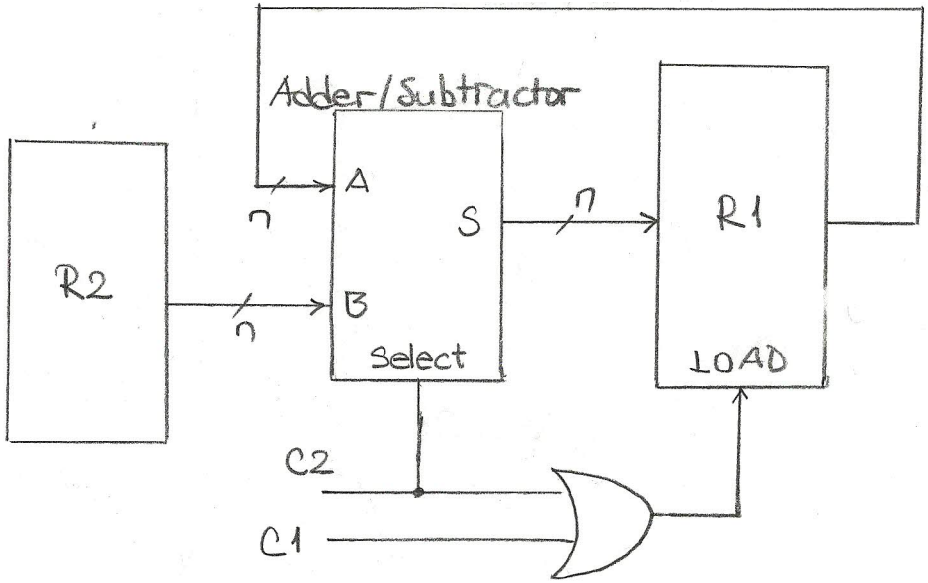
3. Show the diagram of the hardware that implements the following register transfer statements:

C1: R1←R1+R2
C2: R1←R1-R2 (two's complement subtraction)

Use 4-bit adder/subtractor and plus external gates as needed. The control signals, C1 and C2, are mutually exclusive. [20pts]

Select=0 → S=A+B (add),
Select=1 → S=A-B (subtract).





Shift Register with Parallel Load

4. 3-bit shift register operates according to the following function table: [20pts]

S1	S0	Register operation
0	0	No change
0	1	Parallel Load
1	0	Arithmetic Shift Right
1	1	Logical Shift Right

Draw logic diagram of the shift register. Implement the register with D flip-flops and 4x1 multiplexers. S1 and S0 are the mode select inputs.

Shift Right Register