**Name**
**Student ID:**

**45 minutes**

**Digital Systems II, 2009-10 Spring**
**Quiz I**

SOLUTIONS

**16.03.2010**
19.03.2010

1. For the sequential circuit in Figure 1:
   a) Derive the state table. (20pts)
   b) Derive the state diagram. (14pts)

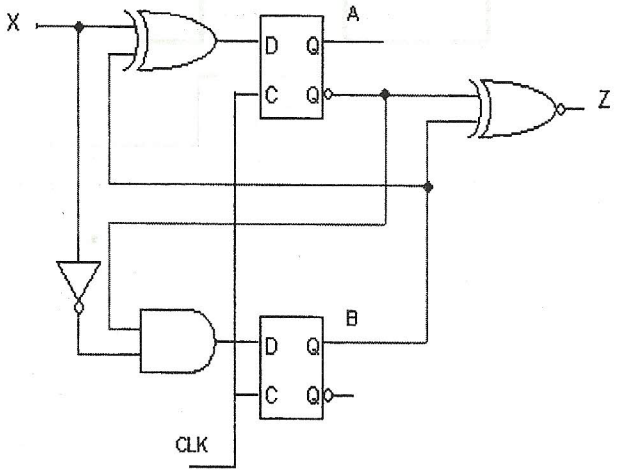
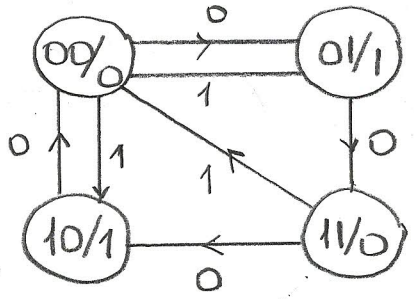



Figure 1

b)




$A(t+1) = x \oplus B \quad B(t+1) = \bar{x}\,\bar{A} \quad Z = \overline{\bar{A} \oplus B} = A \oplus B$

a)

| Present State A | Present State B | Input x | Next State A(t+1) | Next State B(t+1) | Output Z |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 | 1 |
| 0 | 1 | 1 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 1 | 0 | 0 | 0 |

2. Design 2-bit binary up/down counter with the direction (DIR) input. DIR=0 count-down, DIR=1 count-up. Use T flip-flops. Do not draw the logic circuit. (40pts)

State/Transition Table

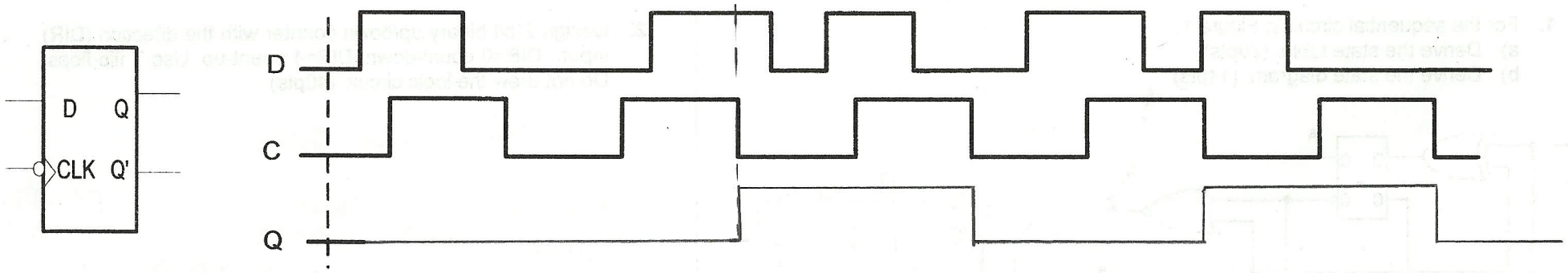
| Present State A | Present State B | Input DIR | Next State A(t+1) | Next State B(t+1) | Flip-Flop Inputs $T_A$ | Flip-Flop Inputs $T_B$ |
|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 0 | 0 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| 1 | 0 | 1 | 1 | 1 | 0 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 1 |

| A \ B.DIR | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | | 1 | |
| 1 | 1 | | 1 | |

$T_A = \bar{B}\,\overline{DIR} + B.DIR = \overline{B \oplus DIR}$

$T_B = 1$

3. Sketch the output Q of the edge triggered D flip-flop. The flip-flop is initially RESET. (14pts)




4. Give the list of flip-flop timing parameters. (12pts)

- Set-up time
- Hold time
- Propagation delay
- Clock frequency