Eskişehir Osmangazi University

Digital Systems II-Evening Class

Homework II

Spring 2006, Solutions : 28.03.2006

---

1. If the waveforms in Figure 1 are applied to an S-R latch, sketch the resulting Q output waveform in relation to the inputs. Assume Q starts LOW.

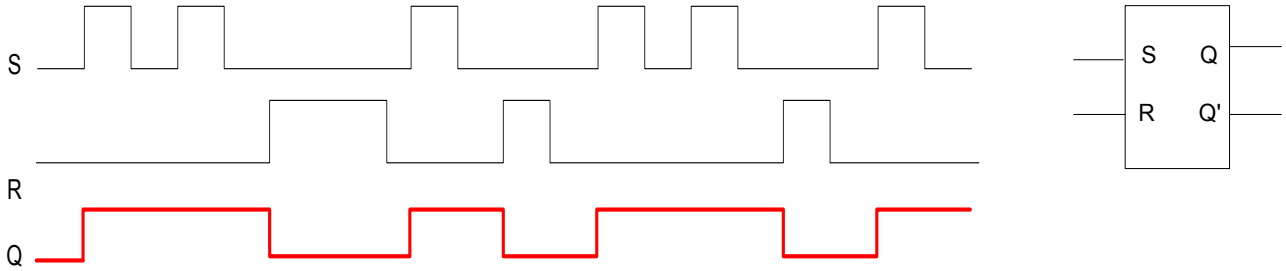


Figure 1

2. For a gated D latch, the waveform shown in Figure 2 is observed on its inputs. Sketch the timing diagram showing the output waveform you expect t see at Q if the latch is initially RESET.

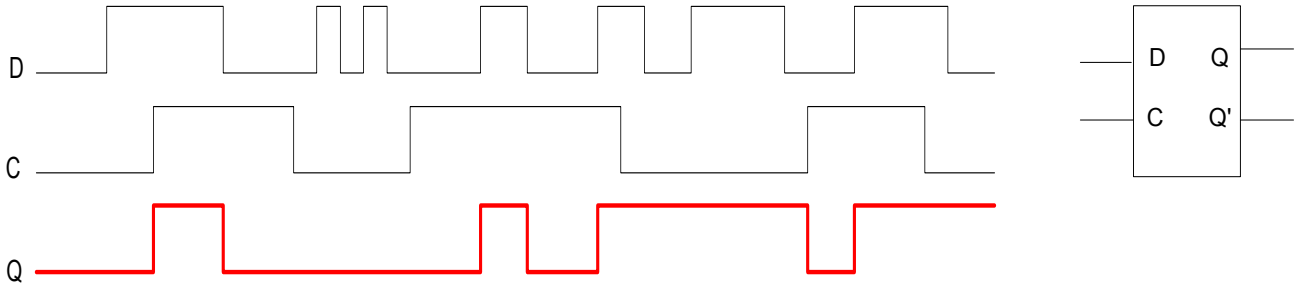


Figure 2

3. For D master-slave flip-flop, the waveform shown in Figure 3 is observed on its inputs. Sketch the output Q. Assume that Q is initially LOW.

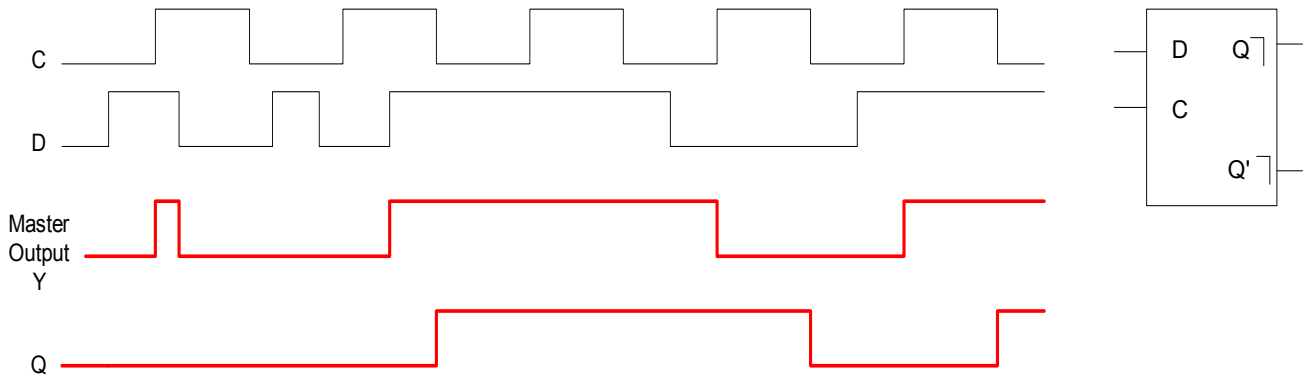


Figure 3

4.

a) For the circuit in Figure 4.a, sketch the output Q. Assume that Q=0 initially.

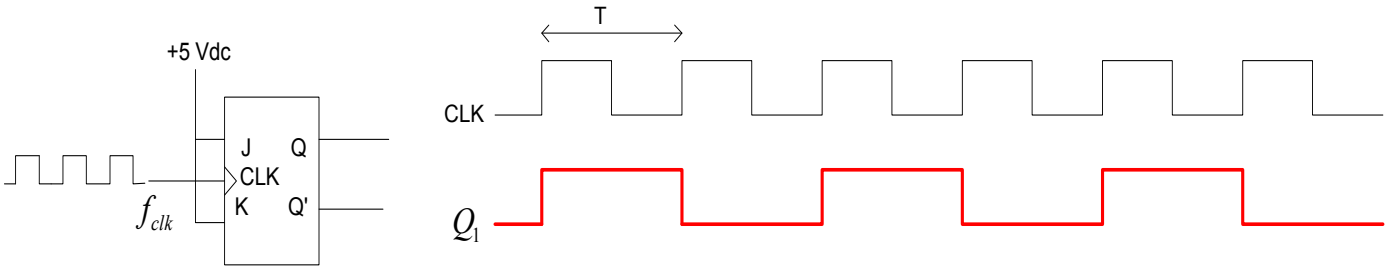


Figure 4.a

b) For the circuit given in Figure 4.b, sketch waveforms at the outputs Q1 and Q2. If $f_{clk} = 10KHz$, find f_2?

$$f_1 = \frac{f_{clk}}{2}\ ,\ f_2 = \frac{f_1}{2} \ \Rightarrow\ f_2 = \frac{f_{clk}}{4} = \frac{10KHz}{4} = 2.5KHz$$

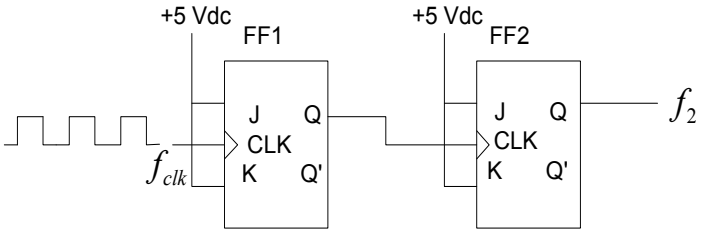
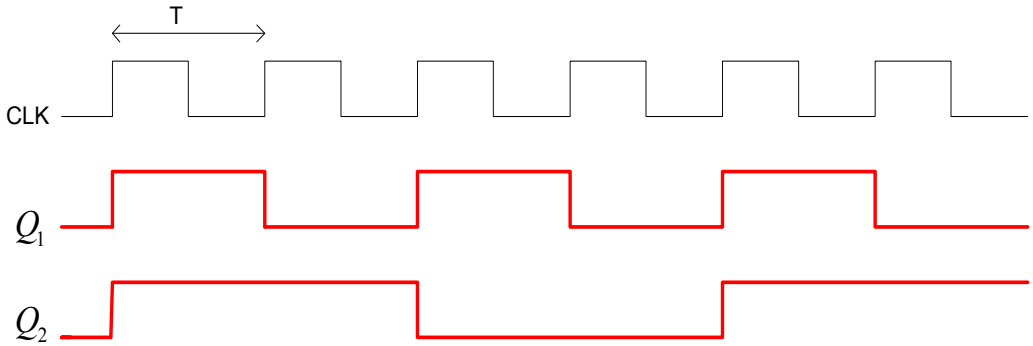


Figure 4.b



http://www.ogu.edu.tr/~redizkan/DigitalSysII_Evening_HW2_Sol.pdf