**Name :** **March 31, 2006**
**Student ID :**

| 1 | 2 | 3 | 4 | 5 | Grade /100 |
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Digital Systems II-Evening Class, Midterm I
105 minutes
No calculator or script sheet is allowed.

**Latch**

1. Consider the AB latch shown in Figure 1. (30pts)

a) Give the function table of this latch.

| A | B | $Q^{n+1}$ |
|---|---|---|
| … | … | … |
| … | … | … |

b) Derive the characteristic equation.
$Q^{n+1}=f(A,B,Q^n)$

c) Complete the timing diagram in Figure 2. Assume that gate delays are 0.

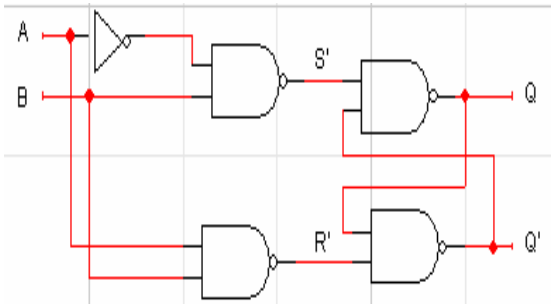



Figure 1. AB latch

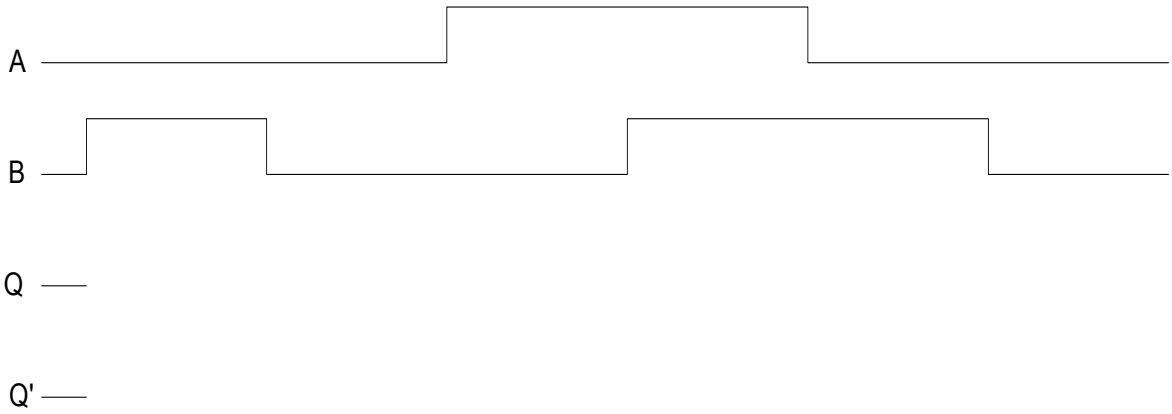



Figure 2. Timing diagram

**Sequential circuit analysis**

2. A sequential circuit has two JK flip-flops A and B, one input x and one output Z. The flip-flop input equations and circuit output equation are:

$$J_A = \overline{x} \qquad K_A = x + B$$
$$J_B = \overline{x}\,\overline{A} \qquad K_B = x + \overline{A}$$
$$Z = \overline{x}\,\overline{A}\,B$$

a) Is this a Mealy or Moore circuit? (02pts)
b) Find the state table and draw the state diagram. (15pts)
c) Starting from state "10" in the state diagram, determine the state transitions and output sequence when an input sequence of 001010111101 is applied. (08pts)

**2's complement signed numbers**

3. a) What is the most positive and negative number that can be represented by 10-bit 2's complement number? Express your answer in decimal form. (05pts)

   b) Perform the following arithmetic operations using 2's complement representation for negative numbers. Express the result as an 8-bit number (use 2's complement for negative numbers). Indicate when overflow has occurred. (15pts)

   - +65+39
   - -56+32
   - -96-45

**Ripple and Carry Lookahead Adder**

4. Consider the 3-bit parallel adder. The sum and carry signal of a full-adder can be written as

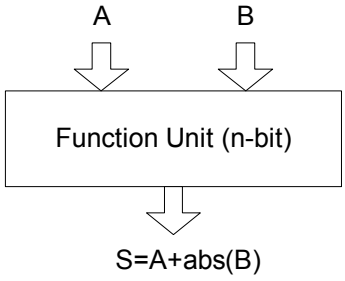
$$S_i = A_i \oplus B_i \oplus C_i$$
$$C_{i+1} = A_i B_i + C_i (A_i \oplus B_i)$$

   a) Assume that the 3-bit adder has been implemented as a ripple adder. (10pts)
      - Under what condition would the worst case delay occur: give the signals $A_2A_1A_0$ and $B_2B_1B_0$ for which the worst case occurs?
      - Give the worst case delay with which the carry out $C_3$ will appear. Assume that all gates have the same delay of 1ns. The signal $A_i$ and $B_i$ are applied to the adder inputs at the moment $t$=0.

   b) You will use carry lookahead adder to reduce the delay. Derive the carry-out signal of second stage, i.e. $C_2$ for the carry lookahead adder. (10pts)

**Arithmetic**

5. Design a combinational circuit that adds absolute value of B to A, $S = A + |B|$. A and B are 4-bit numbers. Assume that the numbers are 2's complement signed numbers. (Hint: use 4-bit adder/subtractor). (05pts)




Good Luck