Name
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Digital Systems II
2010-2011 Spring Quiz II

SOLUTIONS

April 19, 2011

April 23, 2011

1. Design a sequential circuit with one input X and one output Z that implements the state diagram in Figure 1. Use D flip-flops. Do not draw the logic diagram. Use Gray codes for state assignment. (40pts)

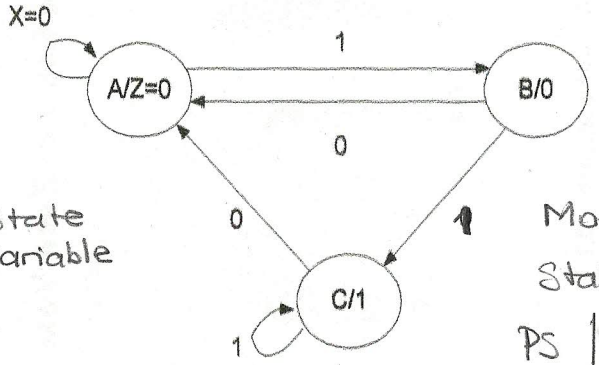


Figure 1. State diagram

Y_1, Y_0: State variable

A = 00
B = 01
C = 11

Moore circuit

State Table

PS	NS X=0	NS X=1	Output
A	A	B	0
B	A	C	0
C	A	C	1

Transition Table

PS Y_1 Y_0	NS X=0	NS X=1	Output Z
0 0	00	01	0
0 1	00	11	0
1 1	00	11	1
1 0	XX	XX	0

Y_1Y_0 \ X	0	1
00		
01		1
11		1
10	X	X

$D_{Y_1} = Y_1(t+1) = Y_0 x$

Y_1Y_0 \ X	1
	1
	1
	1
X	X

$D_{Y_0} = Y_0(t+1) = x$

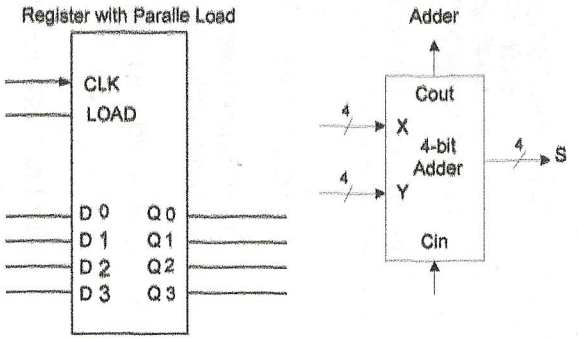
Flip-Flop input equations

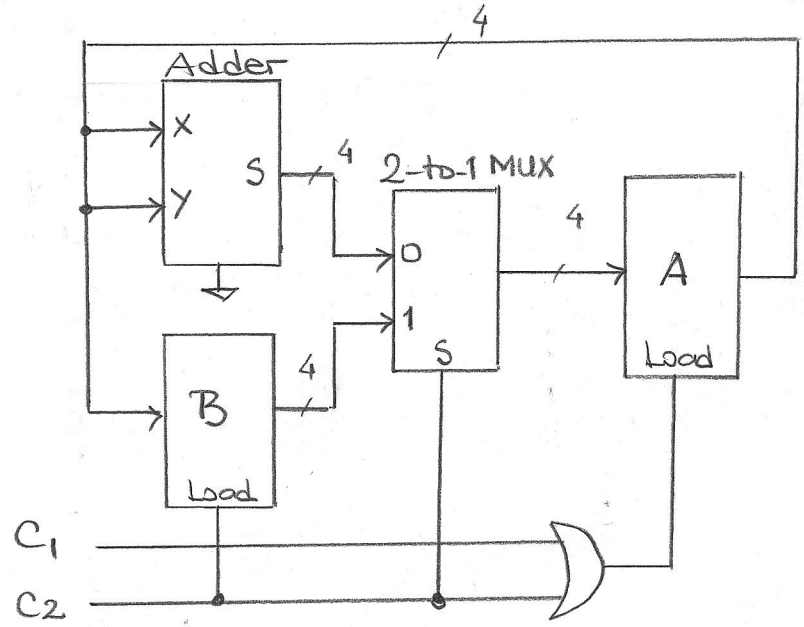
Output Equation: $Z = Y_1 Y_0$

2. Show the diagram of the hardware that implements the register transfer statements

C1: A ← 2A
C2: A ← B, B ← A

Use the register with parallel load and a 4-bit adder. You can also use additional logic gates or functions in the hardware. (30pts)





3. Register A has the following transfer functions:

C1: A←sl A (logical shift left)
C2: A←asl A (arithmetic shift left)
C3: A←sr A (logical shift right)
C4: A←asr A (arithmetic shift right)
C5: A←rol A (rotate left)
C6: A←ror A (rotate right)

A : n-bit register

For the register cell (Ai), find the flip-flop input equation $D_{i,FF}$ using simple approach technique . The control signals are mutually exclusive.(30pts)

$$D_{i,FF} = \overline{LOAD}\, A_i + LOAD \cdot D_i$$

$$LOAD = C1 + C2 + C3 + C4 + C5 + C6$$

$$D_i = (C1 + C2 + C5)\, A_{i-1} + (C3 + C4 + C6)\, A_{i+1}$$

$(i = 1, 2, .. n-2)$

$$D_0 = (C3 + C4 + C6)\, A_1 + C5 \cdot A_{n-1}$$

$$D_{n-1} = (C1 + C2 + C5)\, A_{n-2} + C4\, A_{n-1} + C6 \cdot A_0$$