Name :
Student ID :

Digital Systems II
Midterm II
2009-10 Spring, ~~I./II.~~ Öğretim

27.04.2010
28.04.2010

90 minutes

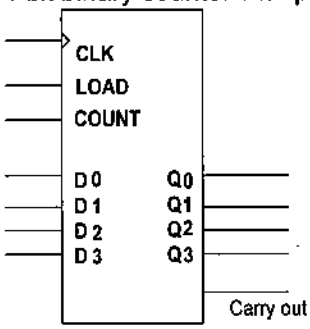
SOLUTIONS

1.
2.
3.
4.

Counter Design

1. Using two 4-bit binary counters of the type shown below and logic gates, construct a binary counter that counts from decimal 20 through decimal 200. Add an additional input to the counter that initializes it synchronously to 20 when the signal INIT is 1. [20pts]

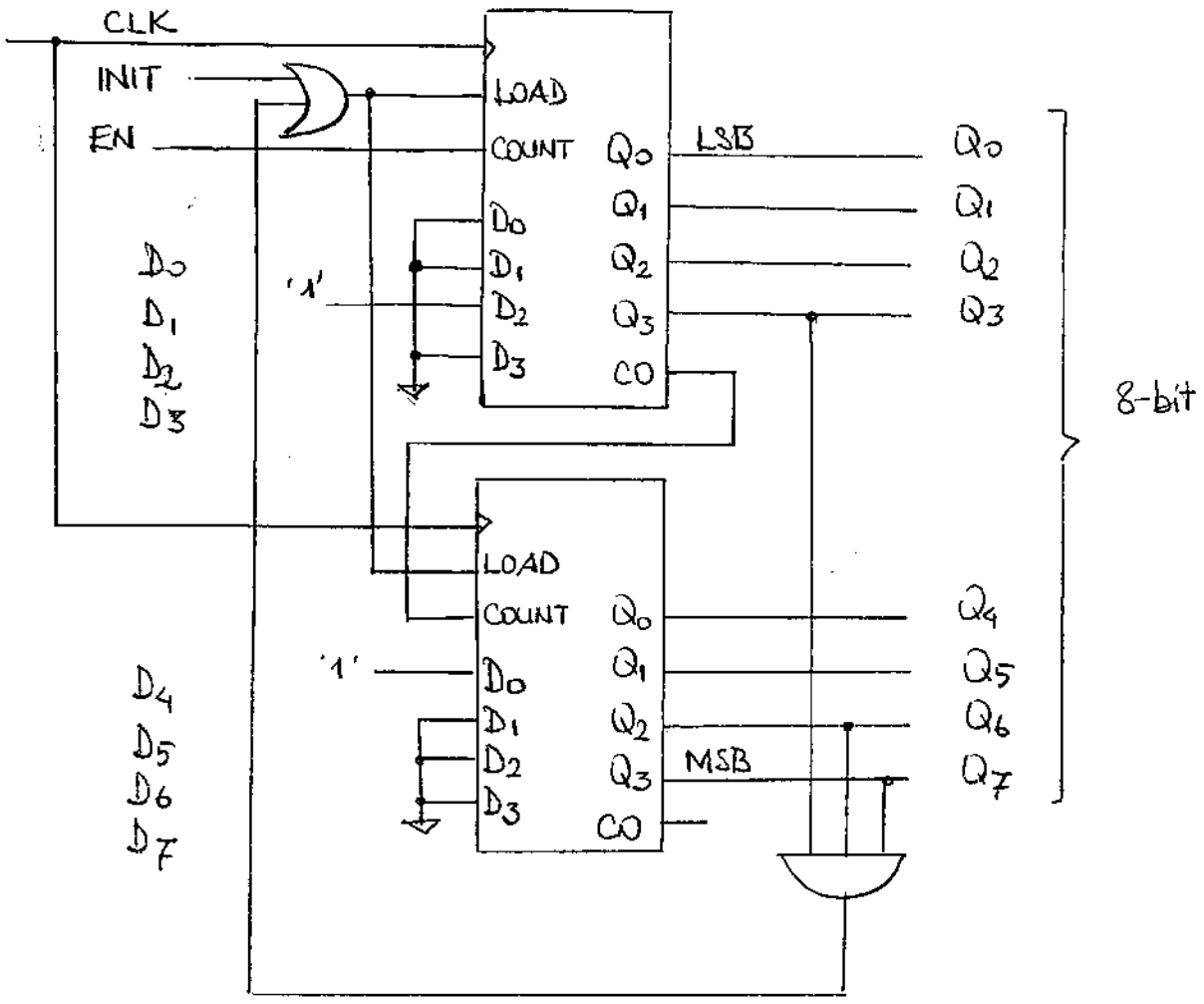
4-bit binary counter with parallel load



$Q_7\ 6\ 5\ 4\ 3\ 2\ 1\ 0$

$(0\ 0\ 0\ 1\ 0\ 1\ 0\ 0)_2 = (20)_{10}$

$(1\ 1\ 0\ 0\ 1\ 0\ 0\ 0)_2 = (200)_{10}$



Register Transfer Structure: Dedicated Multiplexers

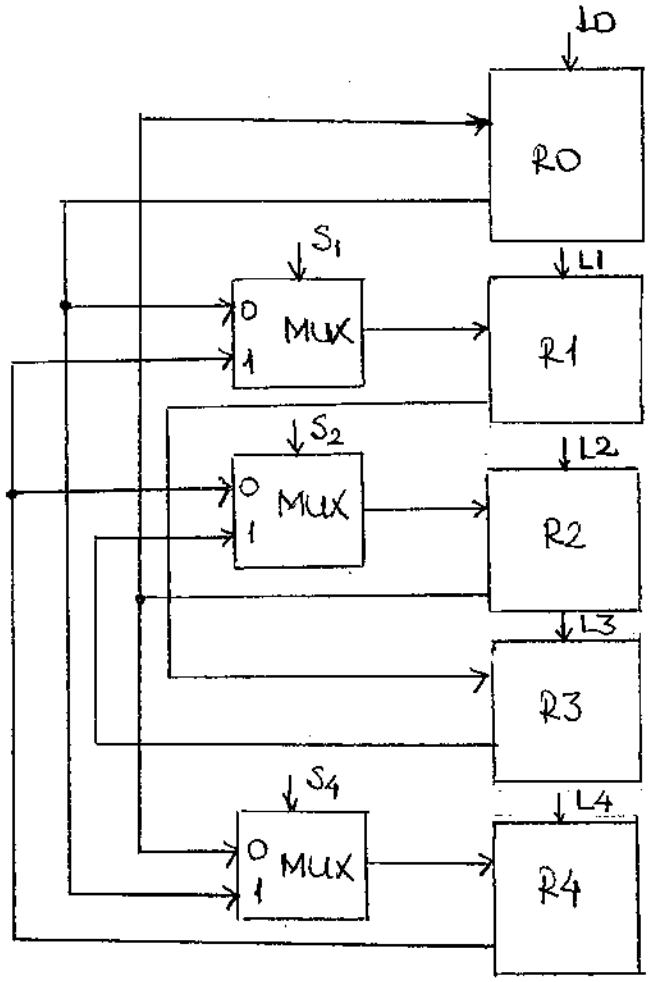
2. A system is to have the following set of register transfers:

$$C_0 : R1 \leftarrow R0$$
$$C_1 : R3 \leftarrow R1, R1 \leftarrow R4, R4 \leftarrow R0$$
$$C_2 : R2 \leftarrow R3, R0 \leftarrow R2$$
$$C_3 : R2 \leftarrow R4, R4 \leftarrow R2$$

a) Using registers and dedicated multiplexers, draw the logic diagram of the system hardware that implements these register transfers. [15pts]

b) Design a simple combinational logic that generates the SELECT signals for the multiplexers and LOAD signals for the register using the control variables C_0, C_1, C_2, and C_3.[15pts]
The control variables are mutually exclusive.

a)



b)

Control Signals				Select			Load				
C_0	C_1	C_2	C_3	S_1	S_2	S_4	LD	L1	L2	L3	L4
0	0	0	0	x	x	x	0	0	0	0	0
1	0	0	0	0	x	x	0	1	0	0	0
0	1	0	0	1	x	1	0	1	0	1	1
0	0	1	0	x	1	x	1	0	1	0	0
0	0	0	1	x	0	0	0	0	1	0	1

$S_1 = S_4 = C_1$
$S_2 = C_2$

$LD = C2$
$L1 = C0 + C1$
$L2 = C_2 + C_3$

$L3 = C1$
$L4 = C1 + C3$

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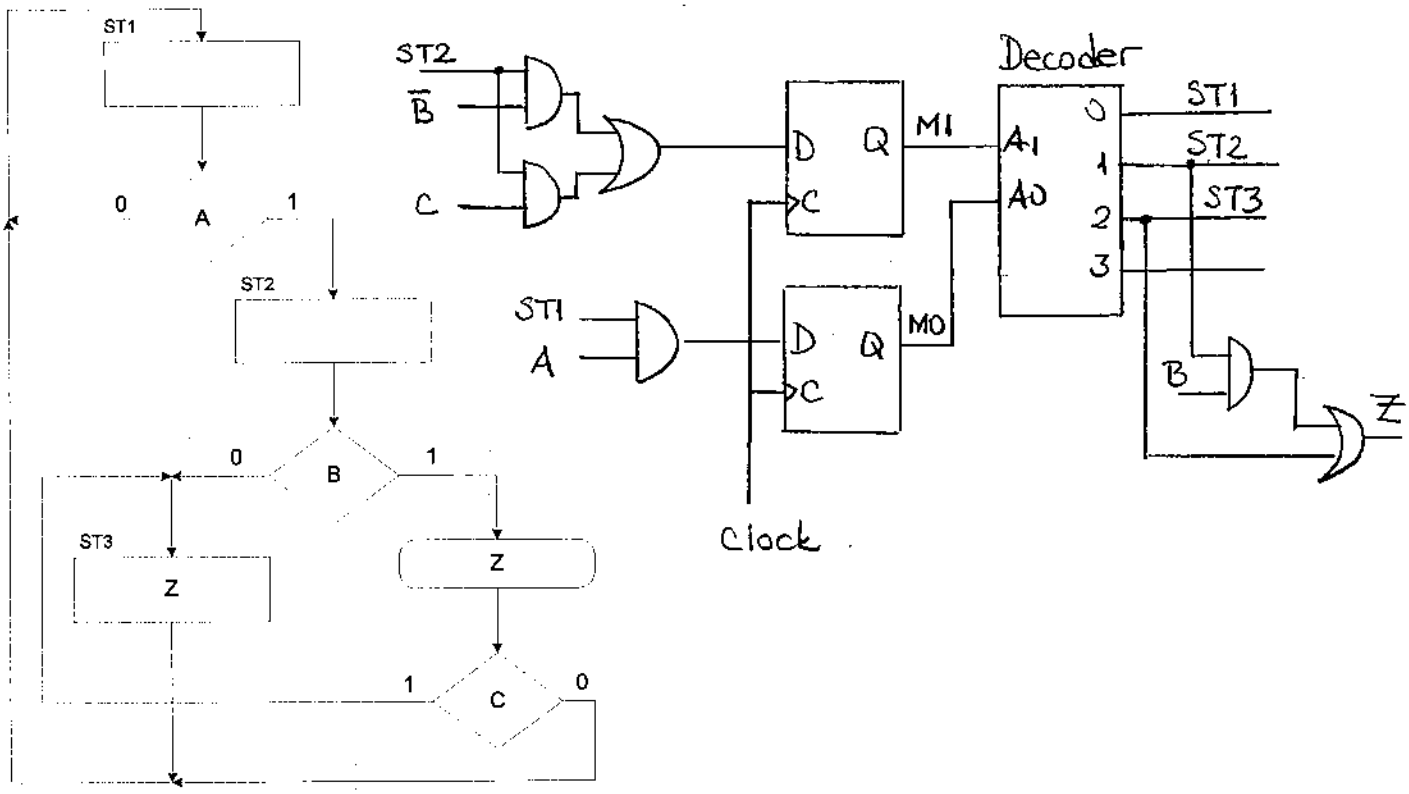
ASM Chart

3. Implement the ASM chart using the sequence register and decoder. The controller has two inputs, A and B, C and one output Z. Draw the logic circuit. [30 pts]



State variables: M1, M0

State Table

	Present State		Inputs			Next State		Decoder Output		
	M1	M0	A	B	C	M1(t+1)	M0(t+1)	ST1	ST2	ST3
ST1	0	0	0	X	X	0	0	1		
	0	0	1	X	X	0	1	1		
ST2	0	1	X	0	X	1	0		1	
	0	1	X	1	0	0	0		1	
	0	1	X	1	1	1	0		1	
ST3	1	0	X	X	X	0	0			1

$D_{M_1} = M1(t+1) = ST2 \cdot \overline{B} + ST2\ B\ C = ST2 \cdot \overline{B} + ST2 \cdot C$

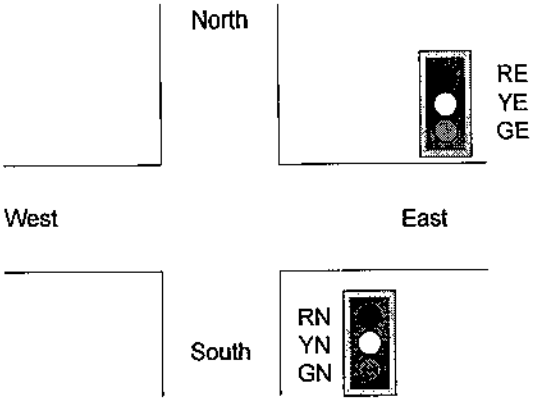
$D_{M_0} = M0(t+1) = ST1 \cdot A$

Controller Design

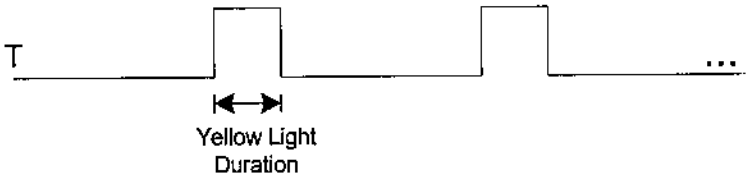
4. Find the ASM chart for a traffic light controller. The controller has one input signal (T) and six Moore type outputs. The timing signal T defines the yellow light interval and also defines the changes of red and green lights. [20pts]

The controller operates as follows:

- If T=0, GN light goes on and RE light goes on.
- With T=1, YN light goes on and RE remains on.
- When T=0, both RN and GE lights go on.
- When T=1, RN remains on and YE goes on.
- The sequence repeats from the beginning.



GN	Green Light, North/South
YN	Yellow Light, North/South
RN	Red Light, North/South
GE	Green Light, East/West
YE	Yellow Light, East/West
RE	Red Light, East/West



Yellow Light Duration