Name :
Student ID :

..... Öğretim

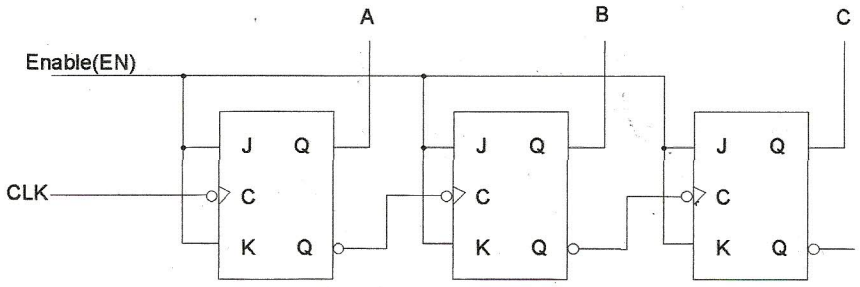
| 1 | 2 | 3 | |
|---|---|---|---|
| | | | |

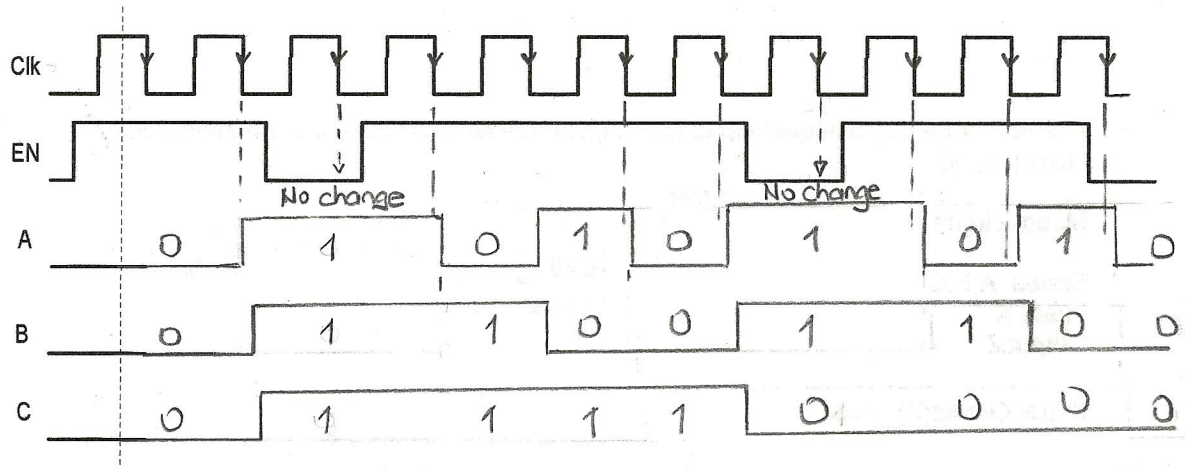
**Digital Systems II**
**Quiz II, 20.04.2010**

**40 minutes**

SOLUTIONS

1. 3-bit ripple counter is shown below. If the enable input is as shown in the timing diagram, sketch the flip-flop outputs A, B, and C. Find the binary count sequence (CBA) of the counter. Is it up or down counter? Assume that flip-flops are initially reset, i.e. A=B=C=0. [40pts]




Down counter 111 → 110 → 101 → ... 001 → 000

2. Design a binary counter.
   a. Use D flip-flops and gates to design the binary counter with the following repeated binary sequence: 0,2,4,6. The next state of unused states will be taken as don't care.[20pts]

| PS | | | NS | | |
|---|---|---|---|---|---|
| A | B | C | A(t+1) | B(t+1) | C(t+1) |
| 0 | 0 | 0 | 0 | 1 | 0 |
| 0 | 0 | 1 | X | X | X |
| 0 | 1 | 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | X | X | X |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | X | X | X |
| 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | X | X | X |

| A \ BC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | X | X | 1 |
| 1 | 1 | X | X | 0 |

$A(t+1) = A \oplus B$

| A \ BC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 1 | X | X | 0 |
| 1 | 1 | X | X | 0 |

$B(t+1) = \overline{B}$

The LSB bit of even number is 0, so two flip-flop are enough to generate even number sequence: 0, 2, 4, 6.

**b.** Using the flip-flop equations found in part (a), find the next state of the unused states.[10pts]

Unused States

| A | B | C |
|---|---|---|
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

In the design, C output of the counter is always zero. Therefore the unused states never occur in this design.

**3.** A state diagram of a sequential circuit is given below. Find the corresponding ASM chart.[30pts]

Moore circuit

States: A,B,C
Input: X
Output:Z.

State/ Output(Z) : A/0