Name **April 07, 2005**
Student ID:

Digital Systems II (A-B), Midterm I

90 minutes

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1. Consider the state table that represents a sequential circuit with one input X and one output Z.

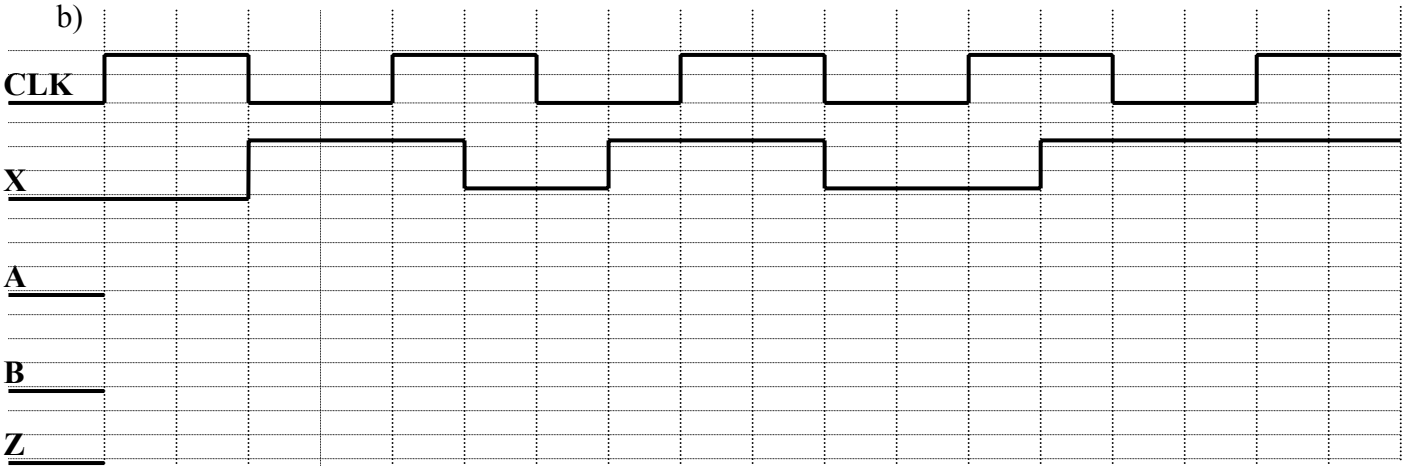
a) Is this a Moore or Mealy machine? Explain briefly. (03 pts)

b) Sketch the waveform for the flip-flop outputs **A** and **B** referring to the state table. Assume that A=B=0 and the output Z=0 initially. The flip-flops are triggered at the positive edge. (12 pts)

a)

Present State		Next State				Output
		X=0		X=1		
A	B	A	B	A	B	Z
0	0	0	0	0	1	0
0	1	0	1	1	0	1
1	0	1	1	1	0	1
1	1	0	0	1	0	0

b)



2. A JN flip-flop has two inputs J and N. Input J behaves like the J input of JK flip-flop. N behaves like the complement of the K input of JK flip-flop (that is N=K).

a) Obtain the characteristic table of JN flip-flop. (07 pts)

b) Derive the excitation table of the flip-flop.(08 pts)

3. Design a sequence detector with one input **X** and one output **Z**. Every time the input "**1 0 1**" is detected the output **Z=1**. However, the detector needs to be first activated with a key, i.e. it has to receive at least three consecutive 0's before it will start detecting the desired sequence "1 0 1". Once the key has been received, the sequence detector keeps looking for the desired sequence. Overlapping sequences are allowed.

a) For the following input sequence give the output sequence (05 pts)

X:	0	1	0	1	1	0	0	0	0	0	1	1	0	1	0	0	1	0	1	0	1	0	0	0	0	1	0	1
Z:																												

b) Give the state diagram of the sequence detector including the key detection. Assume that the circuit is a Mealy machine. (20 pts)

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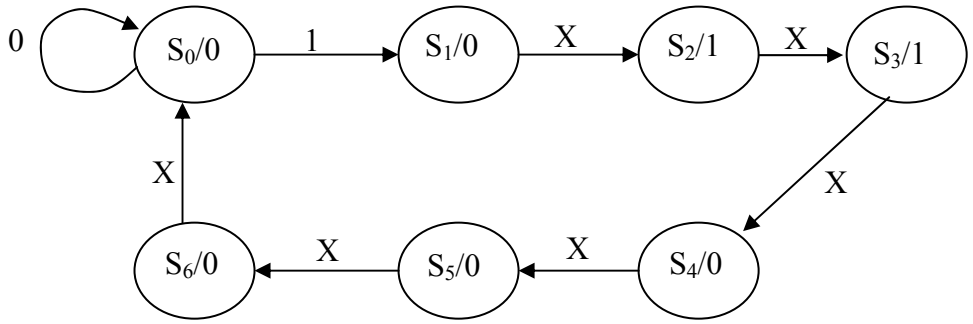
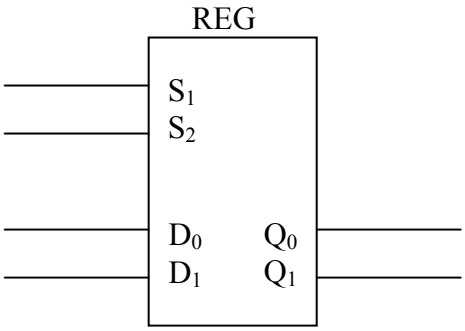
4. Consider the following state diagram that represents a sequential circuit with one input **X** and one output **Z**. Design the circuit with D flip-flops. Give the state table, derive the logic equations for the inputs to the flip-flops and for the output function. Assume that the states are encoded as follows: S_0(000), S_1(001), S_2(010), S_3(011), etc. X: don't care (25 pts)



5. Draw the logic diagram of a 2-bit register with mode selection inputs S_1 and S_2. The register is to be operated according to the following function table:

S_1	S_2	Register Operation
0	0	No change
0	1	Clear register to 0
1	0	Load parallel data
1	1	Complement output



Use JK flip-flops in the register. Use only the inputs J and K to perform the listed operation. (20 pts)