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Osmangazi University
Electrical and Electronics Engineering Department
Digital Systems II (A-B)
Midterm II May 18, 2005

105 minutes

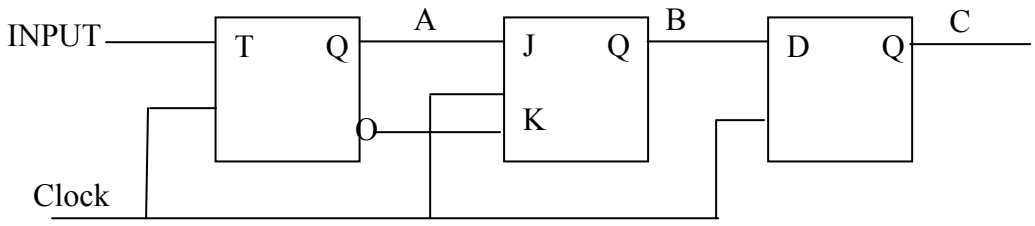
1. Draw the logic diagram of a 3-bit register with mode selection inputs S_1 and S_2. The register is to be operated according to the following function table: [20 pts]

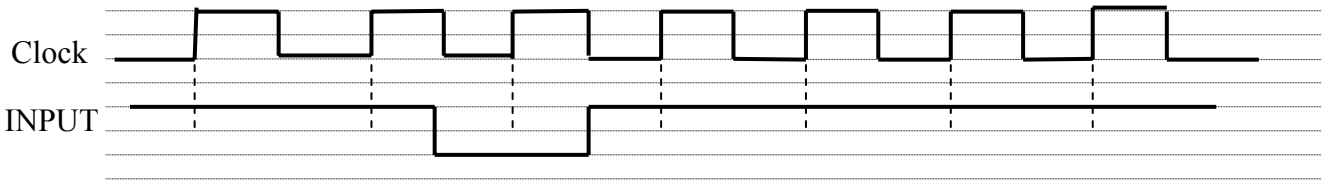
S_1	S_2	Register Operation
0	0	No change
0	1	Clear register to 0
1	0	Load parallel data
1	1	Count Up

Use synchronous binary up counter to implement the count up operation. For an n-bit synchronous binary up counter, the input equations of JK flip-flops are expressed as follows:

$$J_{Q0} = K_{Q0} = 1,\ J_{Q1} = K_{Q1} = Q_0,\ J_{Q2} = K_{Q2} = Q_0 \cdot Q_1$$
$$J_{Qi} = K_{Qi} = Q_0 \cdot Q_1 \cdot Q_2 \cdot \ldots\ldots \cdot Q_{i-1} \quad i=1,2,\ldots,n$$

2. For the following circuit





a) Determine the output sequence for A, B, and C when the input sequence is 110111. All flip-flops are initially reset 0. [10pts]

b) If C is connected back to INPUT, the circuit can be considered as a counter, of which ABC is the count. Find its possible counting sequences, assuming that the counter starts in ABC=001 state. [10pts]

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3. a) Consider a 4096x8 RAM chip. The chip is organized as a square array and uses 2-dimensional internal organization, row and column decoding (coincident decoding). How many address bits are required for the row and column decoders? [05 pts]

   b) Show the logic diagram that implements 64Kx8 RAM module using 32Kx4 RAM chips. In the diagram include the connection between all the memory chips and other chip that is needed. Indicate the address and data lines, the chip select (CS), Read/Write (R/W) and data I/O lines, and also indicate the bus width. [15 pts]

4. a) Given the 11-bit data word 00101101011, generate the corresponding 15-bit Hamming code word. [05pts]

b) How many parity check bits must be included with the data word to achieve single error correction and double error detection when the data word contains 16-bit. [05pts]

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5. Using two 4-bit registers R1 and R2, and AND gates, OR gates and inverter, draw <u>one bit slice</u> of the logic diagram that implements the following statements:

$C_0 : R0 \leftarrow 0$ Clear $R0$ synchronously with the clock

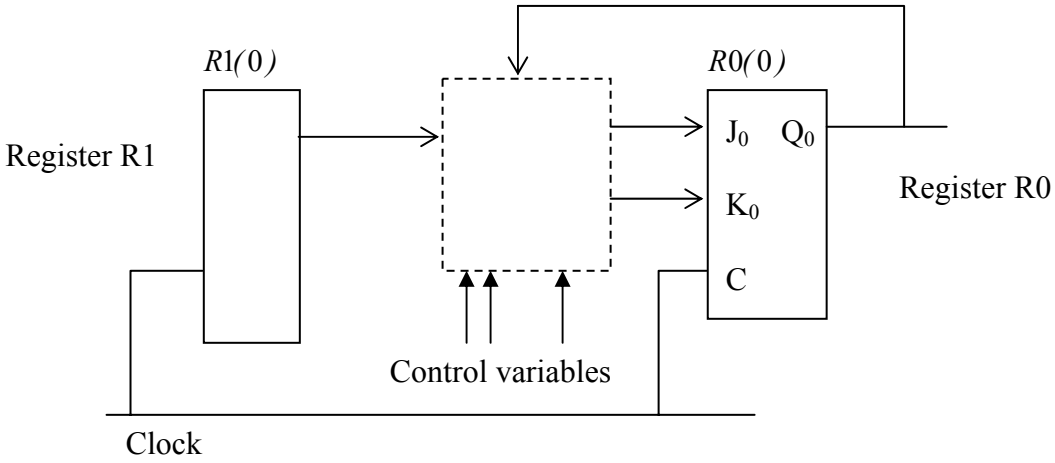
$C_1 : R0 \leftarrow R1$ Transfer $R1$ to $R0$

$C_2 : R0 \leftarrow \overline{R}0$ Complement $R0$

$C_3 : R0 \leftarrow R0 \wedge R1$ Logical bitwise AND

C_i represents the control variable.

<u>The control variables are mutually exclusive; i.e., only one variable can be equal to 1 at any time, while the other three are equal to 0</u>. [15 pts]



6. The register transfer statement

$$C_1 : R0 \leftarrow R1, \quad \overline{C}_1 C_2 : R0 \leftarrow R2$$
$$R0, R1, R2 : n\text{-}bit\ register$$

will be implemented with the hardware that uses either multiplexer-based transfer or bus-based transfer. Show the logic diagrams of the hardware belonging to the multiplexer-based and the bus-based transfer.
Hint: for bus-based transfer, use n-bit the registers with three-state outputs. [15pts]