EXPERMENT 1 : TTL Gate Characteristics

OBJECTIVES

- To observe the transfer characteristics of TTL gates.
- To investigate various logic gate characteristics, including voltage levels, noise margin and propagation delay.

APPARATUS

74LS04 Hex inverter

Connection wires or Jumper wires, Wire Stripper / Cutter

Multimeter

INTRODUCTION

Standard commercially available digital logic gates are available in two basic families or forms, TTL which stands for *Transistor-Transistor Logic* such as the 7400 series, and CMOS which stands for *Complementary Metal-Oxide-Silicon* which is the 4000 series of chips. This notation of TTL or CMOS refers to the logic technology used to manufacture the integrated circuit, (IC) or a "chip" as it is more commonly called. Generally speaking, TTL logic IC's use NPN and PNP type Bipolar Junction Transistors CMOS logic IC's use complementary MOSFET or JFET type Field Effect Transistors for both their input and output circuitry.

A ***voltage transfer curve*** is a graph of the input voltage to a gate versus its output voltage. Voltage transfer curve of a TTL inverter is given in figure 1.

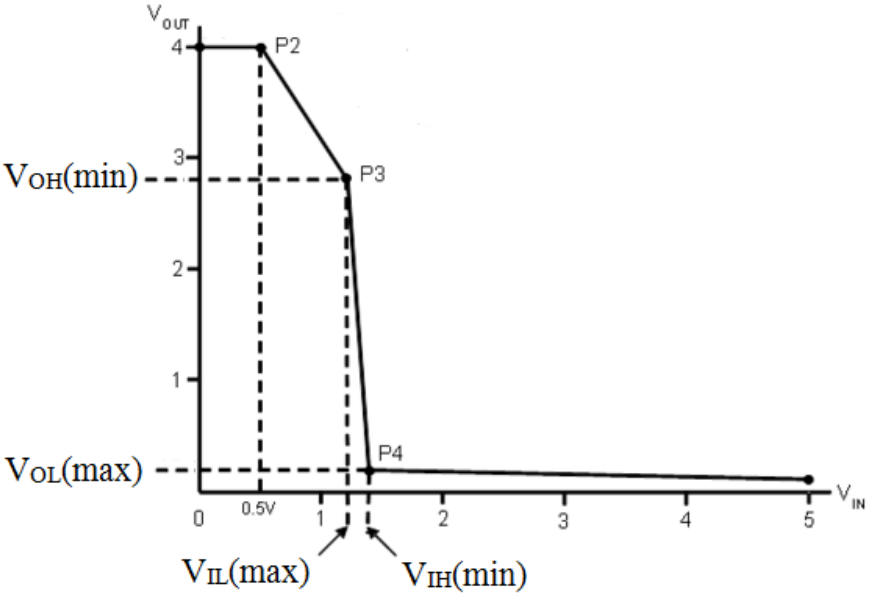

Figure 1

For the TTL family ***voltage levels***, theoretically, the low state is 0 V and high sate is 5 V. But practically, this ideal situation never occurs and a range of voltage is defined to recognize each of the logic states. These voltage ranges are explained below.

- Any voltage from 0 V to V_{IL}(max) V is recognized by the TTL gates as the low input level range without changing the output.
- Any voltage from V_{IH}(min) V to 5 V is recognized by the TTL gates as the high input level range without changing the output.
- Logic low output voltage level must be within 0 V to V_{OL}(max) V.
- Logic high output voltage level must be within V_{OH}(min) V to 5 V.

Hence, as far as the TTL output is concerned, any voltage from V_{OL}(max) V to V_{OH}(min) V is undesirable and leads to an unpredictable output state. A low voltage greater than V_{IL}(max)and a high voltage lower than V_{IH}(min) are not desirable at the input and lead to unpredictable output at the TTL gates.

The term noise denotes any unwanted signal that causes the change in the input voltage level. ***Noise immunity*** or ***the noise margin*** is the limit of noise voltage that may appear at the input of the logic gate without any impairment of its proper logic operation. Noise margin values can be calculated as;

V_{NL} = LOW level noise margin = V_{IL}(max) - V_{OL}(max)
V_{NH} = HIGH level noise margin = V_{OH}(min) - V_{IH}(min)

These TTL noise margins are illustrated in figure 2.

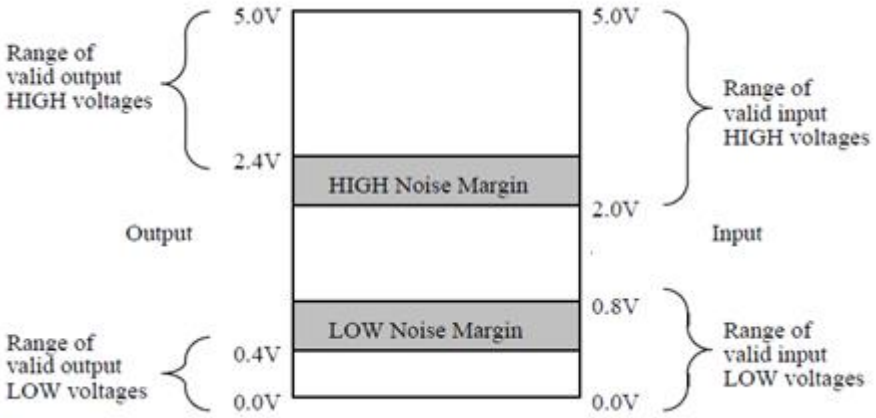

Figure 2

Propagation delay is defined as the time taken for the output of a logic gate to change after the inputs have changed. The delay times are measured by time elapsed between the 50% voltage levels of the input and the output waveforms while making the transition (see figure 3). Two types of propagation delay times are defined as:

t_{PLH} = propagation delay when the OUTPUT switches from LOW to HIGH.
t_{PHL} = propagation delay when the OUTPUT switches from HIGH to LOW.

In general, the t_{PLH} and t_{PHL} are not necessarily equal and will vary depending on load conditions. The average of the two propagation is called *the average delay* and this parameter is used to rate the circuit.

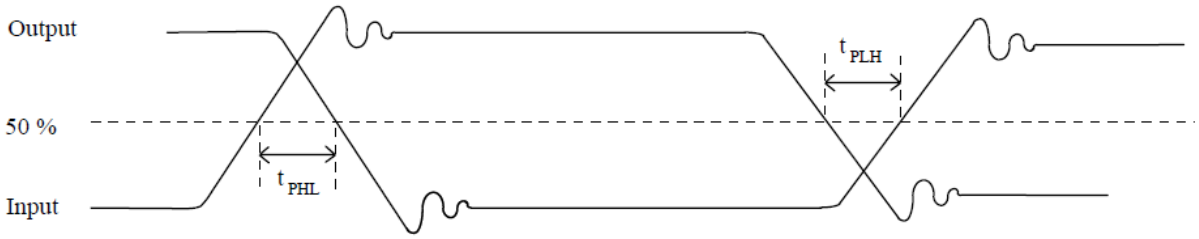

Figure 3

PROCEDURE

1- Construct Circuit given in figure 4. Increase the input voltage, V_{IN} from 0V to 5V by the values given in steps of 0.1 V and record the output voltage V_{OUT} in each case. Do not increase the voltage above 5V or you may destroy the IC. Using the data from the table, draw the voltage transfer characteristic of the inverter.

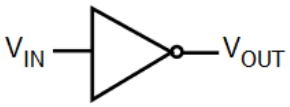

Figure 4

2- By using the voltage transfer curve, determine the voltage levels V_{IL}(max), V_{OL}(max), V_{OH}(min) and V_{IH}(min). Then calculate the noise margins for this gate.

3- Construct Circuit given in figure 5. Set V_{IN} 100 kHz 0 – 5 V squarewave. View both waveforms A and B on the oscilloscope with channel1 and channel 2, respectively. Then measure t_{PLH} and t_{PHL}. Also sketch the waveforms seen on the oscilloscope.

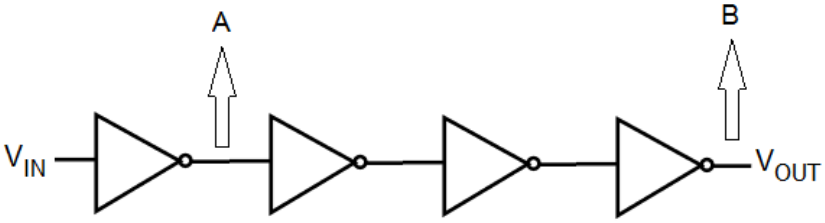

Figure 5