EXPERIMENT 4 : Synchronous Sequential Circuits

OBJECTIVES

- To design, build and test synchronous sequential circuits.

APPARATUS

7404 hex inverter
7474 dual positive edge triggered D flip-flops
7486 quad 2-input XOR gate
74HC14 schmitt-trigger hex inverter
470 ohm, 10 Kohm Resistors
100 nf Capacitor
Connection wires or Jumper wires, Wire Stripper / Cutter
Push Button

PRELIMINARY WORK

Q1. Design a synchronous sequential circuit with one input x, and one output z. When x=1, this circuit goes through the following repeated binary state sequence: … 00, 01, 11, 10, 00, 01... When x=0, this circuit goes through the following repeated binary state sequence: … 00, 10, 11, 01, 00, 10... The output z=1 if the present state is either 00 or 11.

a. Draw the state diagram of the sequential circuit. Is it a Moore or Mealy machine? Explain your answer.
b. Obtain the state table for the given circuit.
c. Design this circuit by using D flip flops and external gates. Draw the logic circuit.

Q2. Design a 4 bit BCD counter by using D flip flops.

a. Draw the state diagram of the sequential circuit.
b. Obtain the state table for the given circuit (take the unused states as don't cares).
c. Design this circuit by using D flip flops and external gates.

IC DESCRIPTION

The ***7474*** IC contains two independent positive-edge-triggered D flip-flops with complementary outputs. The pin assignment is shown in Fig 7. The information on the D input is accepted by the flip-flops on the positive going edge of the clock pulse. A low logic level on the preset or clear inputs will set or reset the outputs regardless of the logic levels of the other inputs. Effects of the mode select inputs are given in table 5.

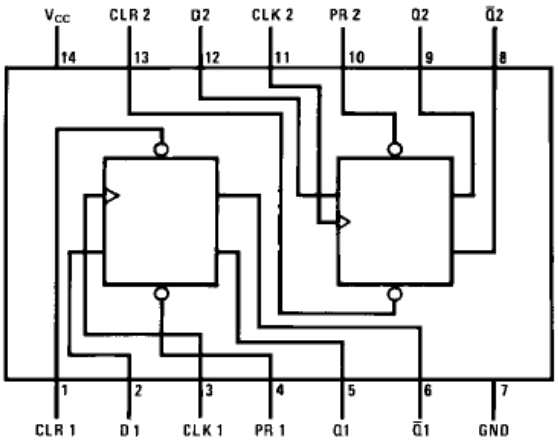


Figure 7

Table 5

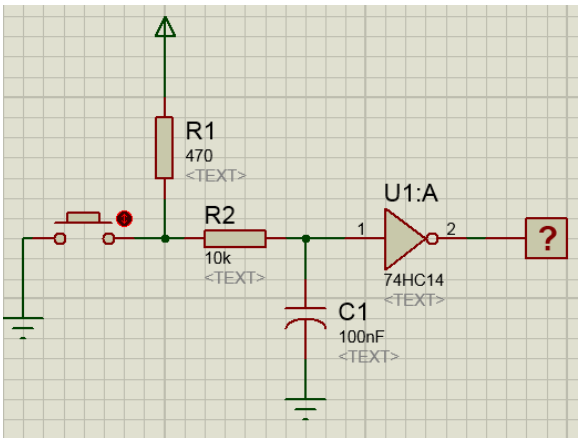
Inputs				Outputs	
PR	CLR	CLK	D	Q	$\overline{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	$\overline{Q}_0$

H = HIGH Logic Level
X = Either LOW or HIGH Logic Level
L = LOW Logic Level
↑ = Positive-going Transition
Q_0 = The output logic level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when either the preset and/or clear inputs return to their inactive (HIGH) level.

PROCEDURE

1. Set up the push button circuit given below and connect it to a led. Then check whether it is working or not.



2. Build the sequential circuit you designed in prelab Q1 by using IC 7474 and external gates (if it is required). Use the push button you build in procedure 1 as clock signal. Also connect the flip flop outputs to the leds to verify the counting sequences.