Lab 7: Introduction to Logic Design With Xilinx ISE

Objectives

- To get familiar with the combinational logic design with Xilinx ISE.

.

INTRODUTION

The Xilinx ISE tools allow you to use schematics, hardware description languages (HDLs), and specially designed modules in a number of ways. In this lab, you will learn how to enter verilog description of a combinational logic circuit and test your HDL definition in Xilinx ISE. Please check the link following for more information about Xilinx ISE http://www.xilinx.com/products/design-tools/ise-design-suite/ise-webpack.htm
While you are entering verilog description of a combinational logic circuit and test your HDL definition in Xilinx ISE, three main steps should be followed:

- STEP-1: Creating a new project
- STEP-2: Design entry
- STEP-3: Simulating your design

PART-1: Creating A New Project

From Project Navigator, select the following;

- *File → New Project*

The New Project Wizard appears. You are prompted to enter a project name, a project location, and a top level module type, as shown in Figure 1. You may change the project location to another folder if you wish. Do not use file or folder names that contain spaces. Select ***HDL*** as the ***Top-Level Source Type***. When you are satisfied with the project name and location, click “Next”.

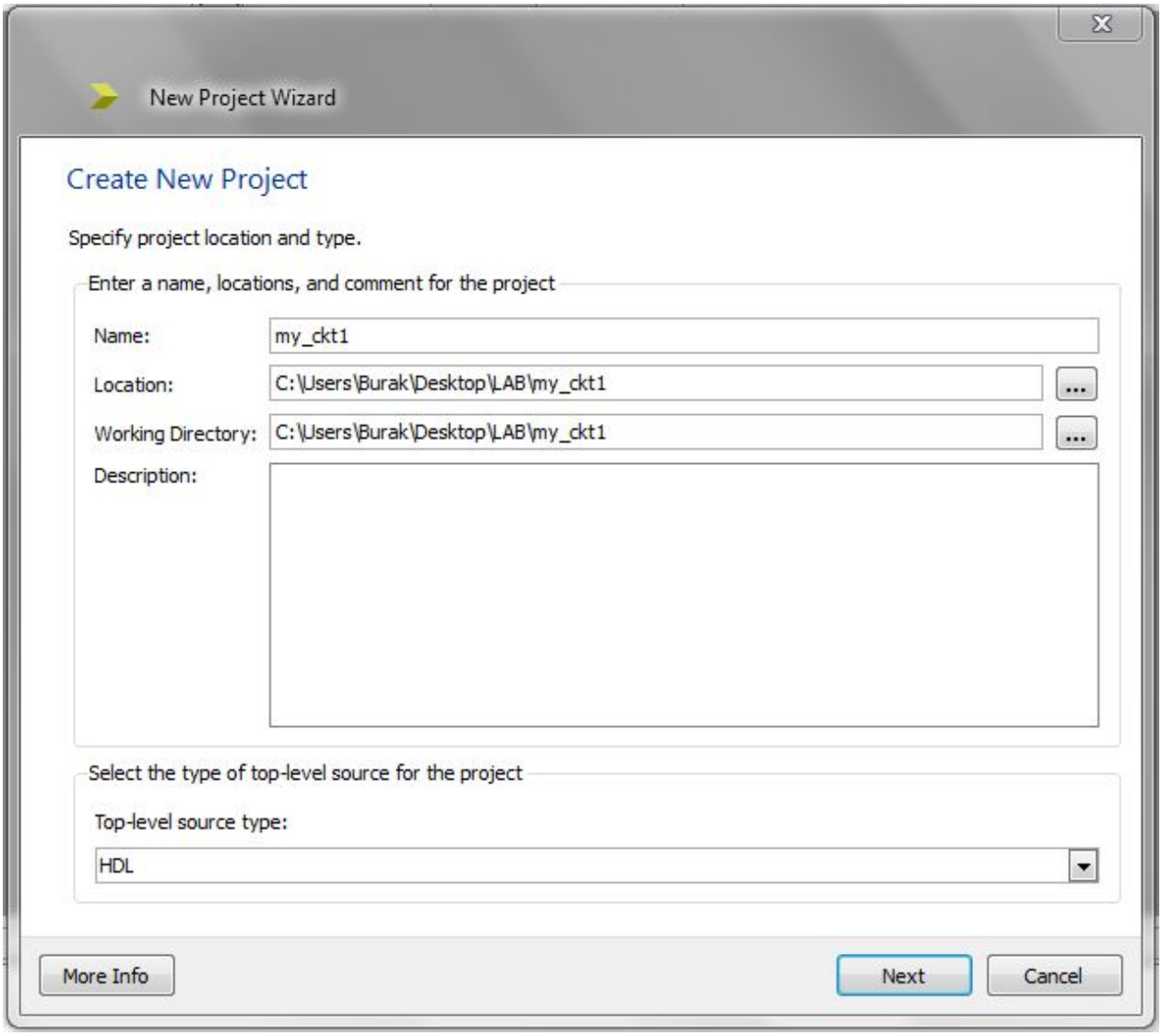

Figure1: New Project Wizard

The next dialog allows you to set additional project options. The first group of settings are related to hardware targets and they are not very important for you at this stage since you will not perform any hardware applications in the lab.. The second group of settings represents the design entry language, synthesis tool, and simulator preferences. As it is given in figure 2, Select ***Verilog*** as the ***Preferred Language*** and select ***ISim*** as the ***Simulator*** and then click “Next”.

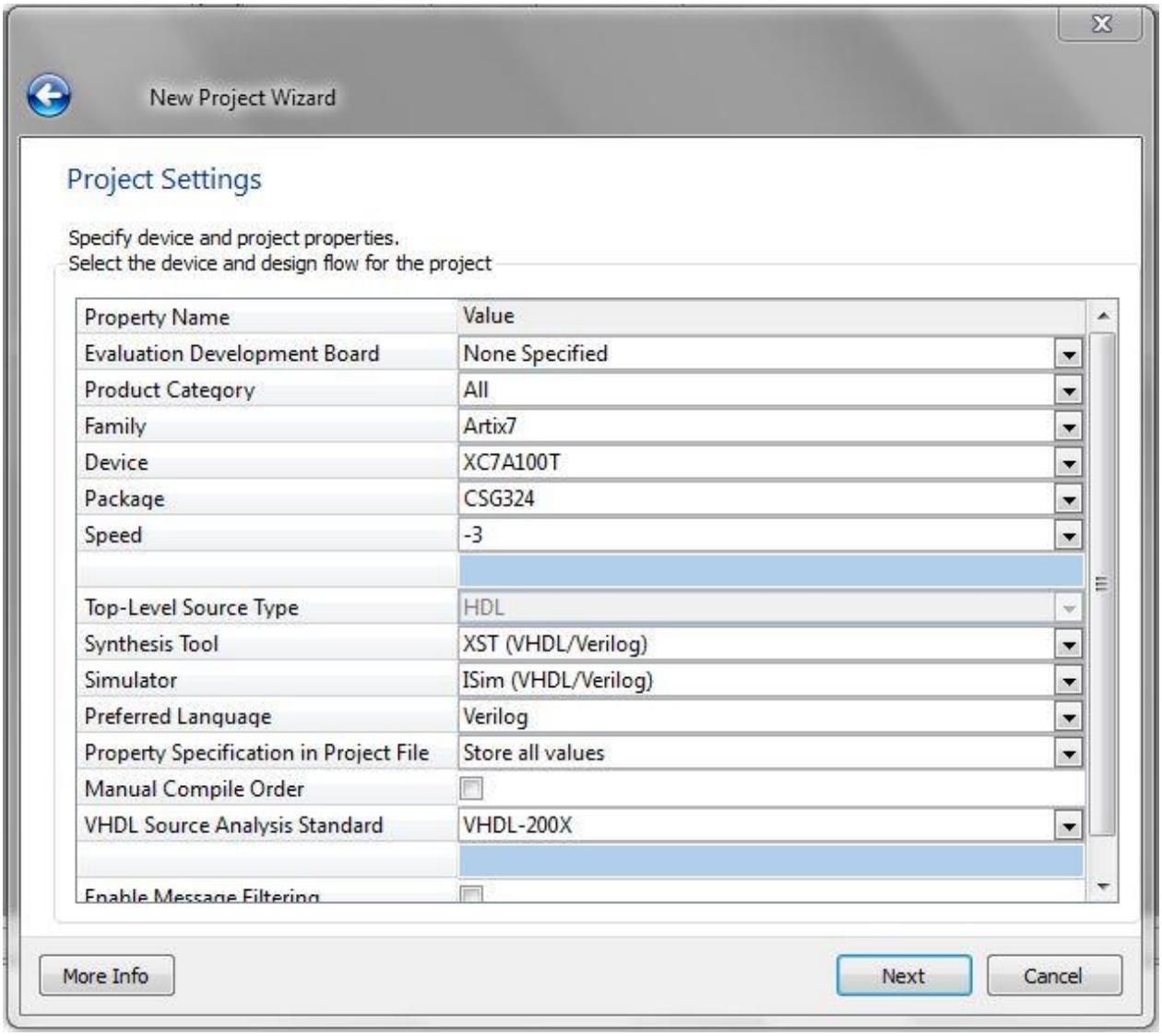

Figure 2: New Project Wizard - Device Properties

The final dialog box in the new project process, provides a summary of the project that Project Navigator will create based on your settings. Review the summary to make sure it matches what is shown in the dialog box. If it does not, go “Back” and correct any errors. Otherwise, click “Finish” to complete this process.

PART-2: Design Entry

At this point, the project has been created but it does not contain any source files. In order to make a new schematic, in the project navigator window select the following

- *Project → New Source*

The New Source dialog box opens: In the pop-up window, click the '**Verilog Module**' to indicate you are creating a module by using Verilog HDL. Then, provide a file name as shown in Figure 3. You should not need to change the specified location, which should be inside the project directory you created earlier. Make sure the **'Add to project'** item is **checked**, then click 'Next'

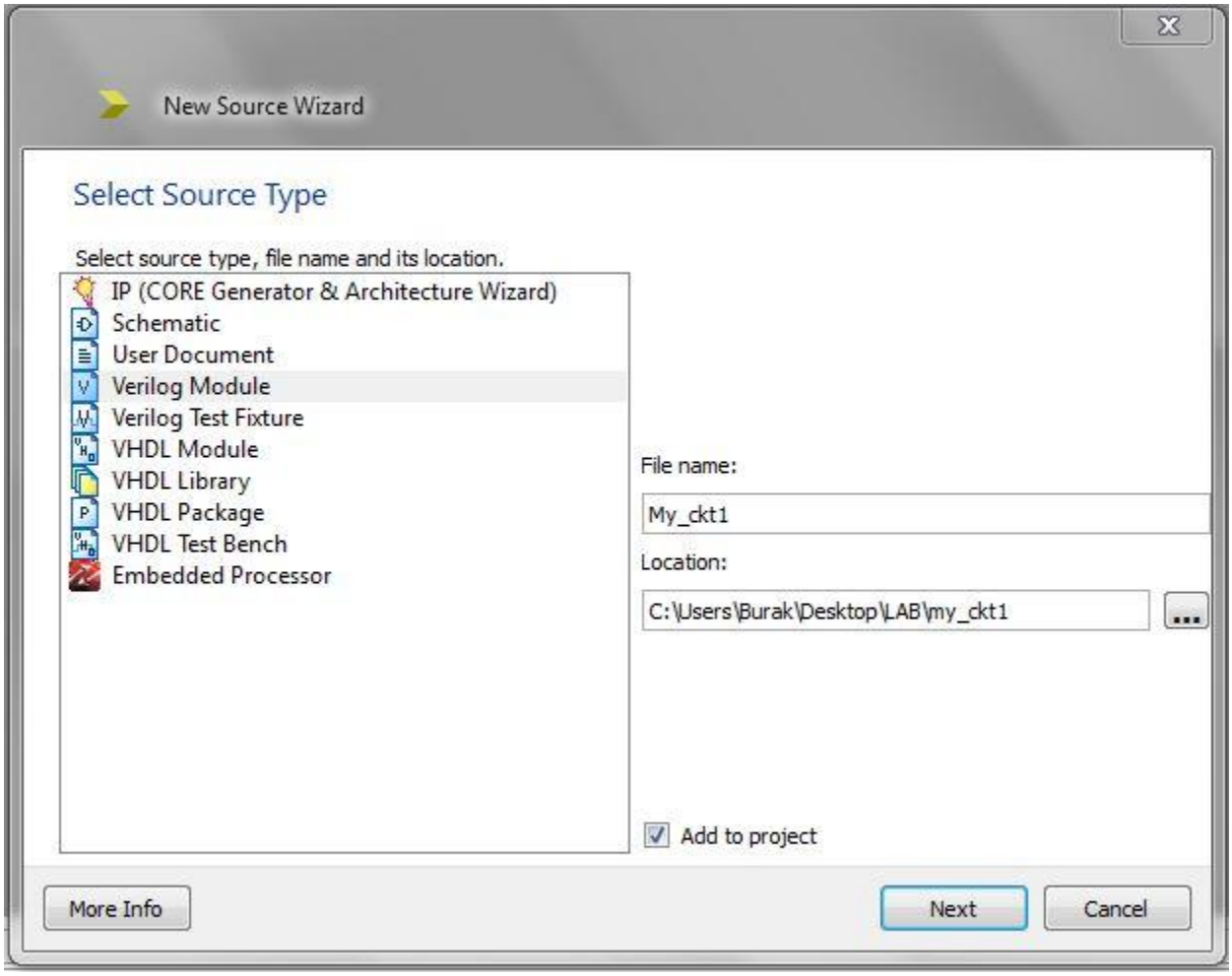

Figure 3: New Source Dialog Box

The next dialog optionally allows you to specify the ports of the module. This may also be done in the text editor, when creating the module, so skip it at this stage. Simply click “Next”.

The final dialog box in the new source process, provides a summary of the source that Project Navigator will create based on your settings. Review the summary to make sure it matches what is shown in the dialog box. If it does not, go “Back” and correct any errors. Otherwise, click “Finish” to complete this process. After clicking “Finish”, the new source file will be automatically opened in the text editor as it given in figure 4.

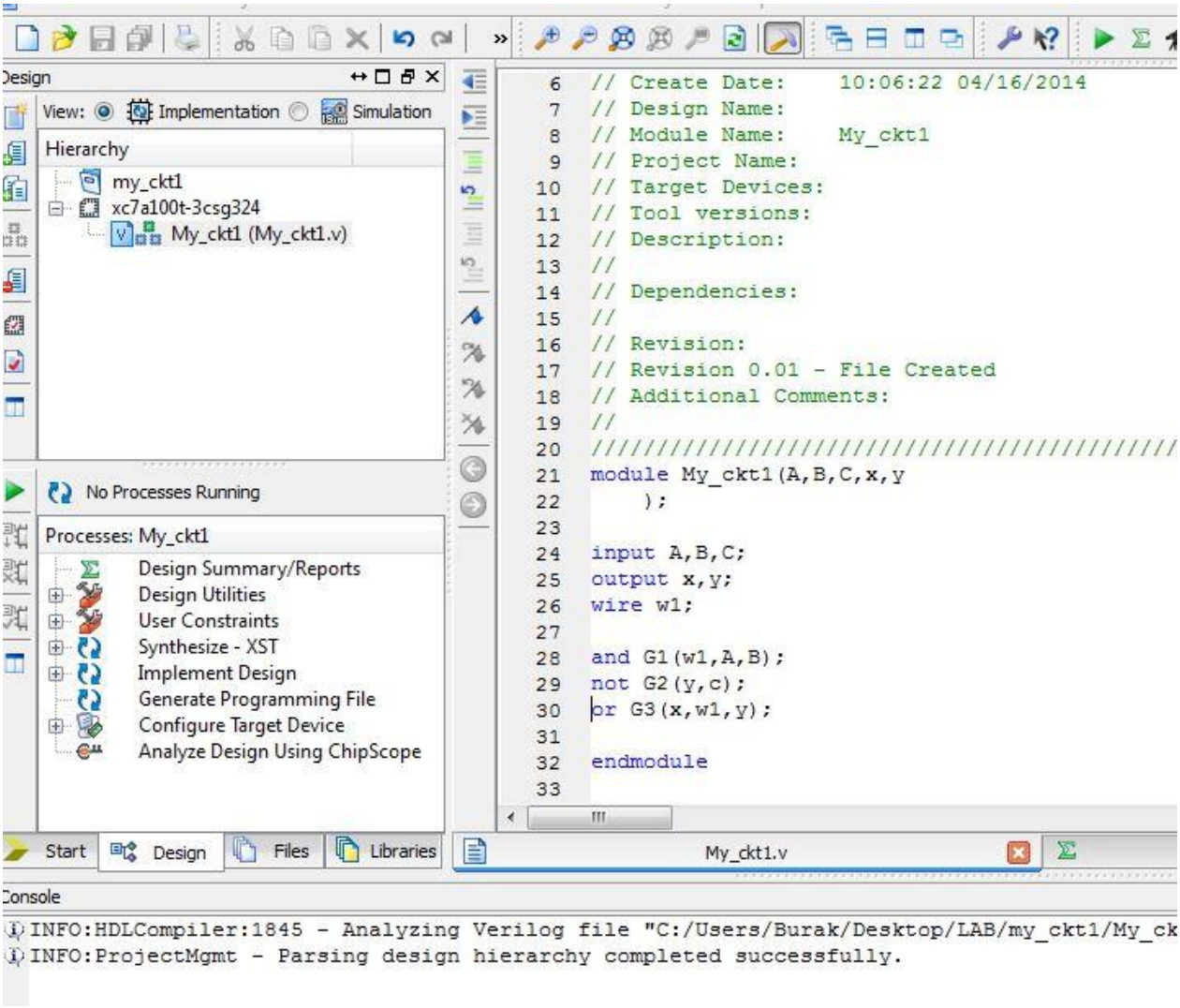

Figure 4: Completed Design

In the text editor, some of the basic file structure is already in place. Keywords are displayed in blue, data types in red, comments in green, and values in black. This color-coding enhances readability and recognition of typographical errors. Now, enter the verilog HDL description of the combinational circuit given in prelab question 1.

At this point, you should end up with a window that looks somewhat like that shown in Figure 10. Once you are satisfied, save the file and close the window. It is a good idea to get in the habit of saving your project. There are options on the main menu to save individual files or the complete project.

STEP-3: Simulating your design

Functional simulation is done before the design is synthesized to verify that the logic you have created is correct. This allows a designer to find and fix any bugs in the design before spending time with subsequent steps. Project Navigator provides an integrated flow with the Xilinx ISE simulator that allows simulations to be run from the Project Navigator. In order to simulate the design, a test bench is required to stimulate the design. First create a new source file for the test bench.

- *Project → New Source*

The New Source dialog box opens: In the pop-up window, click the '**Verilog Test Fixture**' to indicate you are creating a test bench file. Then, provide a file name as shown in Figure 5. You should not need to change the specified location, which should be inside the project directory you created earlier. Make sure the **'Add to project'** item is **checked**, then click 'Next'

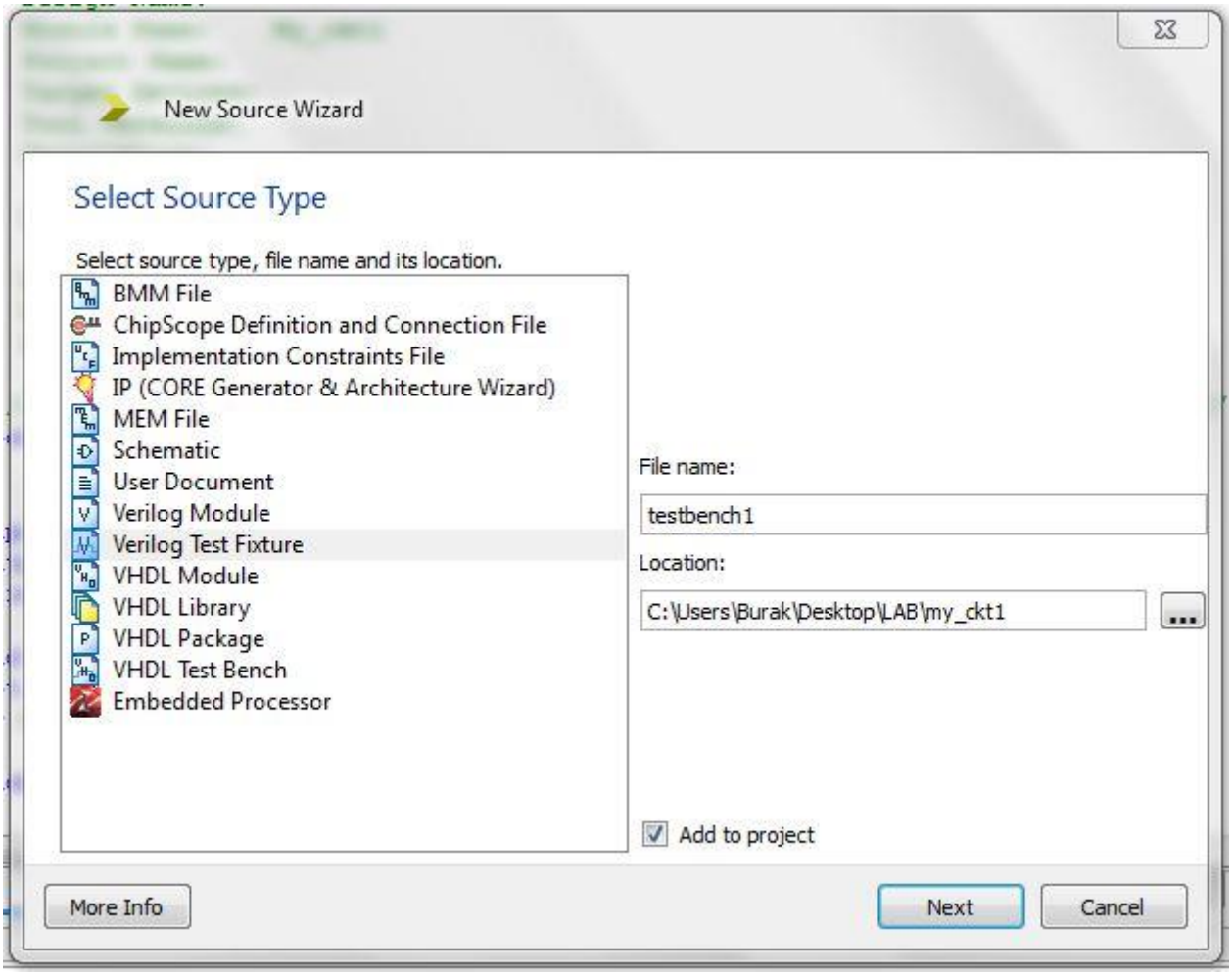

Figure 5: New Source Dialog Box

The second dialog, shown in Figure 6, asks you to identify a design module with which the test bench should be associated. Select the module you designed at previous step as shown and click “Next”.

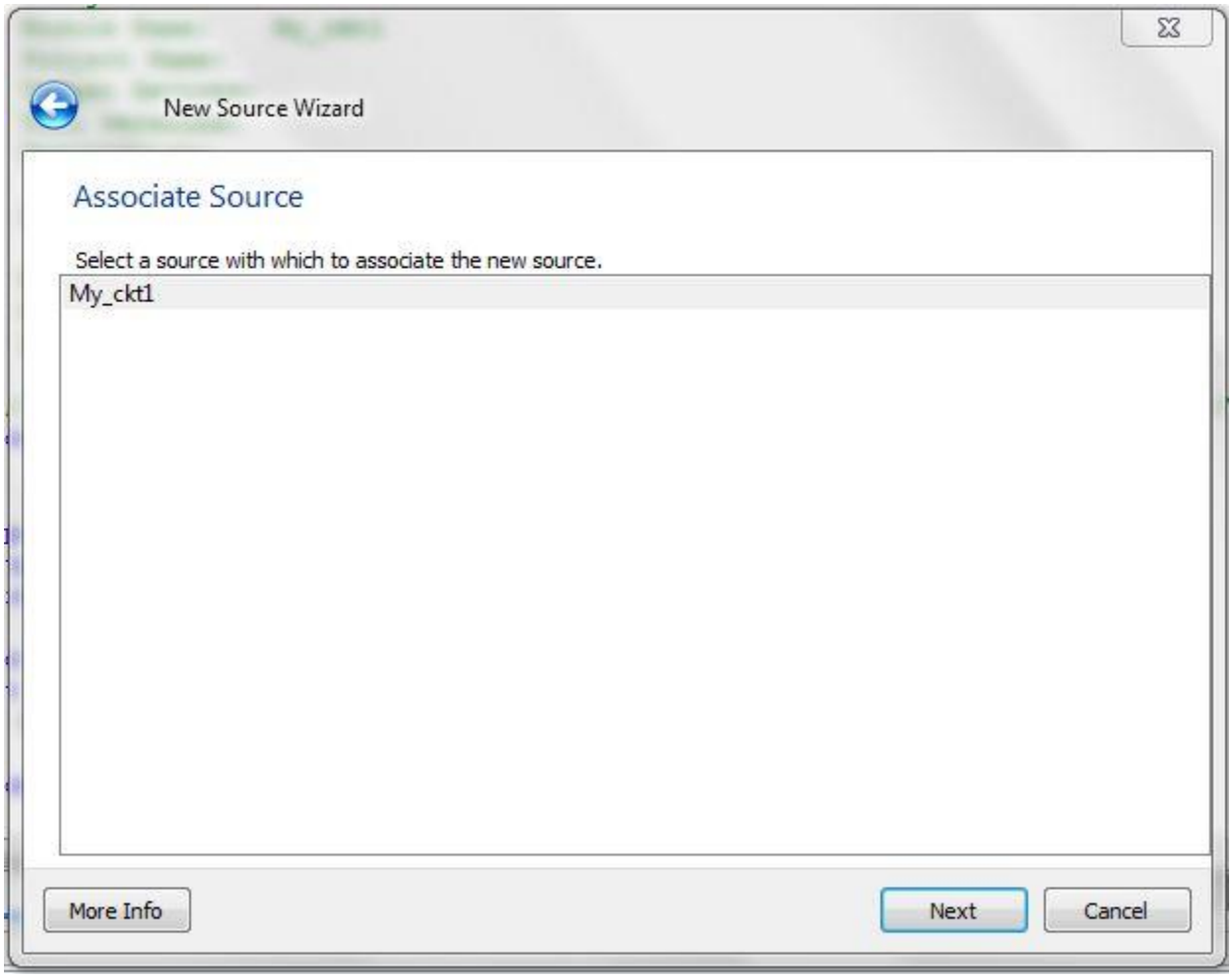

Figure 7: New Source Dialog Box – Associating source file

The final dialog box provides a summary of the source that Project Navigator will create based on your settings. Review the summary to make sure it matches what is shown in the dialog box. If it does not, go "Back" and correct any errors. Otherwise, click "Finish" to complete this process. The new source file will be automatically opened in the text editor.

In the text editor, some of the basic file structure is already in place. Keywords are displayed in blue, data types in red, comments in green, and values in black. This color-coding enhances readability and recognition of typographical errors. Now, enter the test bench you prepared in prelab question 2. At this point, you should end up with a window that looks somewhat like that shown in Figure 8. Once you are satisfied, save the file and close the window. It is a good idea to get in the habit of saving your project.

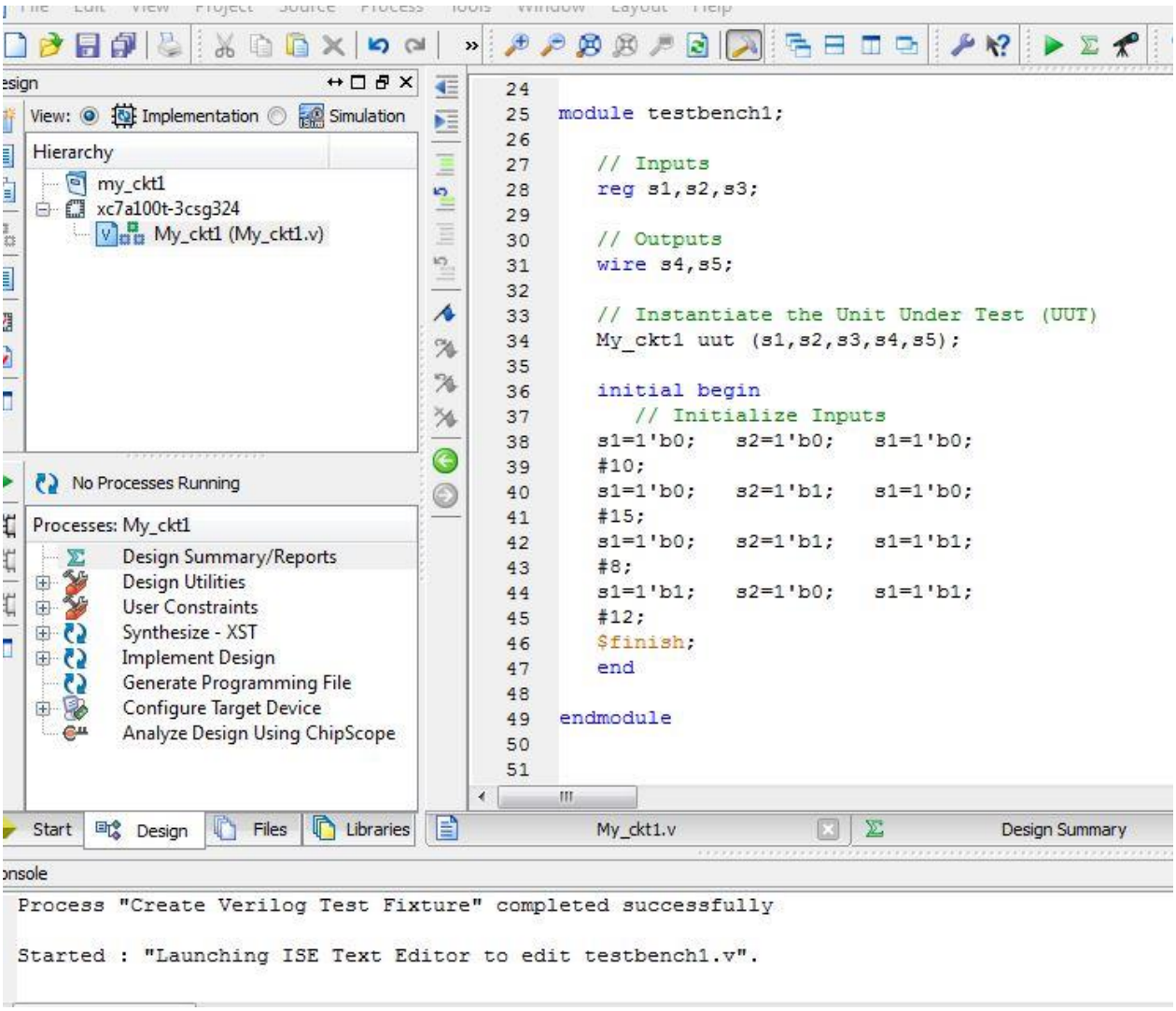

Figure 8: Completed Test bench

Now that you have a test bench in your project, you can perform functional simulation on the design. The simulation processes enable you to run simulation on the design using ISim Simulator. First mark simulation option on the left column. After than you will see your project, test bench file and module file in the hierarchy window. Here you should select your test bench file. Then, click the + next to the ISim Simulator entry in the Processes for Current Source window to expand the item, this is also shown in Figure 9.

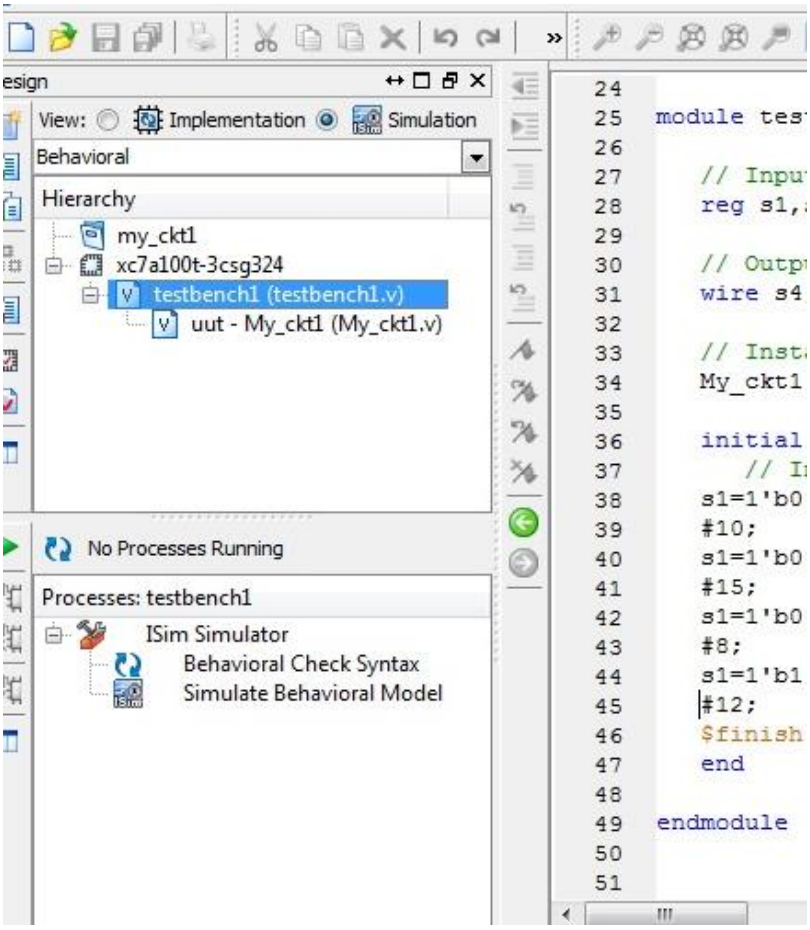

Figure 9: Hierarchy and Processes windows

After then, to start the simulation, double-click Simulate Behavioral Model. Finally you will have the window that you can see the input and output signals as it is given in Figure 10.

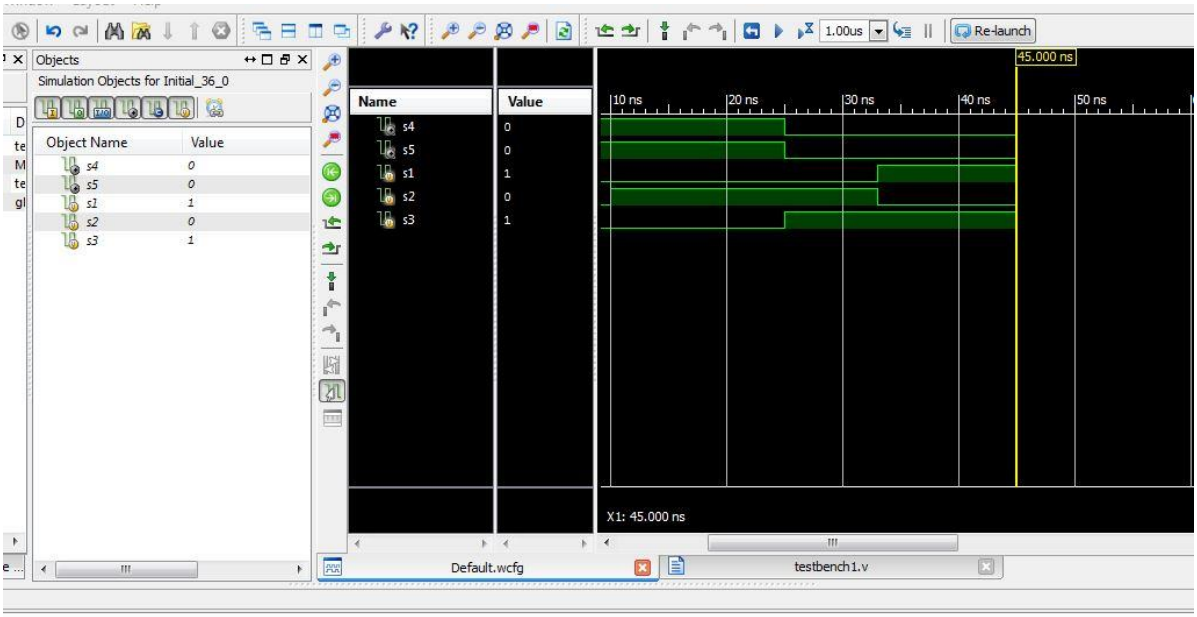

Figure 10: Simulation Results